



1990
MILITARY PRODUCTS
DATABOOK

MONOLITHIC INTEGRATED CIRCUITS
HYBRID CIRCUITS

APRIL 1990



**MILITARY PRODUCTS DATABOOK
1990**

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Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.:

RE29,619, RE29,992, RE30,586, RE31,850, DES. 233,909, 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,268,759, 4,270,118, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399,345, 4,400,689, 4,400,690, 4,427,973, 4,439,724, 4,460,891, 4,475,103, 4,475,169, 4,476,538, 4,481,708, 4,484,149, 4,485,372, 4,491,825, 4,511,413, 4,521,764, 4,543,560, 4,543,561, 4,547,766, 4,547,961, 4,556,870, 4,558,242, 4,562,400, 4,565,000, 4,586,019, 4,586,155, 4,590,456, 4,596,976, 4,601,760, 4,604,532, 4,608,541, 4,622,512, 4,626,769, 4,639,683, 4,644,253, 4,646,056, 4,646,238, 4,678,936, 4,684,922, 4,685,200, 4,694,276, 4,697,151, 4,703,283, 4,707,682, 4,709,167, 4,717,883, 4,722,910, 4,742,331, 4,751,455, 4,752,900, 4,761,636, 4,769,564, 4,771,011, 4,774,685, 4,791,318, 4,791,551, 4,800,524, 4,804,960, 4,808,908, 4,811,296, 4,814,767, 4,833,345, 4,839,653, 4,855,585, 4,855,618, 4,855,684, 4,857,862, 4,859,944, 4,862,073, 4,864,454, 4,866,505, 4,878,770, 4,879,505, 4,884,075

France:

111.833, 70.10561, 75.27557, 76 08238, 77 20799, 78 10462, 79 24041, 80 00960, 80 11312, 80 11916, 81 02661, 81 14845, 83 03140, 96 08238

Japan:

1,092,928, 1,242,936, 1,242,965, 1,306,235, 1,337,318, 1,401,661, 1,412,991, 1,432,164

West Germany:

2,014 034, 25 40 451.7, 26 11 858.1

U.K.:

1,310,591, 1,310,592, 1,537,542, 1,590,136, 1,590,137, 1,599,538, 2,008,876, 2,032,659, 2,040,087, 2,050,740, 2,054,992, 2,075,295, 2,081,040, 2,087,656, 2,103,884, 2,104,288, 2,107,951, 2,115,932, 2,118,386, 2,119,139, 2,119,547, 2,126,445, 2,126,814, 2,135,545, 2,137,787

Canada:

984,015, 1,006,236, 1,025,558, 1,035,464, 1,054,248, 1,141,034, 1,141,820, 1,142,445, 1,143,306, 1,150,414, 1,153,607, 1,157,571, 1,159,956, 1,177,127, 1,177,966, 1,184,662, 1,184,663, 1,191,715, 1,192,310, 1,192,311, 1,192,312, 1,203,628, 1,205,920, 1,212,730, 1,214,282, 1,219,679, 1,219,966, 1,223,086, 1,232,366, 1,233,913, 1,234,921, 1,140,267

Sweden:

7603320-8

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General Introduction

This databook was developed to provide defense system suppliers with complete information for devices processed in accordance with MIL-STD-883 and offered as part of Analog Devices standard 883 program. All products specified in this databook are available as catalog items from Analog Devices.

The information contained in this databook, in terms of both content and format, facilitate the preparation of Standard Military or Source Control Drawings (SMDs or SCDs). If you would like to sponsor an SMD for a part that does not currently have a drawing assigned, Analog Devices would be pleased to support your effort. To initiate this process, simply contact your local sales representative.

NEW PRODUCTS

Most new products released by Analog Devices after the publication of this databook will be available as 883 compliant products. Information on availability of new 883 products can be provided by your local sales representative. Information will also be provided in "Analog Briefings."

CERTIFICATES OF CONFORMANCE

A Certificate of Conformance (C of C) certifying that the devices received meet all applicable specifications is furnished at no charge.

ATTRIBUTES DATA

A copy of attributes data (screening tests for the date code(s) of devices supplied) can be made available upon request. There will be no charge for providing this data.

GROUPS A AND B DATA

A copy of the Group A and B (quality conformance) attributes data for the date code(s) of the devices can be supplied at no charge when specified at the time of order placement.

GROUP C AND D GENERIC DATA

Quality conformance attributes data from generically similar die and/or packages can be made available, when specified at time of order placement, and specified on the conforming purchase order. Generic data is compiled in accordance with MIL-STD-883 and MIL-M-38510. This data is available at no charge.

If specified lot related Group C or D testing is required, contact a local sales office. A quotation will be prepared for your specific needs.

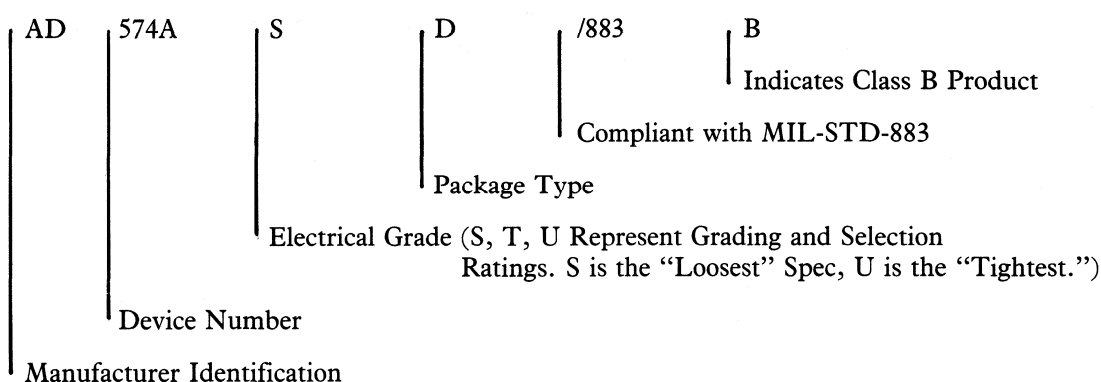
Ordering Guide

This Ordering Guide should make it easy to order Analog Devices products. Model numbers can be found in paragraph 1.2 of the Detail Specifications.

1. Find the correct part number and package options you want.
2. Get a price quotation from the local sales office in your area. These locations are listed at the back of this databook.

HOW TO FIND THE PART NUMBER

The complete part number can be found in paragraph 1.2 of the Device Specification when only one package type is available. The part number is composed as follows:



When there are package options available, paragraph 1.2 then refers to paragraph 1.2.3 where the package options are listed with the corresponding letter designator. Substitute the package designator symbol for the (X) in the part number shown in paragraph 1.2.

Example:

PARA 1.2

Device	Part Number ¹
-1	AD574AS(X)/883B
-2	AD574AT(X)/883B
-3	AD574AU(X)/883B

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

PARA 1.2.3

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28A	28-Pin LCC

If the dash-1 device is the product desired, go to paragraph 1.2.3 and choose the desired package, i.e., the LCC, the "E" package. The complete part number for ordering, therefore, is AD574ASE/883B.

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MIL-M-38510 and Military Drawing Cross Reference

BY JAN NUMBER

JAN Part Number	Generic Part Number	Description
JM38510/12101BJC	AD562SD	12-Bit Current-Output DAC
JM38510/12103BJC	AD565SD	12-Bit Current-Output DAC
JM38510/12702BEC	AD7520UD	10-Bit Multiplying DAC
JM38510/12801BGA	AD584SH	Multitap Reference
JM38510/12802BGA	AD584TH	Multitap Reference
JM38510/13301BEA	AD561SD	10-Bit DAC, I _{OUT}
JM38510/13901BCA	AD534TD	Analog Multiplier, Programmable Scale
JM38510/13901BIA	AD534TH	Analog Multiplier, Programmable Scale
JM38510/13902BCA	AD534SD	Analog Multiplier, Programmable Scale
JM38510/13902BIA	AD534SH	Analog Multiplier, Programmable Scale
JM38510/13903BCA	AD532SD	Analog Multiplier, Programmable Scale
JM38510/13903BIA	AD532SH	Analog Multiplier, Programmable Scale
JM38510/14001BXA	AD574AUD	Complete 12-Bit ADC*
JM38510/14002BXA	AD574ATD	Complete 12-Bit ADC*

Generic Part Number	JAN Part Number	Description
AD532SD	JM38510/13903BCA	Analog Multiplier, Programmable Scale
AD532SH	JM38510/13903BIA	Analog Multiplier, Programmable Scale
AD534SD	JM38510/13902BCA	Analog Multiplier, Programmable Scale
AD534SH	JM38510/13902BIA	Analog Multiplier, Programmable Scale
AD534TD	JM38510/13901BCA	Analog Multiplier, Programmable Scale
AD534TH	JM38510/13901BIA	Analog Multiplier, Programmable Scale
AD561SD	JM38510/13301BEA	10-Bit DAC, I _{OUT}
AD562SD	JM38510/12101BJC	12-Bit Current Output DAC
AD565SD	JM38510/12103BJC	12-Bit Current Output DAC
AD574ATD	JM38510/14002BXA	Complete 12-Bit ADC*
AD574AUD	JM38510/14001BXA	Complete 12-Bit ADC*
AD584SH	JM38510/12801BGA	Multitap Reference
AD584TH	JM38510/12802BGA	Multitap Reference
AD7520UD	JM38510/12702BEC	10-Bit Multiplying DAC

* μ P compatible.

**Release pending.

BY SMD PART NUMBER

SMD Part Number	Generic Part Number	Description
5962-7801903EA	AD96687TQ/883B	Voltage Comparator
5962-78019032A	AD96687TE/883B	Voltage Comparator
5962-80013	ADLH0032/883B	High Speed Op Amp
5962-80014	ADLH0033/883B	High Speed Buffer Amp
5962-8300201JC	ADDAC87-CBI-V/883B	12-Bit Hybrid DAC
5962-8503001XC	AD2700SD/883B	Precision +10 V Reference
5962-8503002XC	AD2700UD/883B	Precision +10 V Reference
5962-8503003XC	AD2702SD/883B	Precision ± 10 V Reference
5962-8503004XC	AD2702UD/883B	Precision ± 10 V Reference
5962-8512701XA	AD574AUD/883B	Complete, 12-Bit ADC*
5962-85127013C	AD574AUE/883B	Complete, 12-Bit ADC**
5962-8512702XA	AD574ATD/883B	Complete, 12-Bit ADC*
5962-85127023C	AD574ATE/883B	Complete, 12-Bit ADC**
5962-8600804EA**	AD96685TQ/883B	Voltage Comparator
5962-86008042A**	AD96685TE/883B	Voltage Comparator
5962-8600804IA**	AD96685TH/883B	Voltage Comparator
5962-86716012X	ADG201HSTE/883B	Quad SPST Fast Switch
5962-8671601EX	ADG201HSTQ/883B	Quad SPST Fast Switch
5962-8680201VA	AD570SD/883B	Complete, 8-Bit ADC
5962-8680202VA	AD571SD/883B	Complete, 10-Bit ADC
5962-8686101XC	AD580SH/883B	Precision +2.5 V Reference
5962-8686102XC	AD580TH/883B	Precision +2.5 V Reference
5962-8686103XC	AD580UH/883B	Precision +2.5 V Reference
5962-8688201*	AD581SH/883B	+10 V Reference
5962-8688202*	AD581TH/883B	+10 V Reference
5962-8688203*	AD581UH/883B	+10 V Reference
5962-87540012C	AD585SE/883B	High Speed S/H Amp
5962-8754001CA	AD585SQ/883B	High Speed S/H Amp
5962-8757101XC	AD590JF/883B	Temperature Transducer 1 μ A/K
5962-8757101YC	AD590JH/883B	Temperature Transducer 1 μ A/K
5962-8757102XC	AD590KF/883B	Temperature Transducer 1 μ A/K
5962-8757102YC	AD590KH/883B	Temperature Transducer 1 μ A/K
5962-8757103XC	AD590LF/883B	Temperature Transducer 1 μ A/K
5962-8757103YC	AD590LH/883B	Temperature Transducer 1 μ A/K
5962-8757104XC	AD590MF/883B	Temperature Transducer 1 μ A/K
5962-8757104YC	AD590MH/883B	Temperature Transducer 1 μ A/K
5962-87591013X	AD7572SE12/883B	Complete, 12-Bit 12 μ s ADC*
5962-8759101LX	AD7572SQ12/883B	Complete, 12-Bit 12 μ s ADC*
5962-87591023X	AD7572TE12/883B	Complete, 12-Bit 12 μ s ADC*
5962-8759102LX	AD7572TQ12/883B	Complete, 12-Bit 12 μ s ADC*
5962-87591033X	AD7572UE12/883B	Complete, 12-Bit 12 μ s ADC*
5962-8759103LX	AD7572UQ12/883B	Complete, 12-Bit 12 μ s ADC*

* μ P compatible.

**Release pending.

SMD Part Number	Generic Part Number	Description
5962-87591043X	AD7572SE05/883B	Complete, 12-Bit 5 μ s ADC*
5962-8759104LX	AD7572SQ05/883B	Complete, 12-Bit 5 μ s ADC*
5962-87591053X	AD7572TE05/883B	Complete, 12-Bit 5 μ s ADC*
5962-8759105LX	AD7572TQ05/883B	Complete, 12-Bit 5 μ s ADC*
5962-87591063X	AD7572UE05/883B	Complete, 12-Bit 5 μ s ADC*
5962-8759106LX	AD7572UQ05/883B	Complete, 12-Bit 5 μ s ADC*
5962-8763501RA**	AD670SD/883B	Signal Conditioning 8-Bit ADC
5962-8768901VX	ADG528ATQ/883B	8-Channel Latched MUX
5962-87700012X	AD7524SE/883B	8-Bit DAC*
5962-8770001EX	AD7524SQ/883B	8-Bit DAC*
5962-87700022X	AD7524TE/883B	8-Bit DAC*
5962-8770002EX	AD7524TQ/883B	8-Bit DAC*
5962-87700032X	AD7524UE/883B	8-Bit DAC*
5962-8770003EX	AD7524UQ/883B	8-Bit DAC*
5962-87701012X	AD7528SE/883B	8-Bit Dual Buffered DAC*
5962-8770101RX	AD7528SQ/883B	8-Bit Dual Buffered DAC*
5962-87701022X	AD7528TE/883B	8-Bit Dual Buffered DAC*
5962-8770102RX	AD7528TQ/883B	8-Bit Dual Buffered DAC*
5962-87701032X	AD7528UE/883B	8-Bit Dual Buffered DAC*
5962-8770103RX	AD7528UQ/883B	8-Bit Dual Buffered DAC*
5962-87702012X	AD7545SE/883B	12-Bit Multiplying DAC*
5962-87702022X	AD7545TE/883B	12-Bit Multiplying DAC*
5962-8770202RX	AD7545TQ/883B	12-Bit Multiplying DAC*
5962-87702032X	AD7545UE/883B	12-Bit Multiplying DAC*
5962-8770203RX	AD7545UQ/883B	12-Bit Multiplying DAC*
5962-87702042X	AD7545GUE/883B	12-Bit Multiplying DAC*
5962-8770204RX	AD7545GUQ/883B	12-Bit Multiplying DAC*
5962-877020IRX	AD7545SQ/883B	12-Bit Multiplying DAC*
5962-877190IEA	AD625SD/883B	Instrumentation Amp
5962-8773501XX	ADSP-2100SG/883B	6 MHz Digital Signal μ P
5962-8773503XX	ADSP-2100ASG/883B	8 MHz Digital Signal μ P
5962-8773504XX	ADSP-2100ATG/883B	10 MHz Digital Signal μ P
5962-87762012X	AD7575SE/883B	8-Bit ADC with T/H*
5962-8776201VX	AD7575SQ/883B	8-Bit ADC with T/H*
5962-87762022X	AD7575TE/883B	8-Bit ADC with T/H*
5962-8776202VX	AD7575TQ/883B	8-Bit ADC with T/H*
5962-87763013X	AD7537SE/883B	12-Bit Dual Multiplying DAC*
5962-8776301LX	AD7537SQ/883B	12-Bit Dual Multiplying DAC*
5962-87763023X	AD7537TE/883B	12-Bit Dual Multiplying DAC*
5962-8776302LX	AD7537TQ/883B	12-Bit Dual Multiplying DAC*
5962-87763033X	AD7537UE/883B	12-Bit Dual Multiplying DAC*
5962-8776303LX	AD7537UQ/883B	12-Bit Dual Multiplying DAC*
5962-87789012C	AD558SE/883B	8-Bit DACPORT™**
5962-8778901EA	AD558SD/883B	8-Bit DACPORT™**
5962-87789022C	AD558TE/883B	8-Bit DACPORT™**
5962-8778902EA	AD558TD/883B	8-Bit DACPORT™**
5962-8780101XA	AD567SD/883B	12-Bit High Speed DAC*
5962-87802012X	AD7226TE/883B	8-Bit Quad DAC with Amps*
5962-8780201RX	AD7226TQ/883B	8-Bit Quad DAC with Amps*

* μ P compatible.

**Release pending.

SMD Part Number	Generic Part Number	Description
5962-8850501RA	AD573SD/883B	10-Bit ADC
5962-8850502RA	AD673SD/883B	8-Bit ADC
5962-8850901X	AD390SD/883B	12-Bit Quad DAC
5962-8850902X	AD390TD/883B	12-Bit Quad DAC
5962-8851001X	AD394SD/883B	12-Bit Quad DAC
5962-8851002X	AD394TD/883B	12-Bit Quad DAC
5962-8851003X	AD395SD/883B	12-Bit Quad DAC
5962-8851004X	AD395TD/883B	12-Bit Quad DAC
5962-885390IEA	AD524SD/883B	Instrumentation Amp
5962-88579	HOS-050A/883B	Video Op Amp
5962-88579	HOS-060SH/883B	Video Op Amp
5962-88615013C	AD674AUE/883B	Complete 12-Bit ADC**
5962-8861501XA**	AD674AUD/883B	Complete, 12-Bit ADC*
5962-88615023C	AD674ATE/883B	Complete 12-Bit ADC**
5962-8861502XA**	AD674ATD/883B	Complete, 12-Bit ADC*
5962-88650012X**	AD7820TE/883B	8-Bit, 2 μ s ADC with T/H*
5962-8865001RX**	AD7820TQ/883B	8-Bit, 2 μ s ADC with T/H*
5962-88650022X**	AD7820UE/883B	8-Bit, 2 μ s ADC with T/H*
5962-8865002RX**	AD7820UQ/883B	8-Bit, 2 μ s ADC with T/H*
5962-88659013C	AD667SE/883B	12-Bit Dual Buffered DAC**
5962-8865901XA	AD667SD/883B	12-Bit Dual Buffered DAC*
5962-8866023X**	AD7228UE/883B	8-Bit Octal Voltage Out DAC*
5962-886602LX**	AD7228UQ/883B	8-Bit Octal Voltage Out DAC*
5962-88663013X**	AD7228TE/883B	8-Bit Octal Voltage Out DAC*
5962-8866301LX**	AD7228TQ/883B	8-Bit Octal Voltage Out DAC*
5962-8876401LX**	AD7824TQ/883B	4-Channel 8-Bit ADC*
5962-8876402LX**	AD7824UQ/883B	4-Channel 8-Bit ADC*
5962-8876403XX**	AD7828TQ/883B	8-Channel 8-Bit ADC*
5962-8876404XX**	AD7828UQ/883B	8-Channel 8-Bit ADC*
5962-8876501RX**	AD7549SQ/883B	12-Bit Dual DAC*
5962-8876502RX**	AD7549TQ/883B	12-Bit Dual DAC*
5962-8876601LX**	AD7245SQ/883B	12-Bit DACPORT™*
5962-8876602RX**	AD7248SQ/883B	12-Bit DACPORT™*
5962-8876701LX**	AD7845SQ/883B	12-Bit V _{OUT} Multiplying DAC*
5962-8951801RX**	AD7821TQ/883B	8-Bit, 600 ns ADC with T/H*
5962-8961601VX**	AD7574SQ/883B	8-Bit ADC*
5962-8961602VX**	AD7574TQ/883B	8-Bit ADC*
5962-8961701LA	AD767SD/883B	12-Bit DAC**
5962-8962901LX**	AD7569SQ/883B	Complete 8-Bit Analog I/O System*
5962-8962902LX	AD7569TQ/883B	Complete 8-Bit Analog I/O System*
5962-8965501LX**	AD7672TQ10/883B	12-Bit High Speed ADC*
5962-8965502LX**	AD7672UQ10/883B	12-Bit High Speed ADC*
5962-8965503LX**	AD7672TQ05/883B	12-Bit High Speed ADC*
5962-8965504LX**	AD7672UQ05/883B	12-Bit High Speed ADC*
5962-8965701LX**	AD7547SQ/883B	12-Bit Dual Multiplying DAC*
5962-8965702LX**	AD7547TQ/883B	12-Bit Dual Multiplying DAC*
5962-8965703LX**	AD7547UQ/883B	12-Bit Dual Multiplying DAC*

* μ P compatible.

**Release pending.

SMD Part Number	Generic Part Number	Description
5962-89728012C	AD588SE/883B	Programmable Reference
5962-8972801EA	AD588SD/883B	Programmable Reference
5962-89728022C	AD588TE/883B	Programmable Reference
5962-8972802EA	AD588TD/883B	Programmable Reference
5962-89822501PA	AD587SQ/883B	Precision +10 V Reference
5962-89822502PA	AD587TQ/883B	Precision +10 V Reference
5962-89822503PA	AD587UQ/883B	Precision +10 V Reference
5962-8982401PA	AD586SQ/883B	Precision +5 V Reference
5962-8982402PA	AD586TQ/883B	Precision +5 V Reference
77052012X**	ADG508ATE/883B	8-Channel Analog MUX
7705201EX	ADG508ATQ/883B	8-Channel Analog MUX
77053022X	ADG201ATE/883B	Quad SPST Analog Switch
7705302EX	ADG201ATQ/883B	Quad SPST Analog Switch
8300301JA	ADDAC87D-CBI-V/883B	12-Bit Monolithic DAC

BY GENERIC PART NUMBER

Generic Part Number	SMD Part Number	Description
AD390SD/883B	5962-8850901X	12-Bit Quad DAC
AD390TD/883B	5962-8850902X	12-Bit Quad DAC
AD394SD/883B	5962-8851001X	12-Bit Quad DAC
AD394TD/883B	5962-8851002X	12-Bit Quad DAC
AD395SD/883B	5962-8851003X	12-Bit Quad DAC
AD395TD/883B	5962-8851004X	12-Bit Quad DAC
AD524SD/883B	5962-885390IEA	Instrumentation Amp
AD558SD/883B	5962-8778901EA	8-Bit DACPORT™★
AD558SE/883B	5962-87789012C	8-Bit DACPORT™★★
AD558TD/883B	5962-8778902EA	8-Bit DACPORT™★
AD558TE/883B	5962-87789022C	8-Bit DACPORT™★★
AD567SD/883B	5962-8780101XA	12-Bit High Speed DAC★
AD570SD/883B	5962-8680201VA	Complete, 8-Bit ADC
AD571SD/883B	5962-8680202VA	Complete, 10-Bit ADC
AD573SD/883B	5962-8850501RA	10-Bit ADC
AD574ATD/883B	5962-8512702XA	Complete, 12-Bit ADC★
AD574ATE/883B	5962-85127023C	Complete, 12-Bit ADC★★
AD574AUD/883B	5962-8512701XA	Complete, 12-Bit ADC★
AD574AUE/883B	5962-85127013C	Complete, 12-Bit ADC★★
AD580SH/883B	5962-8686101XC	Precision +2.5 V Reference
AD580TH/883B	5962-8686102XC	Precision +2.5 V Reference
AD580UH/883B	5962-8686103XC	Precision +2.5 V Reference
AD581SH/883B	5962-8688201★	+10 V Reference
AD581TH/883B	5962-8688202★	+10 V Reference
AD581UH/883B	5962-8688203★	+10 V Reference
AD585SE/883B	5962-87540012C	High Speed S/H Amp
AD585SQ/883B	5962-8754001CA	High Speed S/H Amp
AD586SQ/883B	5962-8982401PA	Precision +5 V Reference
AD586TQ/883B	5962-8982402PA	Precision +5 V Reference
AD587SQ/883B	5962-89822501PA	Precision +10 V Reference
AD587TQ/883B	5962-89822502PA	Precision +10 V Reference
AD587UQ/883B	5962-89822503PA	Precision +10 V Reference

*μP compatible.
 **Release pending.

Generic Part Number	SMD Part Number	Description
AD588SD/883B	5962-8972801EA	Programmable Reference
AD588SE/883B	5962-89728012C	Programmable Reference
AD588TD/883B	5962-8972802EA	Programmable Reference
AD588TE/883B	5962-89728022C	Programmable Reference
AD590JF/883B	5962-8757101XC	Temperature Transducer 1 μ A/K
AD590JH/883B	5962-8757101YC	Temperature Transducer 1 μ A/K
AD590KF/883B	5962-8757102XC	Temperature Transducer 1 μ A/K
AD590KH/883B	5962-8757102YC	Temperature Transducer 1 μ A/K
AD590LF/883B	5962-8757103XC	Temperature Transducer 1 μ A/K
AD590LH/883B	5962-8757103YC	Temperature Transducer 1 μ A/K
AD590MF/883B	5962-8757104XC	Temperature Transducer 1 μ A/K
AD590MH/883B	5962-8757104YC	Temperature Transducer 1 μ A/K
AD625SD/883B	5962-8771901EA	Instrumentation Amp
AD667SD/883B	5962-8865901XA	12-Bit Dual Buffered DAC*
AD667SE/883B	5962-88659013C	12-Bit Dual Buffered DAC**
AD670SD/883B	5962-8763501RA**	Signal Conditioning 8-Bit ADC
AD673SD/883B	5962-8850502RA	8-Bit ADC
AD674ATD/883B	5962-8861502XA**	Complete, 12-Bit ADC*
AD674ATE/883B	5962-88615023C	Complete, 12-Bit ADC**
AD674AUD/883B	5962-8861501XA**	Complete, 12-Bit ADC*
AD674AUE/883B	5962-88615013C	Complete, 12-Bit ADC**
AD2700SD/883B	5962-8503001XC	Precision +10V Reference
AD2700UD/883B	5962-8503002XC	Precision +10V Reference
AD2702SD/883B	5962-8503003XC	Precision $\pm$ 10V Reference
AD2702UD/883B	5962-8503004XC	Precision $\pm$ 10V Reference
AD7226TE/883B	5962-87802012X	8-Bit Quad DAC with Amps*
AD7226TQ/883B	5962-8780201RX	8-Bit Quad DAC with Amps*
AD7228TE/883B	5962-88663013X**	8-Bit Octal Voltage Out DAC*
AD7228TQ/883B	5962-8866301LX**	8-Bit Octal Voltage Out DAC*
AD7228UE/883B	5962-8866023X**	8-Bit Octal Voltage Out DAC*
AD7228UQ/883B	5962-886602LX**	8-Bit Octal Voltage Out DAC*
AD7245SQ/883B	5962-8876601LX**	12-Bit DACPORT™*
AD7248SQ/883B	5962-8876602RX**	12-Bit DACPORT™*
AD7524SE/883B	5962-87700012X	8-Bit DAC*
AD7524SQ/883B	5962-8770001EX	8-Bit DAC*
AD7524TE/883B	5962-87700022X	8-Bit DAC*
AD7524TQ/883B	5962-8770002EX	8-Bit DAC*
AD7524UE/883B	5962-87700032X	8-Bit DAC*
AD7524UQ/883B	5962-8770003EX	8-Bit DAC*
AD7528SE/883B	5962-87701012X	8-Bit Dual Buffered DAC*
AD7528SQ/883B	5962-8770101RX	8-Bit Dual Buffered DAC*
AD7528TE/883B	5962-87701022X	8-Bit Dual Buffered DAC*
AD7528TQ/883B	5962-8770102RX	8-Bit Dual Buffered DAC*
AD7528UE/883B	5962-87701032X	8-Bit Dual Buffered DAC*
AD7528UQ/883B	5962-8770103RX	8-Bit Dual Buffered DAC*
AD7537SE/883B	5962-87763013X	12-Bit Dual Multiplying DAC*
AD7537SQ/883B	5962-8776301LX	12-Bit Dual Multiplying DAC*
AD7537TE/883B	5962-87763023X	12-Bit Dual Multiplying DAC*
AD7537TQ/883B	5962-8776302LX	12-Bit Dual Multiplying DAC*

* μ P compatible.

**Release pending.

Generic Part Number	SMD Part Number	Description
AD7537UE/883B	5962-87763033X	12-Bit Dual Multiplying DAC*
AD7537UQ/883B	5962-8776303LX	12-Bit Dual Multiplying DAC*
AD7545GUE/883B	5962-87702042X	12-Bit Multiplying DAC*
AD7545GUQ/883B	5962-8770204RX	12-Bit Multiplying DAC*
AD7545SE/883B	5962-87702012X	12-Bit Multiplying DAC*
AD7545SQ/883B	5962-8770201RX	12-Bit Multiplying DAC*
AD7545TE/883B	5962-87702022X	12-Bit Multiplying DAC*
AD7545TQ/883B	5962-8770202RX	12-Bit Multiplying DAC*
AD7545UE/883B	5962-87702032X	12-Bit Multiplying DAC*
AD7545UQ/883B	5962-8770203RX	12-Bit Multiplying DAC*
AD7547SQ/883B	5962-8965701LX**	12-Bit Dual Multiplying DAC*
AD7547TQ/883B	5962-8965702LX**	12-Bit Dual Multiplying DAC*
AD7547UQ/883B	5962-8965703LX**	12-Bit Dual Multiplying DAC*
AD7549SQ/883B	5962-8876501RX**	12-Bit Dual DAC*
AD7549TQ/883B	5962-8876502RX**	12-Bit Dual DAC*
AD7569SQ/883B	5962-8962901LX**	Complete 8-Bit Analog I/O System*
AD7569TQ/883B	5962-8962902LX	Complete 8-Bit Analog I/O System*
AD7572SE05/883B	5962-87591043X	Complete, 12-Bit 5 μ s ADC*
AD7572SE12/883B	5962-87591013X	Complete, 12-Bit 12 μ s ADC*
AD7572SQ05/883B	5962-8759104LX	Complete, 12-Bit 5 μ s ADC*
AD7572SQ12/883B	5962-8759101LX	Complete, 12-Bit 12 μ s ADC*
AD7572TE05/883B	5962-87591053X	Complete, 12-Bit 5 μ s ADC*
AD7572TE12/883B	5962-87591023X	Complete, 12-Bit 12 μ s ADC*
AD7572TQ05/883B	5962-8759105LX	Complete, 12-Bit 5 μ s ADC*
AD7572TQ12/883B	5962-8759102LX	Complete, 12-Bit 12 μ s ADC*
AD7572UE05/883B	5962-87591063X	Complete, 12-Bit 5 μ s ADC*
AD7572UE12/883B	5962-87591033X	Complete, 12-Bit 12 μ s ADC*
AD7572UQ05/883B	5962-8759106LX	Complete, 12-Bit 5 μ s ADC*
AD7572UQ12/883B	5962-8759103LX	Complete, 12-Bit 12 μ s ADC*
AD7574SQ/883B	5962-8961601VX**	8-Bit ADC*
AD7574TQ/883B	5962-8961602VX**	8-Bit ADC*
AD7575SE/883B	5962-87762012X	8-Bit ADC with T/H*
AD7575SQ/883B	5962-8776201VX	8-Bit ADC with T/H*
AD7575TE/883B	5962-87762022X	8-Bit ADC with T/H*
AD7575TQ/883B	5962-8776202VX	8-Bit ADC with T/H*
AD767SD/883B	5962-8961701LA	12-Bit DAC**
AD7672TQ05/883B	5962-8965503LX**	12-Bit High Speed ADC*
AD7672TQ10/883B	5962-8965501LX**	12-Bit High Speed ADC*
AD7672UQ05/883B	5962-8965504LX**	12-Bit High Speed ADC*
AD7672UQ10/883B	5962-8965502LX**	12-Bit High Speed ADC*
AD7820TE/883B	5962-88650012X**	8-Bit, 2 μ s ADC with T/H*
AD7820TQ/883B	5962-8865001RX**	8-Bit, 2 μ s ADC with T/H*
AD7820UE/883B	5962-88650022X**	8-Bit, 2 μ s ADC with T/H*
AD7820UQ/883B	5962-8865002RX**	8-Bit, 2 μ s ADC with T/H*
AD7821TQ/883B	5962-8951801RX**	8-Bit, 600 ns ADC with T/H*
AD7824TQ/883B	5962-8876401LX**	4-Channel 8-Bit ADC*
AD7824UQ/883B	5962-8876402LX**	4-Channel 8-Bit ADC*
AD7828TQ/883B	5962-8876403XX**	8-Channel 8-Bit ADC*
AD7828UQ/883B	5962-8876404XX**	8-Channel 8-Bit ADC*

* μ P compatible.

**Release pending.

Generic Part Number	SMD Part Number	Description
AD7845SQ/883B	5962-8876701LX**	12-Bit V _{OUT} Multiplying DAC*
AD96685TE/883B	5962-8600804EA**	Voltage Comparator
AD96685TH/883B	5962-86008042A**	Voltage Comparator
AD96685TQ/883B	5962-8600804IA**	Voltage Comparator
AD96687TE/883B	5962-7801903EA	Voltage Comparator
AD96687TQ/883B	5962-78019032A	Voltage Comparator
AD DAC87-CBI-V/883B	5962-8300201JC	12-Bit Hybrid DAC
AD DAC87D-CBI-V/883B	8300301JA	12-Bit Monolithic DAC
ADG201ATE/883B	77053022X	Quad SPST Analog Switch
ADG201ATQ/883B	7705302EX	Quad SPST Analog Switch
ADG201HSTE/883B	5962-86716012X	Quad SPST Fast Switch
ADG201HSTQ/883B	5962-8671601EX	Quad SPST Fast Switch
ADG508ATE/883B	77052012X**	8-Channel Analog MUX
ADG508ATQ/883B	7705201EX	8-Channel Analog MUX
ADG528ATQ/883B	5962-8768901VX	8-Channel Latched MUX
ADLH0032/883B	5962-80013	High Speed Op Amp
ADLH0033/883B	5962-80014	High Speed Buffer Amp
ADSP-2100ASG/883B	5962-8773503XX	8 MHz Digital Signal μ P
ADSP-2100ATG/883B	5962-8773504XX	10 MHz Digital Signal μ P
ADSP-2100SG/883B	5962-8773501XX	6 MHz Digital Signal μ P
HOS-050A/883B	5962-88579	Video Op Amp
HOS-060SH/883B	5962-88579	Video Op Amp

BY FUNCTION

D/A CONVERTERS

Generic Part Number	SMD Part Number	Description
AD390SD/883B	5962-8850901X	12-Bit Quad DAC
AD390TD/883B	5962-8850902X	12-Bit Quad DAC
AD394SD/883B	5962-8851001X	12-Bit Quad DAC
AD394TD/883B	5962-8851002X	12-Bit Quad DAC
AD395SD/883B	5962-8851003X	12-Bit Quad DAC
AD395TD/883B	5962-8851004X	12-Bit Quad DAC
AD558SD/883B	5962-8778901EA	8-Bit DACPORT™*
AD558SE/883B	5962-87789012C	8-Bit DACPORT™**
AD558TD/883B	5962-8778902EA	8-Bit DACPORT™*
AD558TE/883B	5962-87789022C	8-Bit DACPORT™**
AD567SD/883B	5962-8780101XA	12-Bit High Speed DAC*
AD667SD/883B	5962-8865901XA	12-Bit Dual Buffered DAC*
AD667SE/883B	5962-88659013C	12-Bit Dual Buffered DAC**
AD7226TE/883B	5962-87802012X	8-Bit Quad DAC with Amps*
AD7226TQ/883B	5962-8780201RX	8-Bit Quad DAC with Amps*
AD7228TE/883B	5962-88663013X**	8-Bit Octal Voltage Out DAC*
AD7228TQ/883B	5962-8866301LX**	8-Bit Octal Voltage Out DAC*
AD7228UE/883B	5962-8866023X**	8-Bit Octal Voltage Out DAC*
AD7228UQ/883B	5962-886602LX**	8-Bit Octal Voltage Out DAC*
AD7245SQ/883B	5962-8876601LX**	12-Bit DACPORT™*
AD7248SQ/883B	5962-8876602RX**	12-Bit DACPORT™*

* μ P compatible.

**Release pending.

Generic Part Number	SMD Part Number	Description
AD7524SE/883B	5962-87700012X	8-Bit DAC*
AD7524SQ/883B	5962-8770001EX	8-Bit DAC*
AD7524TE/883B	5962-87700022X	8-Bit DAC*
AD7524TQ/883B	5962-8770002EX	8-Bit DAC*
AD7524UE/883B	5962-87700032X	8-Bit DAC*
AD7524UQ/883B	5962-8770003EX	8-Bit DAC*
AD7528SE/883B	5962-87701012X	8-Bit Dual Buffered DAC*
AD7528SQ/883B	5962-8770101RX	8-Bit Dual Buffered DAC*
AD7528TE/883B	5962-87701022X	8-Bit Dual Buffered DAC*
AD7528TQ/883B	5962-8770102RX	8-Bit Dual Buffered DAC*
AD7528UE/883B	5962-87701032X	8-Bit Dual Buffered DAC*
AD7528UQ/883B	5962-8770103RX	8-Bit Dual Buffered DAC*
AD7537SE/883B	5962-87763013X	12-Bit Dual Multiplying DAC*
AD7537SQ/883B	5962-8776301LX	12-Bit Dual Multiplying DAC*
AD7537TE/883B	5962-87763023X	12-Bit Dual Multiplying DAC*
AD7537TQ/883B	5962-8776302LX	12-Bit Dual Multiplying DAC*
AD7537UE/883B	5962-87763033X	12-Bit Dual Multiplying DAC*
AD7537UQ/883B	5962-8776303LX	12-Bit Dual Multiplying DAC*
AD7545GUE/883B	5962-87702042X	12-Bit Multiplying DAC*
AD7545GUQ/883B	5962-8770204RX	12-Bit Multiplying DAC*
AD7545SE/883B	5962-87702012X	12-Bit Multiplying DAC*
AD7545SQ/883B	5962-8770201RX	12-Bit Multiplying DAC*
AD7545TE/883B	5962-87702022X	12-Bit Multiplying DAC*
AD7545TQ/883B	5962-8770202RX	12-Bit Multiplying DAC*
AD7545UE/883B	5962-87702032X	12-Bit Multiplying DAC*
AD7545UQ/883B	5962-8770203RX	12-Bit Multiplying DAC*
AD7547SQ/883B	5962-8965701LX**	12-Bit Dual Multiplying DAC*
AD7547TQ/883B	5962-8965702LX**	12-Bit Dual Multiplying DAC*
AD7547UQ/883B	5962-8965703LX**	12-Bit Dual Multiplying DAC*
AD7549SQ/883B	5962-8876501RX**	12-Bit Dual DAC*
AD7549TQ/883B	5962-8876502RX**	12-Bit Dual DAC*
AD767SD/883B	5962-8961701LA	12-Bit DAC**
AD7845SQ/883B	5962-8876701LX**	12-Bit V _{OUT} Multiplying DAC*
ADDAC87-CBI-V/883B	5962-8300201JC	12-Bit Hybrid DAC
ADDAC87D-CBI-V/883B	8300301JA	12-Bit Monolithic DAC

A/D CONVERTERS

Generic Part Number	SMD Part Number	Description
AD570SD/883B	5962-8680201VA	Complete, 8-Bit ADC
AD571SD/883B	5962-8680202VA	Complete, 10-Bit ADC
AD573SD/883B	5962-8850501RA	10-Bit ADC
AD574ATD/883B	5962-8512702XA	Complete, 12-Bit ADC*
AD574ATE/883B	5962-85127023C	Complete, 12-Bit ADC**
AD574AUD/883B	5962-8512701XA	Complete, 12-Bit ADC*
AD574AUE/883B	5962-85127013C	Complete, 12-Bit ADC**
AD670SD/883B	5962-8763501RA**	Signal Conditioning 8-Bit ADC
AD673SD/883B	5962-8850502RA	8-Bit ADC

*μP compatible.

**Release pending.

Generic Part Number	SMD Part Number	Description
AD674ATD/883B	5962-8861502XA**	Complete, 12-Bit ADC*
AD674ATE/883B	5962-88615023C	Complete, 12-Bit ADC**
AD674AUD/883B	5962-8861501XA**	Complete, 12-Bit ADC*
AD674AUE/883B	5962-88615013C	Complete, 12-Bit ADC**
AD7572SE05/883B	5962-87591043X	Complete, 12-Bit 5 μ s ADC*
AD7572SE12/883B	5962-87591013X	Complete, 12-Bit 12 μ s ADC*
AD7572SQ05/883B	5962-8759104LX	Complete, 12-Bit 5 μ s ADC*
AD7572SQ12/883B	5962-8759101LX	Complete, 12-Bit 12 μ s ADC*
AD7572TE05/883B	5962-87591053X	Complete, 12-Bit 5 μ s ADC*
AD7572TE12/883B	5962-87591023X	Complete, 12-Bit 12 μ s ADC*
AD7572TQ05/883B	5962-8759105LX	Complete, 12-Bit 5 μ s ADC*
AD7572TQ12/883B	5962-8759102LX	Complete, 12-Bit 12 μ s ADC*
AD7572UE05/883B	5962-87591063X	Complete, 12-Bit 5 μ s ADC*
AD7572UE12/883B	5962-87591033X	Complete, 12-Bit 12 μ s ADC*
AD7572UQ05/883B	5962-8759106LX	Complete, 12-Bit 5 μ s ADC*
AD7572UQ12/883B	5962-8759103LX	Complete, 12-Bit 12 μ s ADC*
AD7574SQ/883B	5962-8961601VX**	8-Bit ADC*
AD7574TQ/883B	5962-8961602VX**	8-Bit ADC*
AD7575SE/883B	5962-87762012X	8-Bit ADC with T/H*
AD7575SQ/883B	5962-8776201VX	8-Bit ADC with T/H*
AD7575TE/883B	5962-87762022X	8-Bit ADC with T/H*
AD7575TQ/883B	5962-8776202VX	8-Bit ADC with T/H*
AD7672TQ05/883B	5962-8965503LX**	12-Bit High Speed ADC*
AD7672TQ10/883B	5962-8965501LX**	12-Bit High Speed ADC*
AD7672UQ05/883B	5962-8965504LX**	12-Bit High Speed ADC*
AD7672UQ10/883B	5962-8965502LX**	12-Bit High Speed ADC*
AD7820TE/883B	5962-88650012X**	8-Bit, 2 μ s ADC with T/H*
AD7820TQ/883B	5962-8865001RX**	8-Bit, 2 μ s ADC with T/H*
AD7820UE/883B	5962-88650022X**	8-Bit, 2 μ s ADC with T/H*
AD7820UQ/883B	5962-8865002RX**	8-Bit, 2 μ s ADC with T/H*
AD7821TQ/883B	5962-8951801RX**	8-Bit, 600 ns ADC with T/H*
AD7824TQ/883B	5962-8876401LX**	4-Channel 8-Bit ADC*
AD7824UQ/883B	5962-8876402LX**	4-Channel 8-Bit ADC*
AD7828TQ/883B	5962-8876403XX**	8-Channel 8-Bit ADC*
AD7828UQ/883B	5962-8876404XX**	8-Channel 8-Bit ADC*

ANALOG I/O

Generic Part Number	SMD Part Number	Description
AD7569SQ/883B	5962-8962901LX**	Complete 8-Bit Analog I/O System*
AD7569TQ/883B	5962-8962902LX	Complete 8-Bit Analog I/O System*

* μ P compatible.
**Release pending.

COMPARATORS

Generic Part Number	SMD Part Number	Description
AD96685TE/883B	5962-8600804EA**	Voltage Comparator
AD96685TH/883B	5962-86008042A**	Voltage Comparator
AD96685TQ/883B	5962-8600804IA**	Voltage Comparator
AD96687TE/883B	5962-7801903EA	Voltage Comparator
AD96687TQ/883B	5962-78019032A	Voltage Comparator

DIGITAL SIGNAL PROCESSORS

Generic Part Number	SMD Part Number	Description
ADSP-2100ASG/883B	5962-8773503XX	8 MHz Digital Signal μ P
ADSP-2100ATG/883B	5962-8773504XX	10 MHz Digital Signal μ P
ADSP-2100SG/883B	5962-8773501XX	6 MHz Digital Signal μ P

INSTRUMENTATION AMPS

Generic Part Number	SMD Part Number	Description
AD524SD/883B	5962-88539OIEA	Instrumentation Amp
AD625SD/883B	5962-87719OIEA	Instrumentation Amp

MULTIPLEXERS

Generic Part Number	SMD Part Number	Description
ADG508ATE/883B	77052012X**	8-Channel Analog MUX
ADG508ATQ/883B	7705201EX	8-Channel Analog MUX
ADG528ATQ/883B	5962-8768901VX	8-Channel Latched MUX

OP AMPS

Generic Part Number	SMD Part Number	Description
ADLH0032/883B	5962-80013	High Speed Op Amp
ADLH0033/883B	5962-80014	High Speed Buffer Amp
HOS-050A/883B	5962-88579	Video Op Amp
HOS-060SH/883B	5962-88579	Video Op Amp

VOLTAGE REFERENCES

Generic Part Number	SMD Part Number	Description
AD2700SD/883B	5962-8503001XC	Precision +10 V Reference
AD2700UD/883B	5962-8503002XC	Precision +10 V Reference
AD2702SD/883B	5962-8503003XC	Precision $\pm$ 10 V Reference
AD2702UD/883B	5962-8503004XC	Precision $\pm$ 10 V Reference
AD580SH/883B	5962-8686101XC	Precision +2.5 V Reference
AD580TH/883B	5962-8686102XC	Precision +2.5 V Reference
AD580UH/883B	5962-8686103XC	Precision +2.5 V Reference

* μ P compatible.

**Release pending.

Generic Part Number	SMD Part Number	Description
AD581SH/883B	5962-8688201*	+10 V Reference
AD581TH/883B	5962-8688202*	+10 V Reference
AD581UH/883B	5962-8688203*	+10 V Reference
AD586SQ/883B	5962-8982401PA	Precision +5 V Reference
AD586TQ/883B	5962-8982402PA	Precision +5 V Reference
AD587SQ/883B	5962-89822501PA	Precision +10 V Reference
AD587TQ/883B	5962-89822502PA	Precision +10 V Reference
AD587UQ/883B	5962-89822503PA	Precision +10 V Reference
AD588SD/883B	5962-8972801EA	Programmable Reference
AD588SE/883B	5962-89728012C	Programmable Reference
AD588TD/883B	5962-8972802EA	Programmable Reference
AD588TE/883B	5962-89728022C	Programmable Reference

SAMPLE-AND-HOLD AMPS

Generic Part Number	SMD Part Number	Description
AD585SE/883B	5962-87540012C	High Speed S/H Amp
AD585SQ/883B	5962-8754001CA	High Speed S/H Amp

SWITCHES

Generic Part Number	SMD Part Number	Description
ADG201ATE/883B	77053022X	Quad SPST Analog Switch
ADG201ATQ/883B	7705302EX	Quad SPST Analog Switch
ADG201HSTE/883B	5962-86716012X	Quad SPST Fast Switch
ADG201HSTQ/883B	5962-8671601EX	Quad SPST Fast Switch

TEMPERATURE TRANSDUCERS

Generic Part Number	SMD Part Number	Description
AD590JF/883B	5962-8757101XC	Temperature Transducer 1 μ A/K
AD590JH/883B	5962-8757101YC	Temperature Transducer 1 μ A/K
AD590KF/883B	5962-8757102XC	Temperature Transducer 1 μ A/K
AD590KH/883B	5962-8757102YC	Temperature Transducer 1 μ A/K
AD590LF/883B	5962-8757103XC	Temperature Transducer 1 μ A/K
AD590LH/883B	5962-8757103YC	Temperature Transducer 1 μ A/K
AD590MF/883B	5962-8757104XC	Temperature Transducer 1 μ A/K
AD590MH/883B	5962-8757104YC	Temperature Transducer 1 μ A/K

* μ P compatible.
 **Release pending.

Radiation Information on Analog Devices Products

RADTESTSM DATA SERVICE

Through directives of the U.S. Department of Defense and the Ministries of Defense of the NATO countries, all strategic and tactical weapons must now be designed to survive radiation environments consistent with their intended missions. System designers must select components that have been shown to survive the required types and levels of radiation. To aid our customers, Analog Devices, Inc. now offers the RADTESTSM data service. Through this service, customers can obtain radiation-performance information on our products, including data gathered from total-dose, dose-rate, and neutron testing. You need only to call any of our sales offices. Our sales engineers can provide this information and assist you in selecting the best product for your application. Our factory radiation-effects experts are available for consultation, if required. In addition, Analog Devices will supply a limited number of free samples of our monolithic products to customers who want to do their own radiation testing and evaluation in exchange for a report of the test results.

ANALOG DEVICES PRODUCT INFORMATION

The products and processes of Analog Devices in general are radiation tolerant. Most of our military-grade products and all of our major wafer-fabrication processes have undergone radiation testing and have passed most of the tactical-level radiation requirements of our customers. Many of the products also qualify for commercial space-system hardness levels. Analog Devices, Inc. has won several government contracts to develop radiation-hardened products and wafer processes that meet military requirements for hostile-space and strategic environments, for example for the Strategic Defense Initiative.

Table 1 lists products that have been characterized and shown to be radiation tolerant for most tactical military weapons systems. All of these products exceed a total dose of 1×10^4 Rad(Si), a dose rate of 1×10^9 RAD(Si)/sec, and a neutron fluence of 1×10^{13} neutrons/cm². The products in **boldface** exceed a total dose of 1×10^5 Rad(Si). The criteria for classifying these products is that these levels do not degrade a data sheet parameter beyond its specified value for the lowest-grade military product. We recommend that customers ask about the latest characterization results on these and other products, as we add them to our RADTESTSM data service.

Analog Devices, Inc. does not guarantee nor take responsibility for maintaining radiation-tolerance levels on any of our products. The data supplied by our RADTESTSM data service is for customer information only. For critical applications, we recommend that the customer test and evaluate the products to verify suitability for a specific application.

All wafer-fabrication, assembly, and test operations, and all design changes are carefully controlled and documented at Analog Devices. Military data sheets and drawings are under documentation control and display revision letters to indicate change status. By selecting our products that considerably exceed program radiation requirements, most customers can satisfy their radiation requirements economically. There are no additional charges for our radiation-tolerant products or for the use of our RADTESTSM data service.

A/D Converters	AD570, AD571 , AD573, AD574 , AD674, AD7572, AD7672, AD7820, AD7821
D/A Converters	AD392, AD395, AD558, AD561 , AD562 , AD563 , AD565 , AD566 , AD7225, AD7245, AD7520, AD7522, AD7528, AD7541, AD7545, AD7547
References	AD580, AD581 , AD584 , AD586 , AD588, AD589
Amplifiers	AD582 , AD585, AD840, AD841, AD842, AD846, AD847, AD9611, AD OP-27
Linear Functions	AD532, AD534 , AD536, AD538, AD539, AD9901
Temp Transducer	AD590
Digital Microprocessor	ADSP-1010A, ADSP-1016A, ADSP-2100/ADSP-2100A
Digital-to-Resolver	DRC1745, DRC1746
Resolver-to-Digital	AD2S80
Synchro-to-Digital	SDC1740, SDC1741, SDC1742
Miscellaneous	AD630, AD9500

Table 1. Products That Have Been Tested to Date and Found to Meet Most Tactical Weapons Radiation Requirements (See Text for Levels)

RADIATION-TOLERANT TECHNOLOGY AT ANALOG DEVICES

Analog Devices products exhibit a high tolerance for radiation across a variety of wafer-fabrication and design technologies. There are many reasons for this. Primarily, we have two decades of experience using proprietary thin-film resistor material to implement precision circuit elements in our monolithic converters and linear products. This very thin, silicon-based, amorphous material is essentially radiation insensitive and has never been identified as a factor contributing to the radiation degradation of our products. This material, when properly laser trimmed, is the key to achieving the precision of our products. Table 2 shows the radiation tolerance of our major manufacturing process technologies.

In general, our Bipolar Processes show a high degree of radiation tolerance, particularly to total dose. This is because our critical bipolar circuit elements are vertical, highly-doped structures and, as such, do not have the sensitivity of MOSFET devices to threshold shifts caused by radiation-induced trapped ionizing charges at the Si-SiO₂ interface. Field-inversion reduction from trapped charges is also reduced because of the higher doping levels in bipolar circuits. Latch-up typically is not a problem for several reasons: the lower substrate resistivity with epi, the use of buried layers, and the conservative layout rules used on these typically low-device-count products. Even though photo currents are high, they generally do not cause device destruction in these high-speed products because the metal bus lines are wide enough to handle such currents and the rad-hard, thin-film resistors act as effective current limiters. Finally neutron tolerance is high because of the high f_T (thin base regions) of the bipolar devices used in these circuits. This is particularly true for our complementary bipolar, trench, and flash processes. The trench process has very high radiation tolerance because of the device-to-device isolation provided by both the sidewall dielectric isolation and the epi-well bottom.

Many of our products made on BiMOS and LC²MOS processes meet minimum tactical-weapons radiation requirements, even though they are somewhat lower in resistance to total-dose radiation than our bipolar processes. This lowered tolerance is the result of combining high-temperature bipolar and JFET process steps with the CMOS process. In the case of the Advanced Bipolar CMOS (ABCMOS) process, this problem is being addressed, with significant improvements evident. Dose-rate tolerance for all three processes is enhanced by utilizing conservative layouts and epi substrates to address the latch-up problem and by laying out wide metal bus lines, which reduce photo-current-induced burnout. The neutron tolerance is extremely high for these three processes, since the bipolar circuit elements have thin base regions, and the MOSFET surface-effect devices are insensitive to bulk damage induced by neutron bombardment.

Our high-density DSP CMOS process has a particularly high total-dose tolerance, exceeding 100k Rads(Si) on such products as the ADSP-2100. This is because of the fortuitous commonality of the process techniques required both to achieve a high-speed, 1.0 μm CMOS source-drain spacing and to minimize radiation-charge trapping in MOS gate and field oxides.

Analog Devices products generally are not sensitive to the single-event upset (SEU) problem. First, there are no sensitive memory elements on our linear products to be upset by SEU-induced substrate charges. In addition, our products are relatively low-current integrated circuits, and the active devices, when driven by SEU-induced photon currents, saturate at a current level that typically cannot fuse the metal interconnect lines. Finally, the latch-up problem associated with SEU is typically not a problem for the reasons already stated.

Wafer Process	Total Dose (RAD-Si)	Dose Rate (RAD-Si/Sec)	Neutron (N/cm ²)
Bipolar I	3E5	1E10	7E12
Bipolar II	3E5	1E10	2E12
Bipolar III	3E5	1E10	1E12
Complementary Bipolar	1E5	9E9	2E12 (Est.)
STAT-1 (Trench)	1E6	2E10	1E13
Flash	5E5	1E9	5E12
BiMOS	1E4	5E9 (Est.)	1E13
LC ² MOS	2E4	7E9	1E13 (Est.)
ABCMOS	5E4	1E10	1E13
DSP CMOS	1E5	1E9	1E14 (Est.)

¹NOTE: Radiation Tolerance of Analog Devices Wafer Processes Based on the Highest Radiation Level that the Products Survive and Still Meet Lowest-Grade Data Sheet Parameters. Since Dose Rate Is Particularly Dependent on Circuit Design and Layout, the Levels Shown Do Not Necessarily Reflect Process Capability Alone.

Table 2. Radiation Tolerance of Analog Devices Processes

Monolithic Circuits

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General Specification	31
Detailed Specifications	35

General Specification Monolithic Circuits

ADI-M-1000

1.0 SCOPE

1.1 Scope.

This specification covers the general requirements for monolithic microcircuits. Specific microcircuit requirements are in the device specification.

1.2 Part Number.

The complete part number is per paragraph 1.2 of the device specification.

1.2.1 Device Type.

The device type and electrical grade selections are per the device specification.

1.2.2 Device Class.

The device conforms to product assurance level Class B per MIL-M-38510.

1.2.3 Case Outline.

The case outline is per paragraph 1.2.3 of the device specification.

1.3 Absolute Maximum Ratings.

Absolute maximum ratings are per paragraph 1.3 of the device specification.

1.3.1 Recommended Operating Conditions.

1.4 Electrostatic Discharge (ESD) Damage.

ESD damage may occur to devices subjected to high energy electrostatic fields.

1.5 Thermal Characteristics.

Maximum temperature rise from junction to case and from junction to ambient are per paragraph 1.5 of the device specification.

2.0 APPLICABLE DOCUMENTS

2.1 Issues of Documents.

The following documents of the issue in effect on the date of product seal, form a part of this specification to the extent specified herein.

MILITARY SPECIFICATION

MIL-M-38510 – Microcircuits, General Requirements for.

MILITARY STANDARD

MIL-STD-883 – Test Methods and Procedures for Microelectronics.

2.2 Order of Precedence.

In the event of a conflict between the text of this specification, the device specification and the references cited herein, the order of precedence shall be as follows:

Device Specification
General Specification
MIL-M-38510

REV. C

3.0 REQUIREMENTS

3.1 Item Requirements.

The individual item requirements are per the device specification.

3.2 Design and Construction.

The design and construction are per paragraph 3.5 of MIL-M-38510.

3.2.1 Circuit Diagram and Terminal Connections.

The circuit functional block diagram and terminal connections are per the device specification.

3.2.2 Schematic Circuit.

The schematic circuit is available for on-site review upon customer's request.

3.2.3 Case Outline.

The case outline is per paragraph 1.2.3 of the device specification.

3.2.4 Microelectronic Group Assignments.

Technology groups are per Appendix E of MIL-M-38510 and are per paragraph 3.2.4 of the device specification.

3.3 Lead Material and Finish.

Lead material and finish are per MIL-M-38510 per paragraph 3.5.6.

3.4 Electrical Performance Characteristics.

The electrical performance characteristics are per Table 1 of the device specification.

3.5 Electrical Test Requirements.

The electrical test requirements are per Table 1 below, and per the device specifications.

MIL-STD-883 TEST REQUIREMENTS	Subgroups
Interim Electrical Parameters (Pre-Burn-In) (Method 5004)	1
Final Electrical Test Parameters (Method 5004)	1*, 2, 3, 4, 5, 6
Group A Test Requirements (Method 5005)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Groups C & D End Point Electrical Test (Method 5005)	1

*PDA applies to subgroup 1 (see paragraph 4.2.1.b) of this specification.

Table 1. Electrical Test Requirements

Electrical testing in the following subgroups is performed as a minimum per the device specification unless otherwise noted.

Subgroup 1	Static Tests @ +25°C
Subgroup 2	Static Tests @ +125°C
Subgroup 3	Static Tests @ -55°C
Subgroup 4	Dynamic and/or Grading and Selection Tests @ +25°C
Subgroup 5	Dynamic and/or Grading and Selection Tests @ +125°C
Subgroup 6	Dynamic and/or Grading and Selection Tests @ -55°C
Subgroup 7	Sample Tests at +25°C

ADI-M-1000

Subgroup 8	Sample Tests at -55°C and $+125^{\circ}\text{C}$
Subgroup 9	Switching Tests @ $+25^{\circ}\text{C}$
Subgroup 10	Switching Tests @ $+125^{\circ}\text{C}$
Subgroup 11	Switching Tests @ -55°C

3.6 Marking.

Each microcircuit is permanently and legibly marked per: MIL-STD-883 paragraph 1.2.1.1 and paragraph 1.2 of the device specification.

3.6.1 Date Code.

The date code is per paragraph 3.6.3 of MIL-M-38510.

3.6.2 Country of Origin Cross Reference.

The following numeric codes may be substituted for the actual country of origin marking.

Country	Code
Philippines	07 XXXX
Taiwan	10 XXXX
USA	49 XXXX
USA	50 XXXX
Ireland	No code used. Devices marked "Ireland"

3.7 Certificate of Conformance.

A Certificate of Conformance will be provided with each shipment of microcircuits per paragraph 1.2.1 of MIL-STD-883.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Sampling and Inspection.

Sampling and inspection procedures are per Appendix B of MIL-M-38510 and Method 5005 of MIL-STD-883.

4.2 Screening.

Screening is per Method 5004 of MIL-STD-883 for Class B devices and is conducted on all devices prior to shipment. The following additional criteria are applicable:

4.2.1 Burn-In.

Burn-In is per Method 1015 of MIL-STD-883.

- The burn-in circuit is per paragraph 4.2.1 of the device specification.
- Percent Defective Allowable (PDA) is 5% for failures from final electrical test, subgroup 1.

4.3 Quality Conformance Inspection.

Quality conformance inspection is in accordance with paragraph 1.2.1 of MIL-STD-883.

4.4 Data Recording.

Data recording is per paragraph 4.8 of MIL-M-38510.

4.5 Change Notification.

The detail specification and this specification will be maintained under revision control. To determine the current revision status, contact the factory.

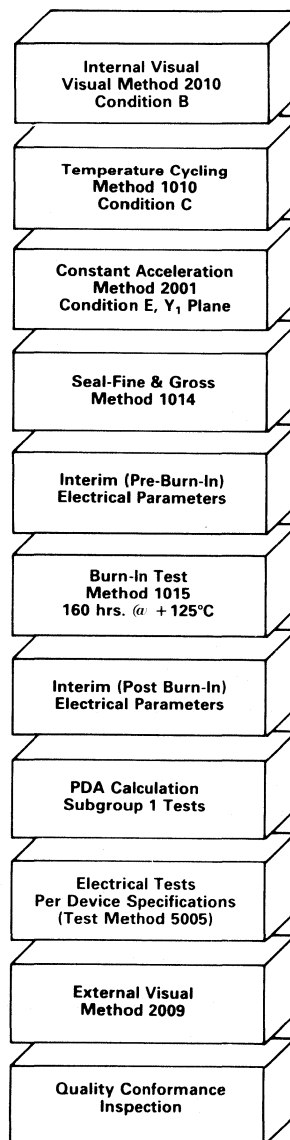
REV. C

5.0 PACKAGING

5.1 Packaging Requirements.

The packaging requirements are per MIL-M-38510. Devices are packaged in conductive foam, tubes or shunts.

MONOLITHIC PROCESS FLOW MIL-STD-883 METHOD 5004 CLASS B DEVICE



6.0 OTHER

1.1 Scope.

This specification covers the detail requirements for a high speed, high slew rate, fast-settling monolithic amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD509SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 20\text{V}$
Internal Power Dissipation ¹	300mW
Differential Input Voltage	$\pm 15\text{V}$
Common-Mode Range ($T_{\min}$ to $T_{\max}$)	$\pm 10\text{V}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Package Type	80°C	7.1mW/°C
TO-99		

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

AD509 – SPECIFICATIONS

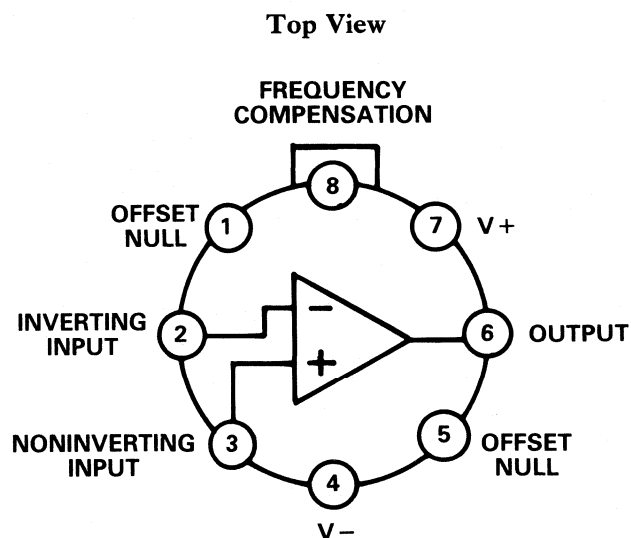
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	10	10	7.5		V _O = ±10V R _L ≥ 2kΩ	V/mV min
Gain Bandwidth Product	GBW	– 1	20					MHz min
Full Power Bandwidth	FBW	– 1	1.5					MHz min
Rise Time	t _R	– 1	25					ns max
Slew Rate	t _{SR}	– 1	100			100	R _L = 2kΩ, V _O = ±5V, C _L = 50pF	V/μs min
Settling Time	t _{SL}	– 1	0.5				To 0.1%	μs max
			2.5				To 0.01%	
Output Voltage Swing	V _{OUT}	– 1	10	10	10		R _L ≥ 2kΩ	± V min
Output Short Circuit Current	I _{SC}	– 1	50					+ mA max
Input Offset Voltage	V _{OS}	– 1	8	8	11			± mV max
Input Offset Drift Voltage	T _C V _{OS}	– 1	30		30			± μV/°C max
Input Offset Current	I _{OS}	– 1	25	25	50			± nA max
Input Bias Current	I _B	– 1	200	200	400			± nA max
Input Resistance Differential	R _{DIFF}	– 1	50					MΩ min
Common-Mode Rejection Ratio	CMRR	– 1	80	80	80		V _{CM} = ±5V	dB min
Differential Input Voltage	V _{DIFF}	– 1	15					± V max
Common-Mode Voltage Range	CMVR	– 1	10					± V min
Input Noise Voltage Density	E _N	– 1	100 30				f = 10Hz f = 100Hz f = 100kHz	nV/√Hz max
Power Supply Current	I _Q	– 1	6	6				mA max
Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max

NOTE

¹T_A = +25°C, V_S = ±15V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

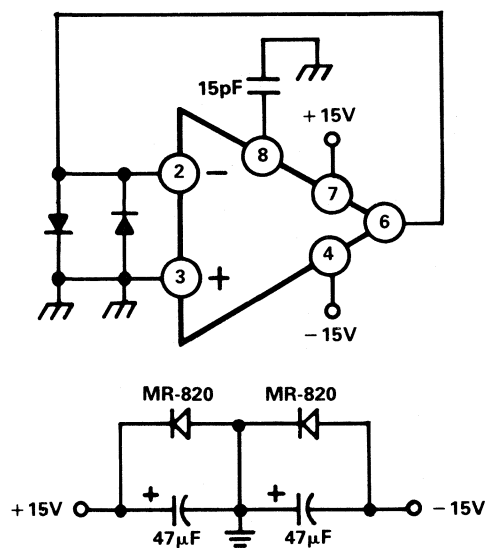


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTES

1. $I_s = 6mA$ MAX/DEVICE.
2. DEVICES ARE IN CARRIERS.

1.1 Scope.

This specification covers the detail requirements for a precision laser-trimmed, high accuracy, low drift amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD510SH/883B

1.2.3 Case Outline.

See Appendix 1, of General Specification ADI-M-1000: package outline: H-08A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 22\text{V}$
Input Voltage	$\pm 22\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$

AD510 – SPECIFICATIONS

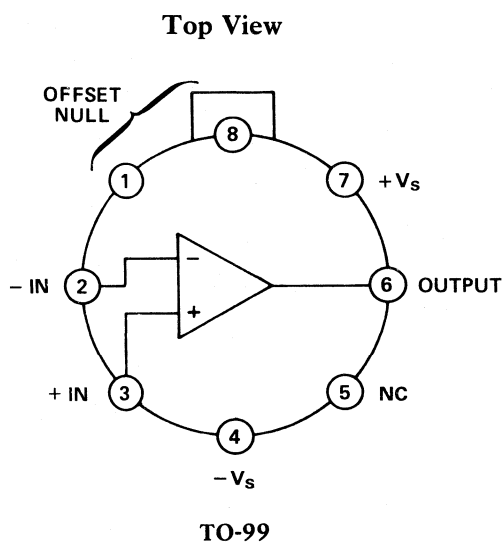
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	1000	1000	250		V _{OUT} = ± 10V	V/mV min
Output Voltage Swing	V _{OUT}	– 1	10	10	10		R _L ≥ 2kΩ	± V min
Output Short Circuit Current	I _{SC}	– 1	25	38				+ mA max
Input Offset Voltage	V _{OS}	– 1	50			50		± μV max
Input Offset Drift	TC V _{OS}	– 1	1.0		1.0			± μV/°C max
Input Offset Current	I _{OS}	– 1	4.0	4.0	10			± nA max
Input Bias Current	I _B	– 1	13	13	30			± nA max
Common-Mode Rejection Ratio	CMRR	– 1	110	110	100		V _{CM} = ± 10V	dB min
Power Supply Current	I _Q	– 1	3	3				mA max
Power Supply Rejection Ratio	PSRR	– 1	10	10	20			± μV/V max

NOTE

¹T_A = +25°C, V_S = ± 15V, unless otherwise noted.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

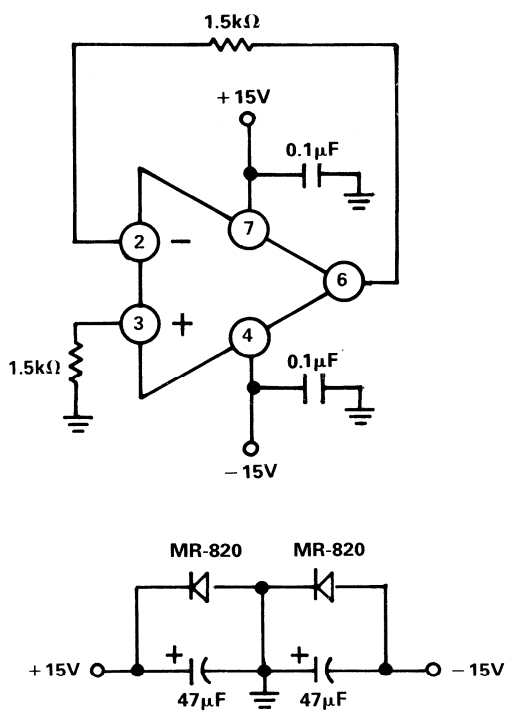


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for an ultralow drift monolithic operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD517SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08B.

1.3 Absolute Maximum Ratings. ($T_A = +25^{\circ}\text{C}$ unless otherwise stated)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm V_S$
Common-Mode Voltage Range	$\pm 10\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^{\circ}\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT	DERATE ABOVE MAXIMUM
Package Type	Temperature for Rating	Ambient Temperature
TO-99	80°C	7.1mW/°C

1.5 Thermal Characteristics.

Thermal Resistance = $\theta_{JC} = 65^{\circ}\text{C/W}$
 $\theta_{JA} = 150^{\circ}\text{C/W}$

AD517 – SPECIFICATIONS

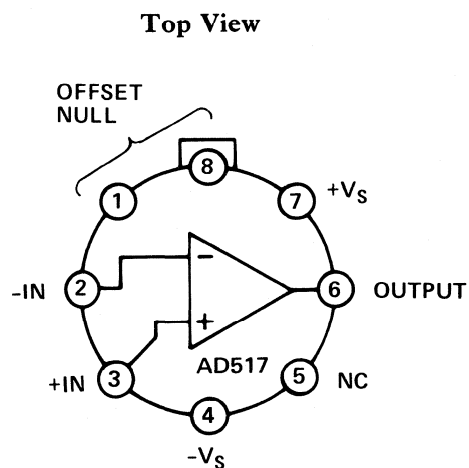
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	1000	1000	250		V _{OUT} = ± 10V, R _L ≥ 2kΩ	V/mV min
Gain Bandwidth Product	GBW	– 1	250					kHz min
Slew Rate, Unity Gain	t _{SR}	– 1	0.10					± V/μs min
Output Voltage Swing	V _{OUT}	– 1	10	10	10		R _L = 2kΩ	± V min
Output Short Circuit Current	I _{SC}	– 1	25	38				mA max
Input Offset Voltage	V _{OS}	– 1	75			75		± μV max
Input Offset Drift	TC V _{OS}	– 1	1.8		1.8			± μV/°C max
Input Bias Current	I _B	– 1	2.0	2.0	10			± nA max
Input Offset Current	I _{OS}	– 1	2.0	2.0	10.0			± nA max
Differential Input Voltage	V _{DIFF}	– 1	15					± V
Common-Mode Rejection Ratio	CMRR	– 1	110	110	100		V _{IN} = ± 10V	dB min
Input Noise Voltage Density	E _N	– 1	20				f = 1kHz	nV/√Hz
Input Noise Voltage	e _n	– 1	2				f = 0.1 to 10Hz	μV p-p
Power Supply Current	I _Q	– 1	3	3				mA max
Power Supply Rejection Ratio	PSRR	– 1	10	10	20			± μV/V max

NOTE

¹T_A = +25°C, V_S = ± 15V unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

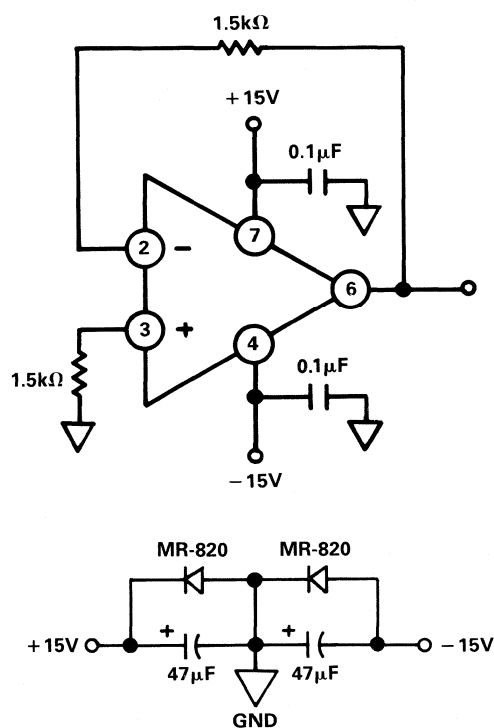


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for an accurately programmable gain instrumentation amplifier. The gain is $G = \frac{R_S}{R_G} \frac{V}{V}$.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD521SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-14.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT	DERATE ABOVE MAXIMUM
Package Type	Temperature for Rating	Ambient Temperature
D-14	$+80^\circ\text{C}$	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C}/\text{W}$
 $\theta_{JA} = 95^\circ\text{C}/\text{W}$

AD521 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Input Offset Voltage	V _{OSI}	– 1	1.5	1.5				± mV max
Input Offset Voltage Drift	TCV _{OSI}	– 1	5		5			± µV/°C max
Output Offset Voltage	V _{OSO}	– 1	200	200				± mV max
Output Offset Voltage Drift	TCV _{OSO}	– 1	150		150			± µV/°C max
Input Offset Current	I _{OS}	– 1	10	10				± nA max
Input Offset Current Drift	TCI _{OS}	– 1	125		125			± pA/°C max
Input Bias Current	I _B	– 1	40	40				± nA max
Input Bias Current Drift	TCI _B	– 1	500		500			± pA/°C max
Quiescent Supply Current	I _{CC}	– 1	5					± mA max
Gain Nonlinearity	GN	– 1	0.2	0.2			1 < G < 1000 V _{OUT} = ± 10V	± % max
Common-Mode Rejection Ratio	CMRR ₁	– 1	74	74			G = 1; dc, 1k Source Imbalance	dB min
Common-Mode Rejection Ratio	CMRR ₁₀	– 1	94				G = 10; dc, 1k Source Imbalance	dB min
Common-Mode Rejection Ratio	CMRR ₁₀₀	– 1	104				G = 100; dc, 1k Source Imbalance	dB min
Common-Mode Rejection Ratio	CMRR ₁₀₀₀	– 1	110	110			G = 1000; dc, 1k Source Imbalance	dB min
Output Voltage Swing	V _{OUT}	– 1	10	10			R _L = 1kΩ	± V min

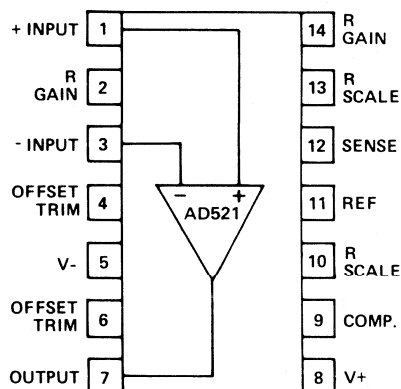
NOTE

¹V_S = ± 15V, R_L = 1kΩ at T_A = + 25°C unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

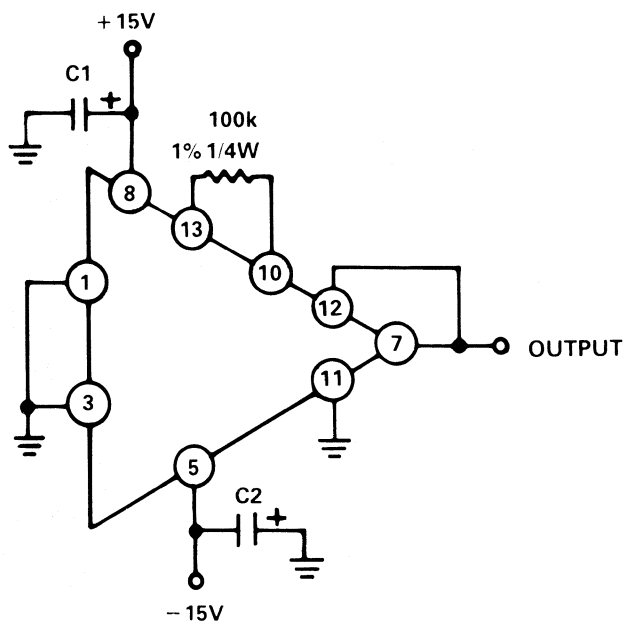


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high accuracy, pin-programmable, precision monolithic instrumentation amplifier. The AD524 doesn't require any external components for fixed gains of 1, 10, 100 and 1000. For other gain settings only a single resistor is required.

The gain equation is: $\frac{40,000}{RG} + 1 \pm 20\%$ with external resistor gain programming.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD524S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-16	16-Pin Side Brazed
E	E-20A	20 Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	± 18V
Internal Power Dissipation	280mW
Rated Operating Temperature Range	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= 22°C/W for D-16
θ_{JA}	= 95°C/W for D-16
θ_{JC}	= 25°C/W for E-20A
θ_{JA}	= 150°C/W for E-20A

AD524 – SPECIFICATIONS

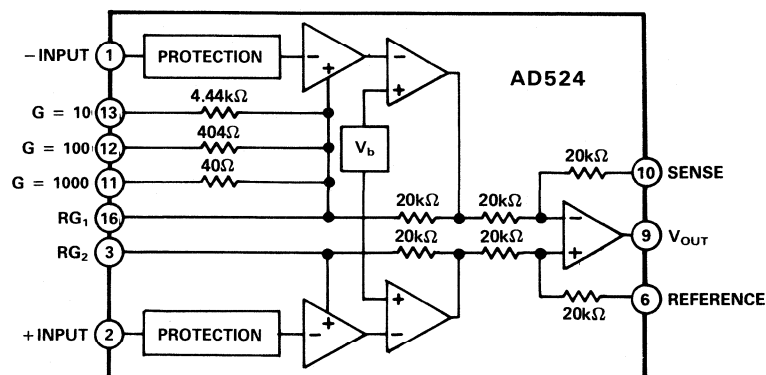
Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Gain Error 1	GE ₁	– 1	0.05	0.05		G = 1, V _O = ± 10V	± % max
Gain Error 10	GE ₁₀	– 1	0.25	0.25		G = 10, V _O = ± 10V	± % max
Gain Error 100	GE ₁₀₀	– 1	0.5	0.5		G = 100, V _O = ± 10V	± % max
Gain Error 1000	GE ₁₀₀₀	– 1	2.0	2.0		G = 1000, V _O = ± 10V	± % max
Gain Error Drift	TCGE ₁	– 1	5		5	G = 1, V _O = ± 10V	± ppm/°C max
Gain Error Drift 10	TCGE ₁₀	– 1	10		10	G = 10, V _O = ± 10V	± ppm/°C max
Gain Error Drift 100	TCGE ₁₀₀	– 1	25		25	G = 100, V _O = ± 10V	± ppm/°C max
Gain Error Drift 1000	TCGE ₁₀₀₀	– 1	50		50	G = 1000, V _O = ± 10V	± ppm/°C max
Input Offset Voltage	V _{OSI}	– 1	100	100		V _{IN} = 0V	± μV max
Input Offset Voltage	TCV _{OSI}	– 1	2		2	G = 1000, V _{IN} = 0V	± μV/°C max
Output Offset Voltage	V _{OSO}	– 1	3	3		V _{IN} = 0V	± mV max
Output Offset Drift	TCV _{OSO}	– 1	50		50	G = 1, V _{IN} = 0V	± μV/°C max
Input Bias Current	I _B	– 1	50	50		G = 1	± nA max
Input Offset Current	I _{OS}	– 1	35	35		G = 1	± nA max
Common-Mode Rejection	+ CMRR ₁	– 1	70	70		G = 1, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₁	– 1	70	70		G = 1, V _{IN} = 0V to – 10V	dB min
Common-Mode Rejection	+ CMRR ₁₀	– 1	90	90		G = 10, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₁₀	– 1	90	90		G = 10, V _{IN} = 0V to – 10V	dB min
Common-Mode Rejection	+ CMRR ₁₀₀	– 1	100	100		G = 100, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₁₀₀	– 1	100	100		G = 100, V _{IN} = 0V to – 10V	dB min
Common-Mode Rejection	+ CMRR ₁₀₀₀	– 1	110	110		G = 1000, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₁₀₀₀	– 1	110	110		G = 1000, V _{IN} = 0V to – 10V	dB min
Power Supply Current	I _{CC}	– 1	5.0	5.0		G = 1	mA max
Power Supply Rejection	PSRR ₁	– 1	75	75		G = 1, V _S = ± 12V, ± 15V	dB min
Power Supply Rejection	PSRR ₁₀	– 1	95	95		G = 10, V _S = ± 12V, ± 15V	dB min
Power Supply Rejection	PSRR ₁₀₀	– 1	105	105		G = 100, V _S = ± 12V, ± 15V	dB min
Power Supply Rejection	PSRR ₁₀₀₀	– 1	110	110		G = 1000, V _S = ± 12V, ± 15V	dB min

NOTE

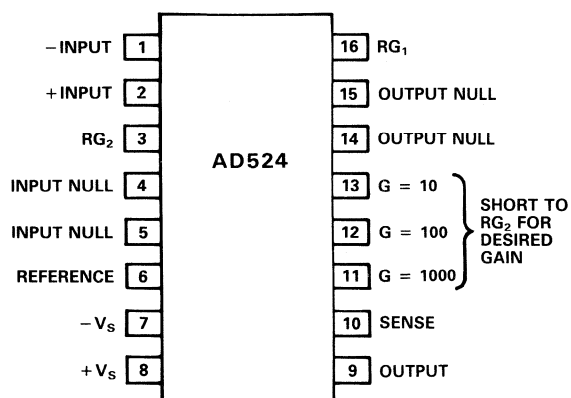
¹V_S = ± 15V, R_L = 2kΩ, unless otherwise specified.

Table 1.

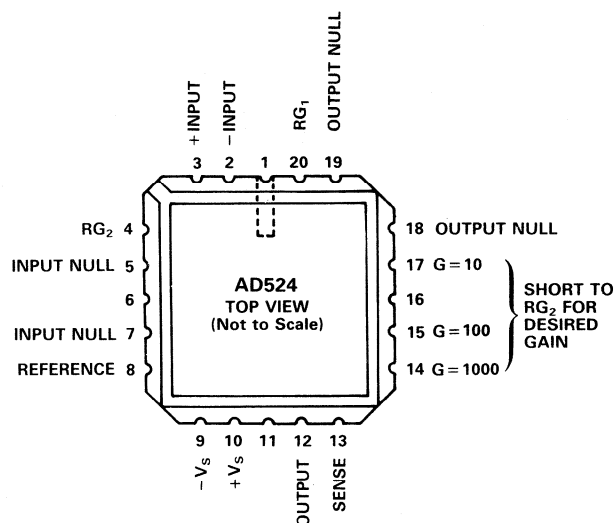
3.2.1 Functional Block Diagram and Terminal Assignments.



D Package



E Package (LCC)

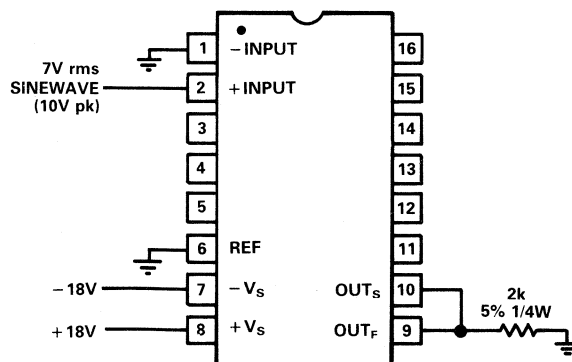


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic, laser-trimmed software programmable gain amplifier. The AD526 provides gains of 1, 2, 4, 8 and 16 depending on the digital input code.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD526SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation	1.2 Watts
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$ for D-16
 $\theta_{JA} = 95^\circ\text{C/W}$ for D-16

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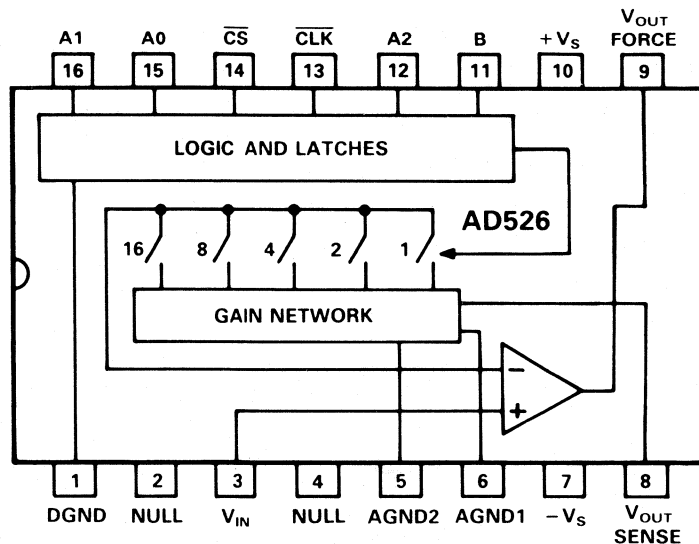
Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Gain Error 1	GE ₁	– 1	0.01	0.01	0.02	G = 1, V _{IN} = + 10V to – 10V	± % max
Gain Error 2	GE ₂	– 1	0.02	0.02	0.03	G = 2, V _{IN} = + 5 to – 5V	± % max
Gain Error 4	GE ₄	– 1	0.02	0.02	0.03	G = 4, V _{IN} = + 2.5V to – 2.5V	± % max
Gain Error 8	GE ₈	– 1	0.04	0.04	0.05	G = 8, V _{IN} = + 1.25V to – 1.25V	± % max
Gain Error 16	GE ₁₆	– 1	0.04	0.04	0.05	G = 16, V _{IN} = + 0.625V to – 0.625V	± % max
Gain Error Drift 1	TCGE ₁	– 1	2				± ppm/°C max
Gain Error Drift 2	TCGE ₂	– 1	2				± ppm/°C max
Gain Error Drift 4	TCGE ₁	– 1	3				± ppm/°C max
Gain Error Drift 8	TCGE ₈	– 1	5				± ppm/°C max
Gain Error Drift 16	TCGE ₁₆	– 1	5				± ppm/°C max
Nonlinearity 1	N ₁	– 1	0.005	0.005	0.01	G = 1, V _O = – 10V to + 10V	± FSR max
Nonlinearity 2	N ₂	– 1	0.001				± FSR max
Nonlinearity 4	N ₄	– 1	0.001				± FSR max
Nonlinearity 8	N ₈	– 1	0.001				± FSR max
Nonlinearity 16	N ₁₆	– 1	0.001				± FSR max
Input Offset Voltage	V _{OS}	– 1	0.5	0.5	0.8		± mV max
Input Offset Voltage Drift	TCV _{OS}	– 1	10				± µV/°C max
Power Supply Rejection	PSRR	– 1	84	84		V _S = 15V, ± 10%	dB min
Input Bias Current	I _B	– 1	150	150		V _{IN} = 0V, V _{IN} = 10V	± pA max
Common-Mode Voltage	CMVR	– 1	10	10			± V min
Output Voltage Swing	V _{OUT}	– 1	10	10			± V min
Short-Circuit Current	I _{SC}	– 1	15	15		G = 16, V _{IN} = 5V, V _{OUT} = 0	± mA min
Slew Rate 1, 2, 4	SR ₁	– 1	4	4		G = 1	V/µs min
Slew Rate 8, 16	SR ₈	– 1	18	18		G = 8	V/µs min
Digital Input High Voltage	V _{IH}	– 1	2				+ V min
Digital Input Low Voltage	V _{IL}	– 1	0.8				+ V max
Data Setup Time	t _{DS}	– 1	30				ns min
Data Hold Time	t _{DH}	– 1	30				ns min
Clock Pulse Width	t _C	– 1	50				ns min
+ Power Supply Current	I _{Q+}	– 1	14	14		V _{IN} = 0	mA max
– Power Supply Current	I _{Q–}	– 1	13	13		V _{IN} = 0	mA max

NOTE

¹V_S = ± 15V, unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

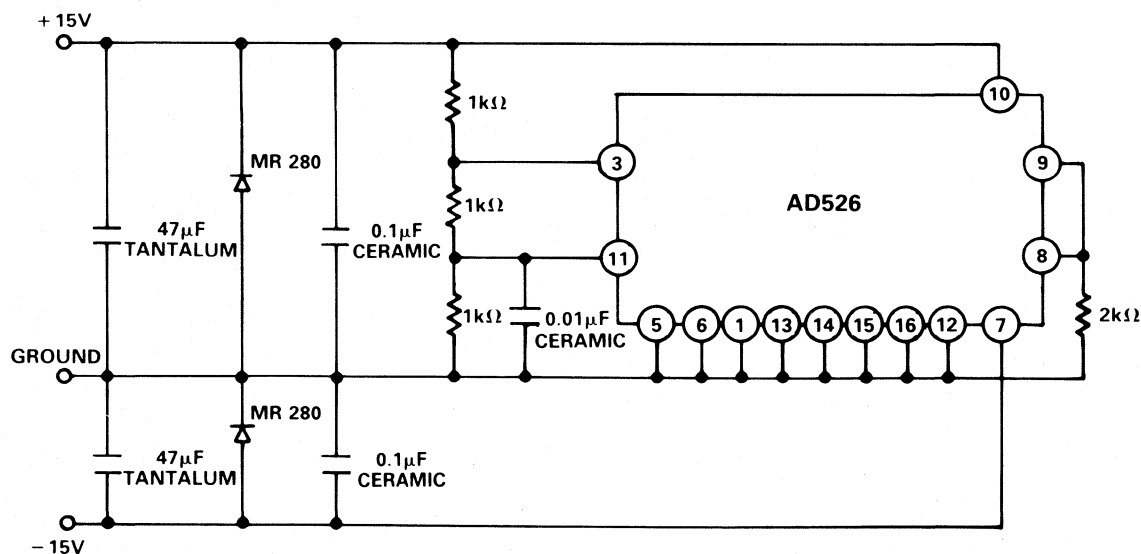


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for a laser-trimmed four-quadrant analog multiplier/divider.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD532S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-14	14-Pin DIP
H	H-10A	10-Pin Metal Package
E	E-20A	20 Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltage X_1, X_2, Y_1, Y_2	$\pm V_S$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 25^\circ\text{C/W}$ for H-10A
θ_{JA}	$= 150^\circ\text{C/W}$ for H-10A
θ_{JC}	$= 22^\circ\text{C/W}$ for D-14 or E-20A
θ_{JA}	$= 85^\circ\text{C/W}$ for D-14 or E-20A

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy ²	RA	– 1	1		4	1	$V_X = -10V, -10V, +10V, +10V$ $V_Y = -10V, +10V, -10V, +10V$	± % FS max
Multiplier Accuracy Drift	TC _{MA}	– 1	0.04		0.04			± %/°C max
Nonlinearity X Input	NL _X	– 1	1.0				$V_X = 20V$ pk-pk $V_Y = +10V$	± % FS max
Nonlinearity Y Input	NL _Y	– 1	0.6				$V_Y = 20V$ pk-pk $V_X = +10V$	± % FS max
Output Offset Voltage	V _{OS}	– 1	30		230	30	$V_X = V_Y = V_Z = 0$	± mV max
Output Offset Voltage Drift	TC V _{OS}	– 1	2		2			± mV/°C max
Input Bias Current X or Y Input	I _B	– 1	4	4				± μA max
Input Bias Current Z Input	I _B	– 1	15	15				± μA max
Input Offset Current X, Y	I _{OS}	– 1	2					± μA max
Supply Current from V _{CC}	I _{CC}	– 1	6.0	6.0			R _L = ∞	+ mA max
Supply Current from V _{EE}	I _{EE}	– 1	6.0	6.0				– mA max
Common-Mode Rejection	CMRR	– 1	50	50			$-10 \leq V_{X1} = V_{X2} \leq 10$ $V_Y = +10$ $-10 \leq V_{Y1} = V_{Y2} \leq 10$ $V_X = +10$	dB min
Output Voltage Range	V _{OUT}	– 1	10	10	10			± V min
Slew Rate	SR	– 1	25					V/μs min
1% Amplitude Error	A _E	– 1	70				$V_X = 2V$ pk-pk C _{LOAD} = 1000pF $V_Y = +10V$	kHz min
Feedthrough X	FT _X	– 1	100			100	Y Nulled, X = 20V pk-pk	± mV max
Feedthrough Y	FT _Y	– 1	80			80	X Nulled, Y = 20V pk-pk	± mV max

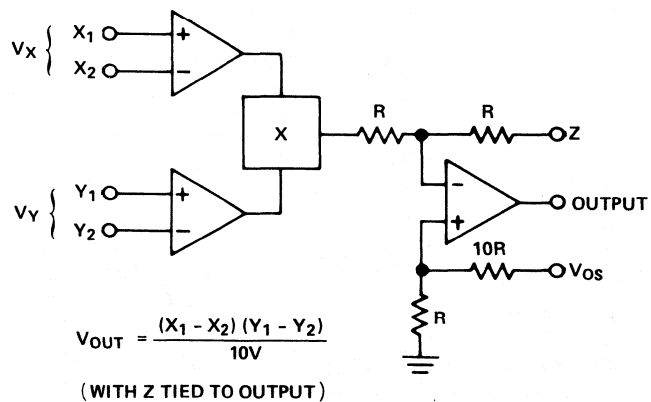
NOTES

¹T_A = +25°C, ± V_S = 15, unless otherwise noted.

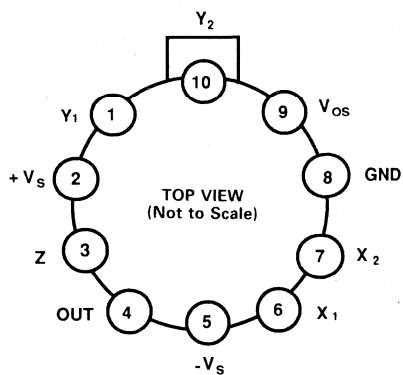
²Figures given are percent full scale, ± 10V (i.e., 0.01% = 1mV).

Table 1.

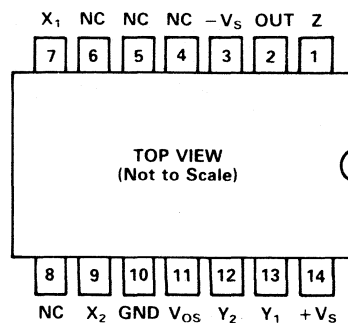
3.2.1 Functional Block Diagram and Terminal Assignments.



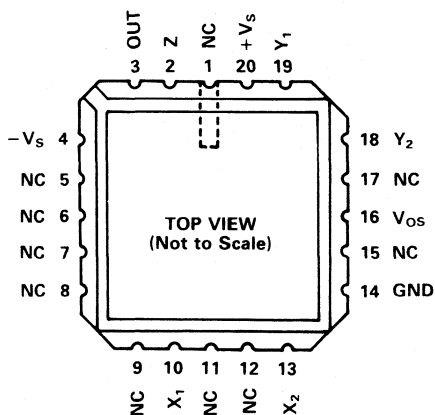
H Package



DIP Package



E Package



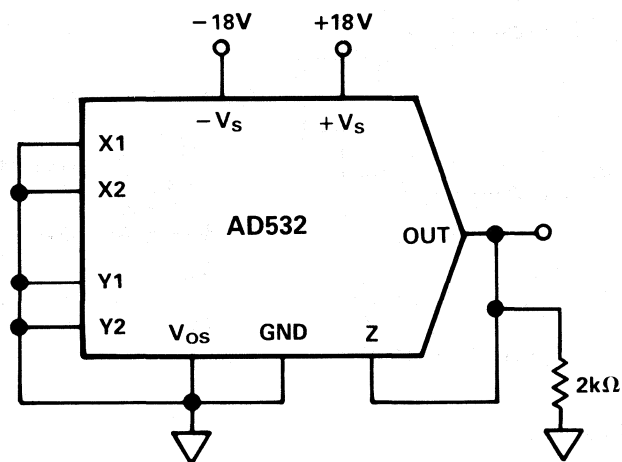
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

AD532

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for an internally trimmed precision monolithic four-quadrant analog multiplier/divider.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD534S(X)/883B
– 2	AD534T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-14	14-Pin DIP (TO-116)
H	H-10A	10-Pin Metal Package
E	E-20A	20 Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltage $X_1, X_2, Y_1, Y_2, Z_1, Z_2$	$\pm V_S$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 25^\circ\text{C/W}$ for H-10A
θ_{JA}	$= 150^\circ\text{C/W}$ for H-10A
θ_{JC}	$= 25^\circ\text{C/W}$ for D-14 or E-20A
θ_{JA}	$= 95^\circ\text{C/W}$ for D-14 or E-20A

AD534 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy ²	RA	-1	1	1	2		$V_X = -10V, -10, +10, +10$	± % FS max
		-2	0.5	1	1	0.5	$V_Y = -10V, +10V, -10, +10$	
Multiplier Accuracy Drift	TC _{MA}	-1	0.02		0.02			± %/°C max
		-2	0.01		0.01			
Nonlinearity, X Input	NL _X	-1	0.6				$V_X = 20V$ pk-pk	± % max
		-2	0.3			0.3	$V_Y = +10V$	
Nonlinearity, Y Input	NL _Y	-1	0.2				$V_Y = 20V$ pk-pk	± % max
		-2	0.10			0.10	$V_X = +10V$	
Output Offset Voltage	V _{OS}	-1	30	30	80		$V_X = V_Y = V_Z = 0V$	± mV max
		-2	15	30	45	15		
Output Offset Voltage Drift	ΔV _{OS} /ΔT	-1	500		500		$V_X = V_Y = V_Z = 0V$	± μV/°C max
		-2	300		300			
Offset Voltage (X)	V _{OSX}	-1	20	20			$V_X = V_Z = 0V$	± mV max
		-2	10	20		10	$V_Y = ±10V$	
Offset Voltage (Y)	V _{OSY}	-1	20	20			$V_Y = V_Z = 0V$	± mV max
		-2	10	20		10	$V_X = ±10V$	
Input Bias Current X, Y or Z Inputs	I _{IB}	-1, 2	2	2			$V_X = V_Y = V_Z = 0V$	± μA max
Input Offset Current X, Y or Z Inputs	I _{OS}	-1, 2	2	2			$V_X = V_Y = V_Z = 0V$	± μA max
Supply Current From V _{CC}	I _{CC}	-1, 2	6.0	6.0			R _L = No Load	+ mA max
Supply Current From V _{EE}	I _{EE}	-1, 2	6.0	6.0				- mA max
Common-Mode Rejection Ratio X, Y, or Z Inputs	CMR _X	-1	60			60	$-10V ≤ V_X ≤ +10V$	dB min
		-2	70			70	$V_Y = +10V$	
	CMR _Y	-1	60			60	$-10V ≤ V_Y ≤ +10V$	dB min
		-2	70			70	$V_X = +10V$	
Output Voltage Swing	V _{OP}	-1, 2	11	11	11			± V min
Slew Rate	SR	-1, 2	18					V/μs min
1% Amplitude Error	A _E	-1, 2	50				$V_X = 2V$ pk-pk C _{LOAD} = 1000pF, $V_Y = +10V$	kHz min
Feedthrough, X Input ³	FRR	-1	0.70				Y Nulled, X = 20V	± % FS max
		-2	0.30			0.30	pk-pk @ 50Hz	
Feedthrough, Y Input ³	FRR	-1	0.40				X Nulled, Y = 20V	± % FS max
		-2	0.10			0.10	pk-pk @ 50Hz	

NOTES

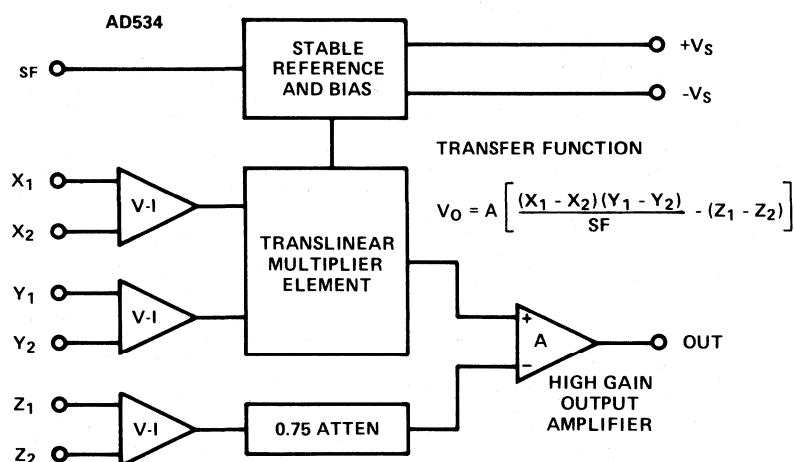
¹T_A = +25°C, V_S = ±15V, unless otherwise noted.

²Figures given are percent of full-scale; ±10V (i.e., 0.01% = 1mV).

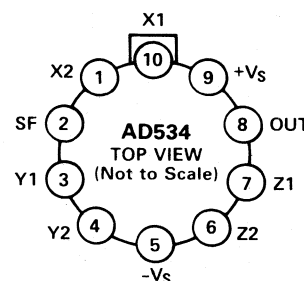
³Irreducible component due to nonlinearity: excludes effects of offsets.

Table 1.

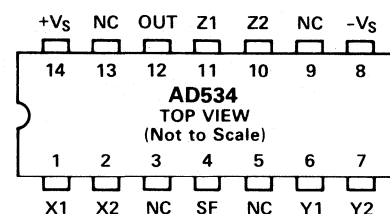
3.2.1 Functional Block Diagram and Pin Assignments.



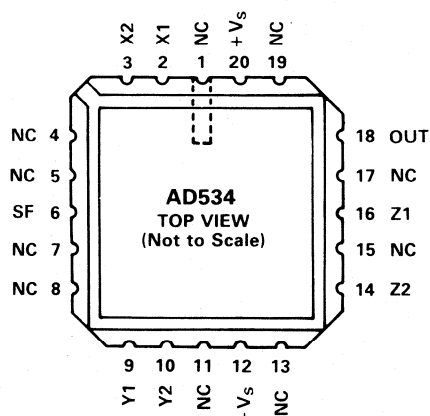
H Package



DIP Package



E Package

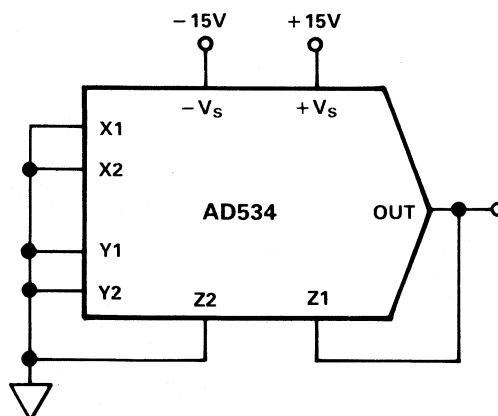


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life in per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a complete monolithic integrated circuit which performs true rms-to-dc conversion with the following transfer function:

$$V_{OUT} = \sqrt{AVG.(V_{IN})^2}$$

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD536AS(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000 package outline:

(X)	Package	Description
D	D-14	14-Pin DIP
H	H-10A	10-Pin Metal Package
E	E-20A	20-Pin Leadless Chip Carrier

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	± 18V
Input Voltage	± 25V
Internal Power Dissipation	700mW
Output Short Circuit Duration	Indefinite
Rated Operating Temperature Range	– 55°C to ± 125°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature. (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14, E-20A
θ_{JA} = 95°C/W for D-14, E-20A

AD536A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Total Error	E _T	– 1	5	5			V _{IN} = ± 300mV to ± 10V	± mV +
		– 1	0.5	0.5				± % of Reading. max
Total Error vs. Temperature 70°C to 125°C	dE _T /dT	– 1	0.3		0.3		V _{IN} = ± 300mV to ± 10V	± mV +
		– 1	0.005		0.005			± % of Reading/°C. max
Total Error vs. Temperature T _{min} to 70°C	dE _T /dT	– 1	0.1		0.1		V _{IN} = ± 300mV to ± 10V	± mV +
		– 1	0.005		0.005			± % of Reading/°C. max
Input Resistance	R _I	– 1	13.33					kΩ min to
		– 1	20.87					max
Input Offset Voltage	V _{OSI}	– 1	2					± mV max
Buffer Output Offset Voltage	V _{OSO}	– 1	2	2			I _{OUT} to BUF _{IN} , V _{IN} = 0V	± mV max
Buffer Output Offset Drift	ΔV _{OS} /ΔT	– 1	0.2		0.2		I _{OUT} to BUF _{IN} , V _{IN} = 0V	± mV/°C max
Buffer Output Voltage Swing	V _{OP}	– 1	+ 11	+ 11			I _{OUT} to BUF _{IN}	V min + Output Only
Buffer Output Current	I _{OUT}	– 1	5					mA min
Buffer Output Resistance	R _{OUT}	– 1	0.5					Ω max
dB Output Error	E _{dB}	– 1	0.6	0.6			± 7mV ≤ V _{IN} ≤ + 7V	± dB max
I _{REF} for 0dB = 1V _{rms}	I _{REF} ⁰	– 1	5	5				μA min
		– 1	80	80				to max
I _{REF} Range	I _{REF}	– 1	1					μA min to
		– 1	100					max
Buffer Input Offset Voltage	V _{OSO}	– 1	4	4			R _S = 25kΩ	± mV max
Buffer Input Bias Current	I _{IB}	– 1	60	60				nA max
Power Supply Range, Dual Supply	V _S	– 1	3					± V min to
		– 1	18	18				max
Power Supply Range, Single Supply	V _S	– 1	5					V min to
		– 1	36	36				max
Quiescent Current	I _Q	– 1	2	2	2		± 5V ≤ V _S ≤ ± 18V	mA max

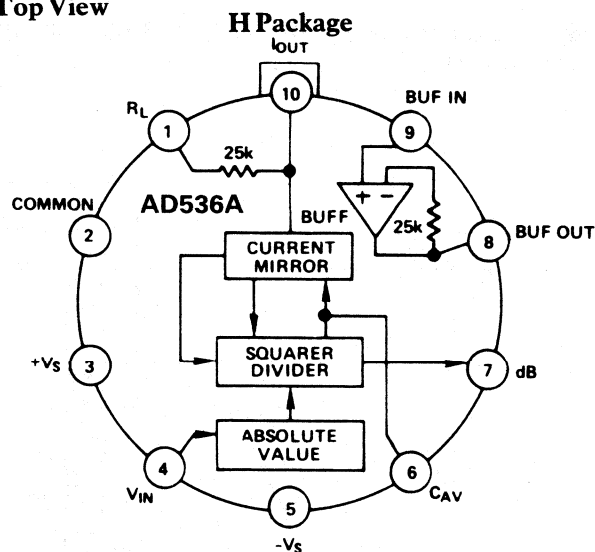
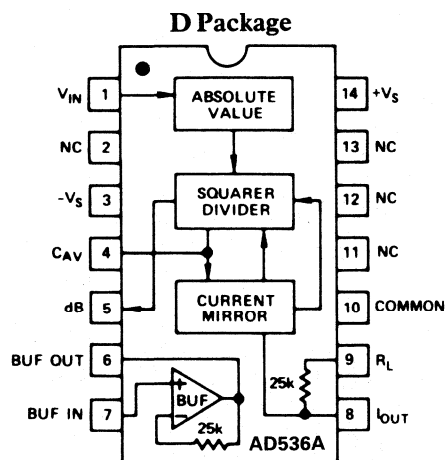
NOTE

¹T_A = +25°C and V_S = ± 15V dc, unless otherwise specified.

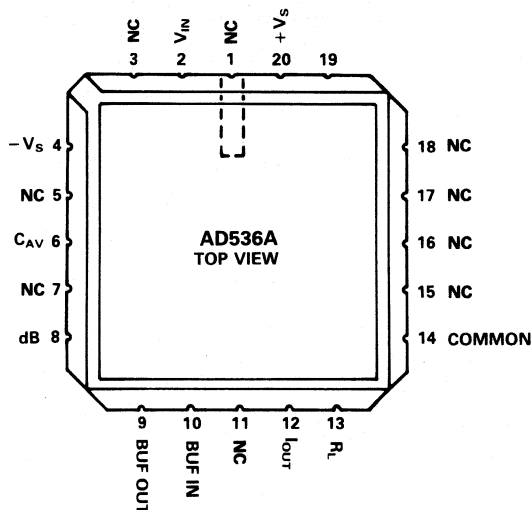
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



E Package



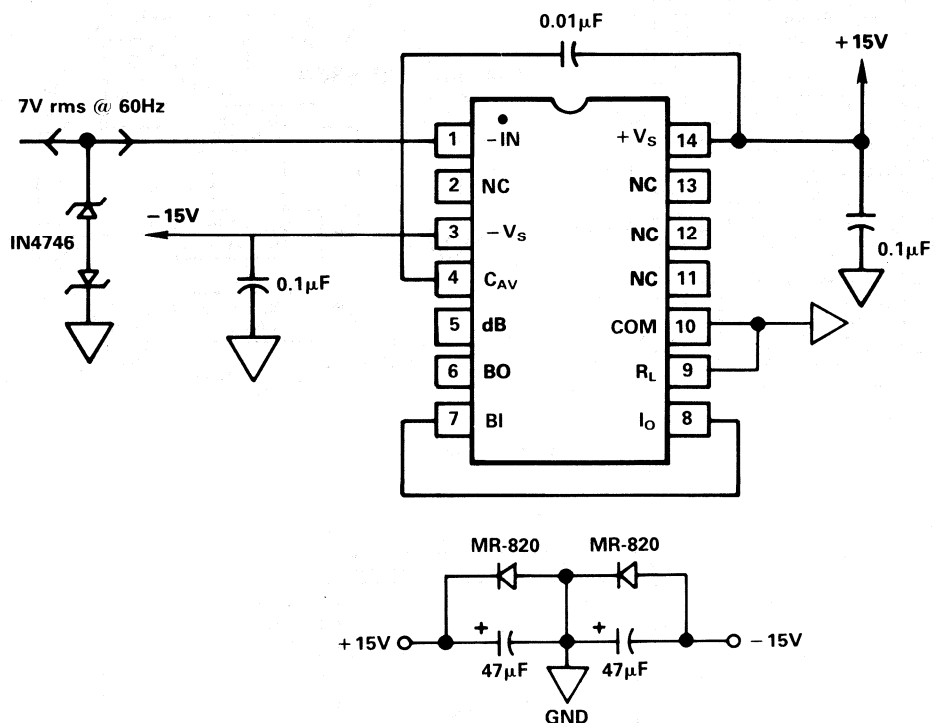
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

AD536A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a voltage-to-frequency converter with full scale range of up to 150kHz.

1.2 Part Number

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD537S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-14	14-Pin DIP
H	H-10A	10-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Voltage, Rated Performance

Single Supply	4.5V to 36V
Dual Supply	$\pm 5\text{V}$ to $\pm 18\text{V}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14
θ_{JA} = 95°C/W for D-14

AD537 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Linearity Error	LE	– 1	0.07	0.07			f = 10kHz	% max
			0.1				f = 100kHz	
Input Offset Voltage ²	V _{IO}	– 1	2	2				mV max
Offset vs. Supply	V _{OS} /V _S	– 1	100	100			15V < V _S < 20V	μV/V max
Offset Drift	ΔV _{OS} /ΔT	– 1			10		25°C to + 125°C	μV/°C max
					10		25°C to – 55°C	
Gain Error	A _E	– 1	5	5			C = 0.01μF, I _{IN} = 1.00mA	± % max
Gain vs. Supply	A _E /V _S	– 1	0.1	0.1			f = 10kHz	%/V max
Gain Drift	dA _E /dT	– 1			150		25°C to + 125°C	± ppm/°C
					150		25°C to – 55°C	max
Input Bias Current	I _{IB}	– 1	100	100				± nA max
Input Resistance	R _I	– 1	250					MΩ min
Initial Cal Temp Ref	V _{REF}	– 1	293					mV min
			303					mV max
Voltage Reference Absolute Value ³	V _{REF}	– 1	5	5				± % max
V _{REF} vs. Supply	V _{REF} /V _S	– 1	0.03	0.03			15V < V _S < 35V	%/V max
Output Leakage Current	I _{OH}	– 1	2	2	2		Logic 1	μA max
Output Voltage Logic Low	V _{OL}	– 1	0.4	0.4	0.4		I _{SINK} = 10mA	V max
Quiescent Current	I _S	– 1	2.5	2.5				mA max

NOTES

¹T_A = + 25°C, V_S = + 15V, C = 0.01μF.

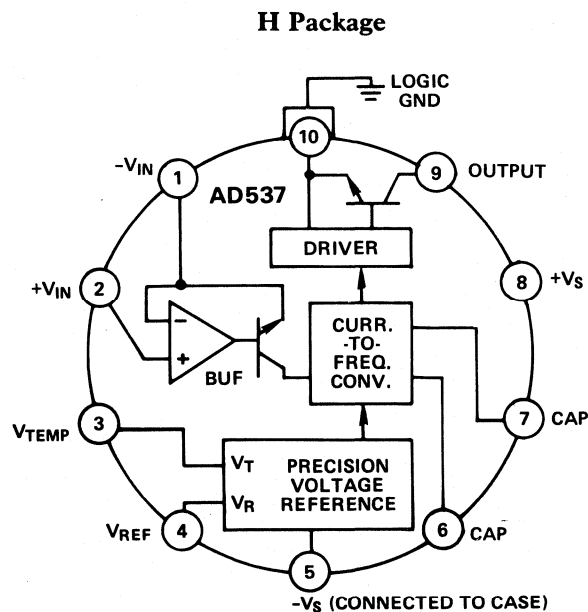
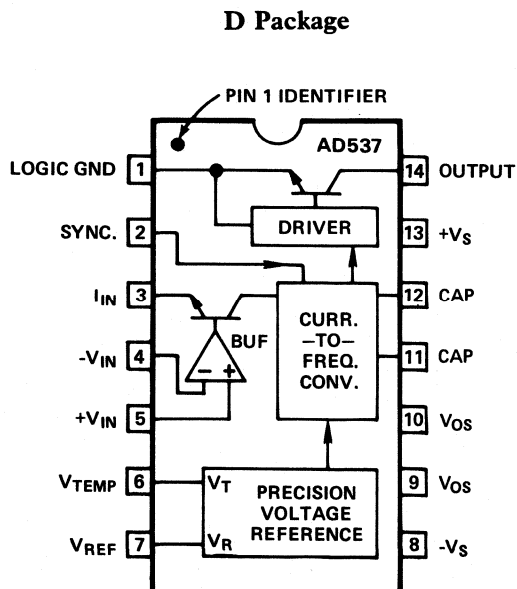
²Trimmable for D-14 package only.

³Nominal value 1.00V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

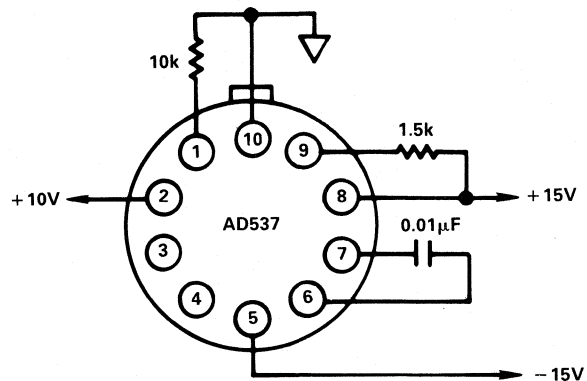
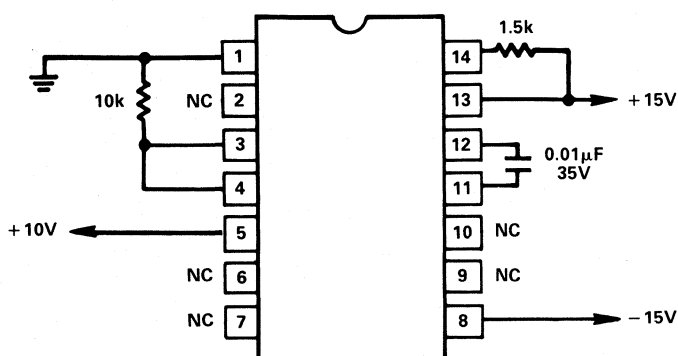


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





AD538

1.1 Scope.

This specification covers the detail requirements for a monolithic computational circuit which provides precision multiplication, division and exponentiation according to the transfer function

$$V_{OUT} = V_Y \left(\frac{V_Z}{V_X} \right)^m$$

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD538SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-18.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	± 18V
Internal Power Dissipation	250mW
Short Circuit to Ground	Indefinite
Input Voltages V _X , V _Y , V _Z	+(V _S - 1V), -1V
Input Currents I _X , I _Y , I _Z , I _O	1mA
Operating Temperature Range	- 55°C to + 125°C
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering 60sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W
θ_{JA} = 120°C/W

AD538 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Multiplier or Divider Total Error ² = E _T	E _R	- 1	1.0	1.0	2.5		100mV ≤ V _X , V _Y , V _Z ≤ 10V, m = 1.0 V _Z ≤ 10V _X	± % of Reading max
	E _O		500	500	1000			± μV max
Low Level Multiplier or Divider Total Error ³ = E _{TL}	E _{RL}	- 1	2.0	2.0	4.0		10mV ≤ V _X ≤ 10V 1mV ≤ V _Y ≤ 10V 0 ≤ V _Z ≤ 10V V _Z ≤ 10V _X m = 1.0	± % of Reading max
	E _{OL}		500	500	1000			± μV max
	E _{GL}		250	250	1000			± μV × (V _Y + V _Z)/V _X max
Output Offset Voltage	V _{OSO}	- 1	500	500	1000		V _Y = 0, Pin C = - 600mV	± μV max
Reference Accuracy	V _{REF}	- 1	50			50	V _{REF} = + 10V or + 2V	± mV max
Reference Temperature Coefficient	TCV _{REF}	- 1	50		50		V _{REF} = + 10V or + 2V	± mV max
Reference Output Current	I _{REF}	- 1	1.0	1.0			V _{REF} = + 10V or + 2V	mA max
Reference Line Regulation	VR _{LINE}	- 1	600	600			V _{REF} = + 2V ± 4.5V ≤ V _S ≤ 18V	± μV/V max
			500	500			V _{REF} = + 10V ± 13V ≤ V _S ≤ 18V	
Power Supply Rejection Ratio	PSRR	- 1	0.1	0.1			± 13.0V ≤ V _S ≤ + 17.5V	± %/V
Supply Current	I _Q	- 1	7	7				mA max

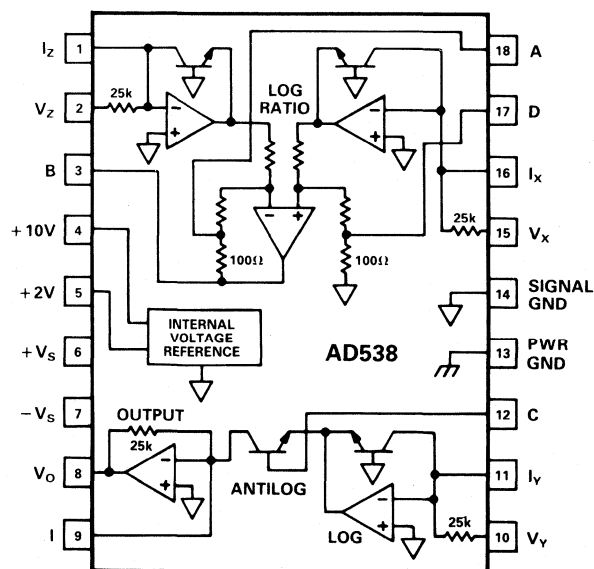
NOTES

¹ ± V_S = 15V, unless otherwise noted.

² Total error over a 100:1 input range consists of two terms; a percent of reading error E_R and an output offset voltage, E_O; where E_T = E_R + E_O.

³ Total error over the input range indicated in the test condition consists of three terms; a percent of reading error E_{RL}, an output offset error E_{OL}, and an input offset voltage multiplied by the incremental gain (V_Y + V_Z)/V_X where E_{TL} = E_{RL} + E_{OL} + E_{GL}.

3.2.1 Functional Block Diagram and Terminal Assignments.



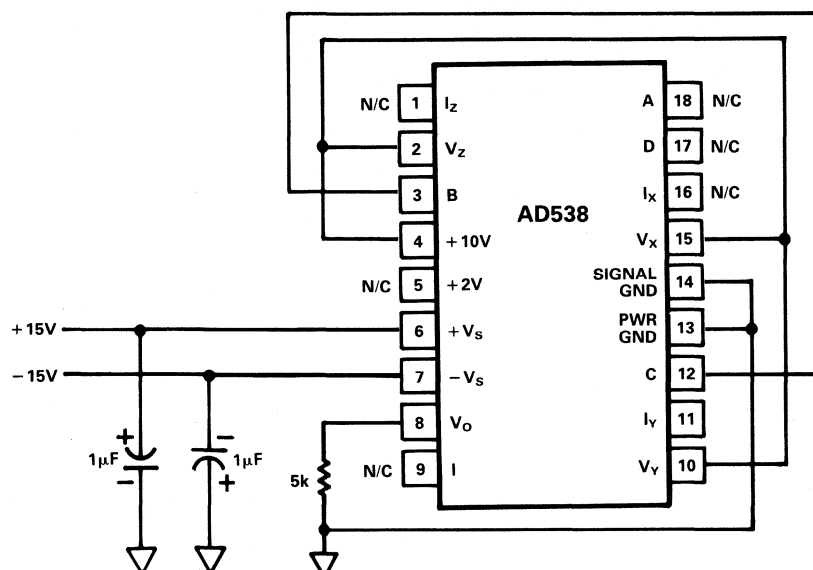
NOTE: LID IS CONNECTED TO $-V_s$

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a two quadrant wideband dual-channel linear multiplier/divider. The transfer function is: $V_{OUT} = -V_x V_y / V_q$ with a suitable external op amp.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD539SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 15\text{V}$
Internal Power Dissipation	135mW
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 25^\circ\text{C/W}$
θ_{JA}	$= 90^\circ\text{C/W}$

AD539 — SPECIFICATIONS

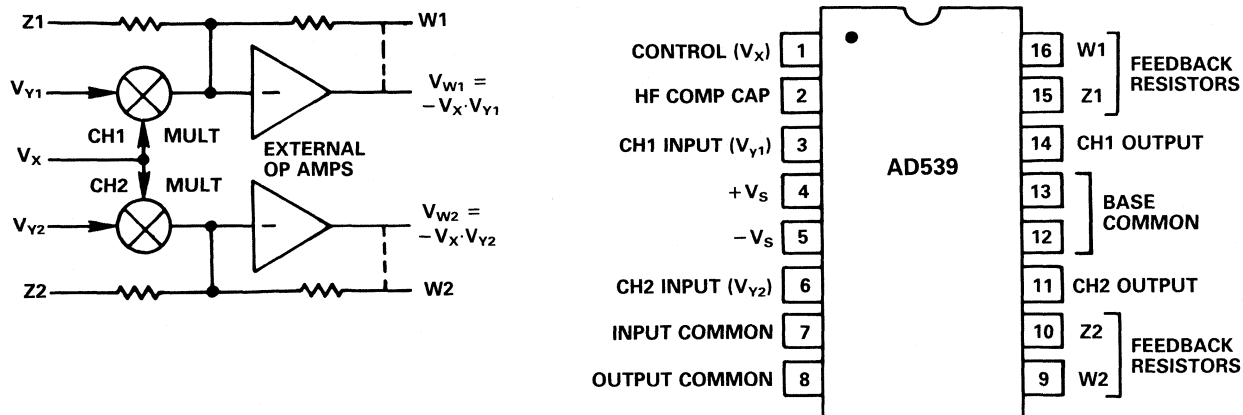
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Multiplier Scaling Voltage CH1 and CH2	V _Q	- 1	0.98	0.98	0.97			V min
			1.02	1.02	1.03			V max
Total Multiplication Error CH1 and CH2	E _T	- 1	2.5	2.5	4.0			± % of FS max
V _Y , Signal Input, Bias	I _{IB}	- 1	30	30	40			± μA max
Signal Input, Offset Voltage	V _{OSSI}	- 1	20	20	35		V _X = 3V, V _Y = 0	± mV max
V _X , Control Input, Offset Voltage	V _{OSCI}	- 1	4	4	5			± mV max
dB Gain Error CH1 and CH2	E _{dB}	- 1	0.4	0.4	0.5		V _X = 0.1 to 3V, V _Y = ± 2V	dB max
Control Feedthrough CH1 and CH2	FT _C	- 1	60	60	120		V _X = 0 to + 3V, V _Y = 0	mV max
Power Supply Range	V _S	- 1	4.5					± V min
			16.5					± V max
Quiescent Current	I _Q	- 1	10.2	10.2	11.0		V _S = ± 5V or ± 15V	mA max
	- I _Q	- 1	22.2	22.2	23.5		V _S = ± 5V or ± 15V	- mA max

NOTE

¹T_A = + 25°C and V_S = ± 5V dc, unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

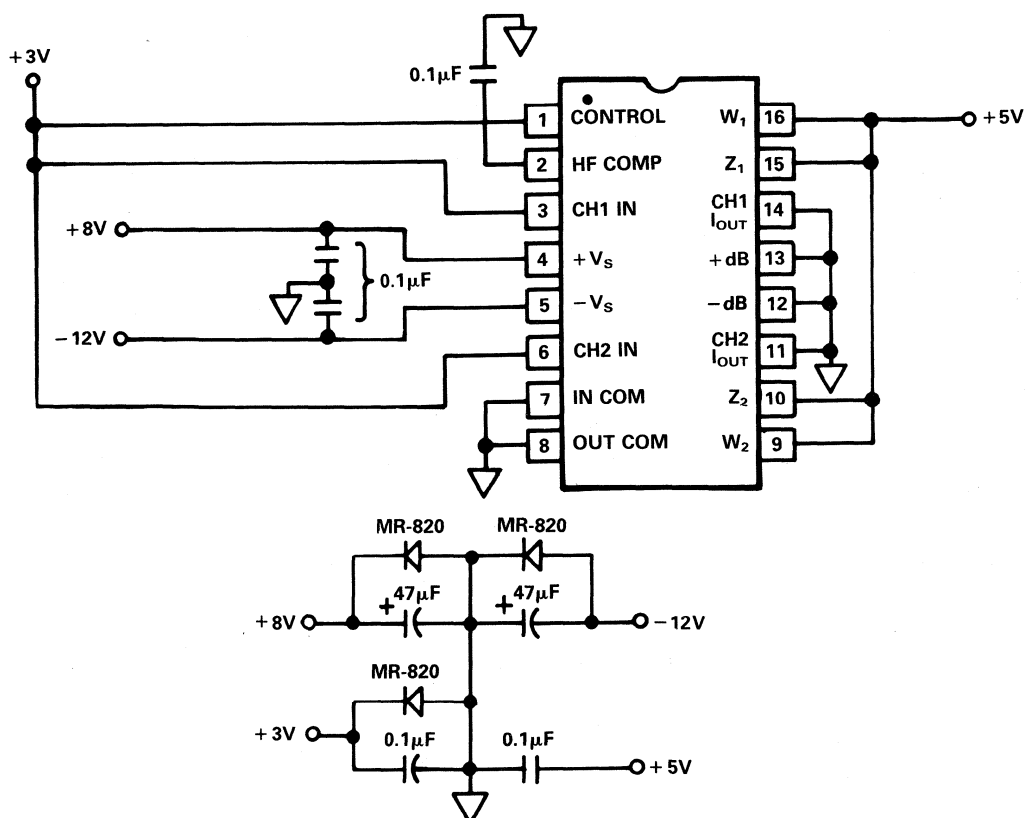


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD542SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 20\text{V}$
Common-Mode Input Voltage Range	$\pm 12\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99	80°C	7.1mW/°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

AD542 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	250	250	100		V _O = ± 10V R _L ≥ 2kΩ	V/mV min
Slew Rate	t _{SR}	– 1	3.0				Unity Gain	V/μs min
Gain Bandwidth Product	GBW	– 1	0.7					MHz min
Output Voltage Swing	V _{OUT}	– 1	10	10	10		R _L ≥ 2kΩ	± V min
			12	12	12		R _L ≥ 10kΩ	± V min
Input Offset Voltage ²	V _{OS}	– 1	1	1				± mV max
Input Offset Drift	TC V _{OS}	– 1	15		15			± μV/°C max
Input Bias Current ³	I _B	– 1	25	25				± pA max
Input Offset Current ³	I _{OS}	– 1	10	10				± pA max
Common-Mode Rejection Ratio	CMRR	– 1	80	80	80			dB min
Common-Mode Voltage Range	CMVR	– 1	10	10	10			± V min
Power Supply Current	I _Q	– 1	1.5	1.5				mA max
Power Supply Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max
Output Short Circuit Current	I _{SC}	– 1	25					mA max

NOTES

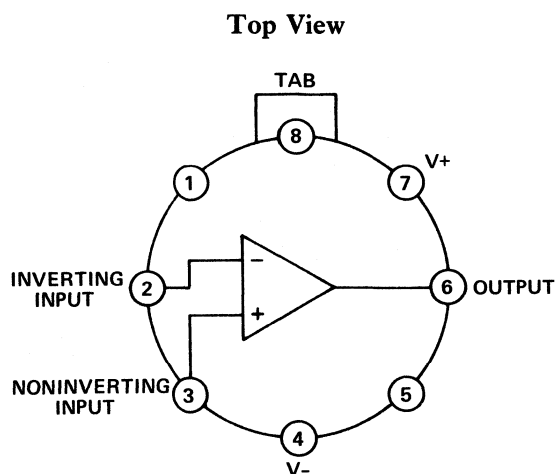
¹T_A = +25°C, V_S = ± 15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C. Nulling will induce an additional ± 3μV/°C.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C. For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

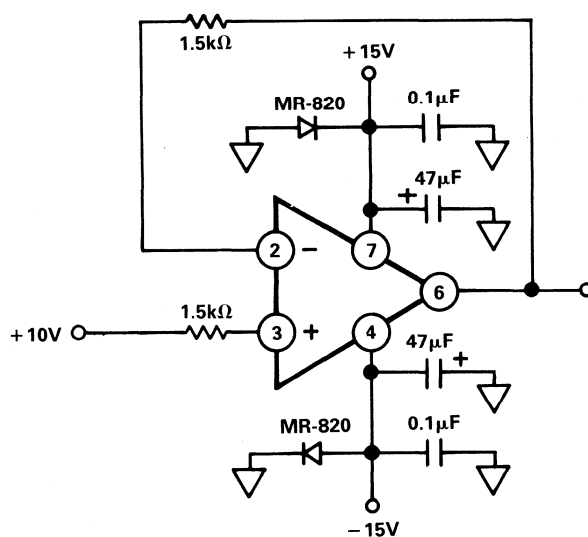


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high speed, precision, monolithic BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD544SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 20\text{V}$
Common-Mode Input Voltage Range	$\pm 12\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Package Type		
TO-99	80°C	7.1mW/°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

AD544 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	50	50	20		V _{OUT} = ± 10V, R _L ≥ 2kΩ	V/mV min
Slew Rate	t _{SR}	– 1	8	8			Unity Gain	V/μs min
Gain Bandwidth Product	GBW	– 1	1.6					MHz min
Output Voltage Swing	V _{OUT}	– 1	10	10	10		R _L ≥ 2kΩ	± V min
			12	12	12		R _L ≥ 10kV	± V min
Input Offset Voltage ²	V _{OS}	– 1	1	1				± mV max
Input Offset Voltage Drift	TC V _{OS}	– 1	15		15			± μV/°C max
Input Bias Current ³	I _B	– 1	25	25				± pA max
Input Offset Current ³	I _{OS}	– 1	15	15				± pA max
Common-Mode Rejection Ratio	CMRR	– 1	80	80	80			dB min
Common-Mode Voltage Range	CMVR	– 1	10	10	10			± V min
Power Supply Current	I _Q	– 1	2.5	2.5				mA max
Power Supply Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max
Output Short Circuit Current	I _{SC}	– 1	25					mA max

NOTES

¹T_A = +25°C, V_S = ± 15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C. Nulling will induce an additional ± 3μV/°C.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C. For temperatures above +25°C, the current doubles every 10°C.

Table 1.



Ultralow Drift BiFET Operational Amplifier

AD547

1.1 Scope.

This specification covers the detail requirements for an ultralow drift, monolithic BiFET operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD547SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 20\text{V}$
Common-Mode Input Voltage Range	$\pm 12\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$

AD547 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	— 1	250	250	100		V _O = ± 10V, R _L ≥ 2kΩ	V/mV min
Gain Bandwidth Product	GBW	— 1	0.7					MHz min
Slew Rate	t _{SR}	— 1	3.0				Unity Gain	V/μs min
Output Voltage Swing	V _{OUT}	— 1	10	10	10		R _L = 2kΩ	± V min
			12	12	12		R _L = 10kΩ	
Input Offset Voltage ²	V _{OS}	— 1	0.5	0.5				± mV max
Input Offset Drift	TC V _{OS}	— 1	5.0		5.0			± μV/°C max
Input Offset Current ³	I _{OS}	— 1	15	15				± pA max
Input Bias Current ³	I _B	— 1	25	25				± pA max
Differential Input Voltage	V _{DIFF}	— 1	20					± V
Common-Mode Rejection Ratio	CMRR	— 1	80	80	80		V _{IN} = ± 10V	dB min
Common-Mode Voltage Range	CMVR	— 1	10	10	10			± V min
Input Noise Voltage	E _{NPP}	— 1	4			4	0.1Hz to 10Hz	μV p-p max
Power Supply Current	I _Q	— 1	1.5	1.5				mA max
Power Supply Rejection Ratio	PSRR	— 1	100	100	100			± μV/V max
Output Short Circuit Current	I _{SC}	— 1	25					mA max

NOTES

¹T_A = +25°C, V_S = ± 15V unless otherwise specified.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

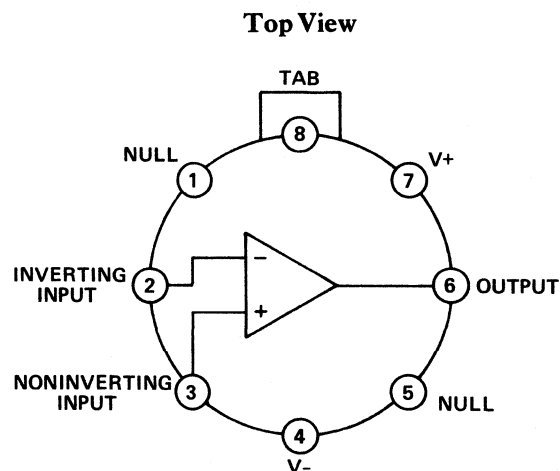
Nulling will induce an additional ± 3μV/°C.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

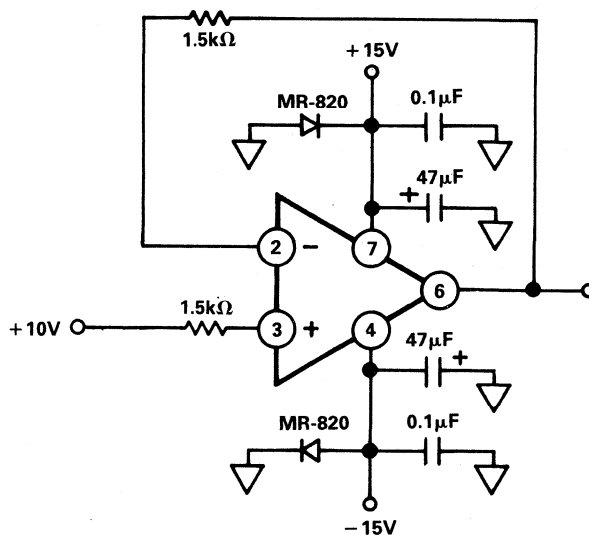


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD548S(X)/883B
- 2	AD548T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8	8-Pin Cerdip Package
H	H-08B	8-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$+V_S$ and $-V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8	75°C	$6.7\text{mW}/^\circ\text{C}$
H-08B	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8
θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08B
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08B

AD548 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	-1	2.0	2.0	3.0			± mV max
		-2	0.5	0.5	1.0			
Input Offset Voltage Drift	TCV _{OS}	-1	20		20			± μV/°C max
		-2	5		5			
Power Supply Rejection Ratio	PSRR	-1	80	80	76			dB min
		-2	86	86	80			
Input Bias Current ³	I _B	-1	20	20			Either Input, V _{CM} = 0	± pA max
		-2	10	10			Either Input, V _{CM} = 0	
		-1	30	30			Either Input, V _{CM} = +10V	± pA max
		-2	15	15			Either Input, V _{CM} = +10V	
Input Offset Current ³	I _{OS}	-1	10	10			V _{CM} = 0	± pA max
		-2	5	5			V _{CM} = 0	
Gain Bandwidth Product	GBW	-1, 2	1.0					MHz min
Slew Rate	t _{SR}	-1, 2	1.0	1.0				V/μs min
Common-Mode Voltage Range	CMVR	-1, 2	-V _S + 4V +V _S - 2V					V
Common-Mode Rejection Ratio	CMRR	-1	76	76	76		V _{CM} = ±10V	dB min
		-2	82	82	82		V _{CM} = ±10V	
		-1	70	70	70		V _{CM} = ±11V	dB min
		-2	76	76	76		V _{CM} = ±11V	
Open Loop Gain	A _{OL}	-1, 2	150/300	150/300	150/300		R _L = 5k/10k	V/mV min
Output Voltage Swing	V _{OUT}	-1, 2	±12/±11	±12/±11	±12/±11		R _L = 10k/5kΩ	± V min
Power Supply Current	I _Q	-1, 2	0.2	0.2				mA max

NOTES

¹T_A = +25°C, V_S = ±15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

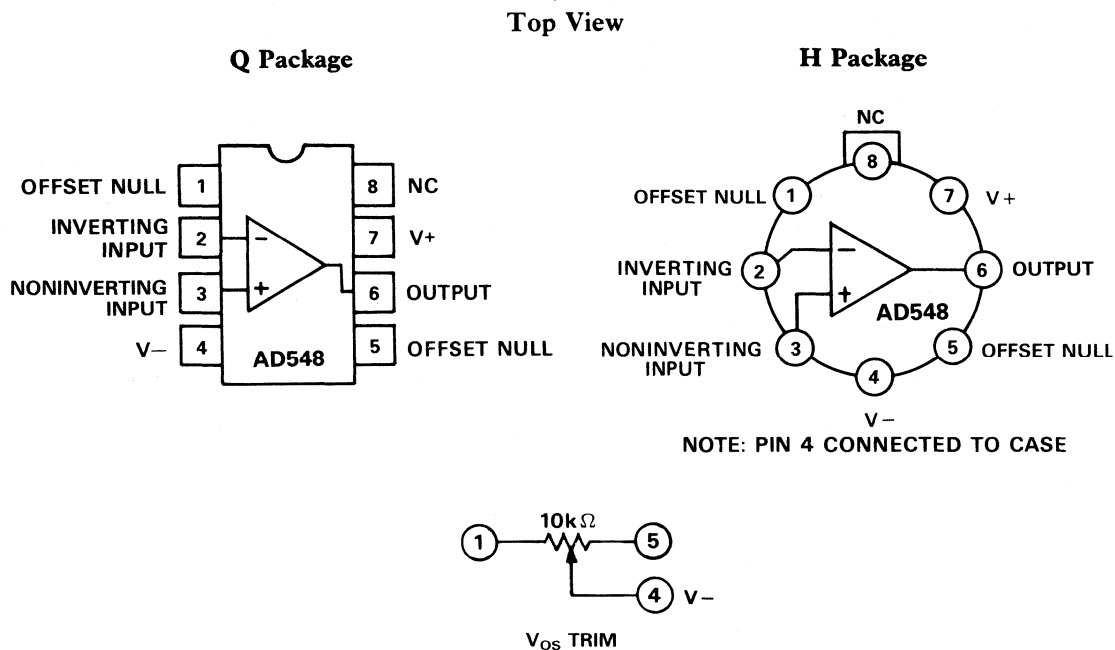
Nulling will induce an additional ±3μV/°C.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

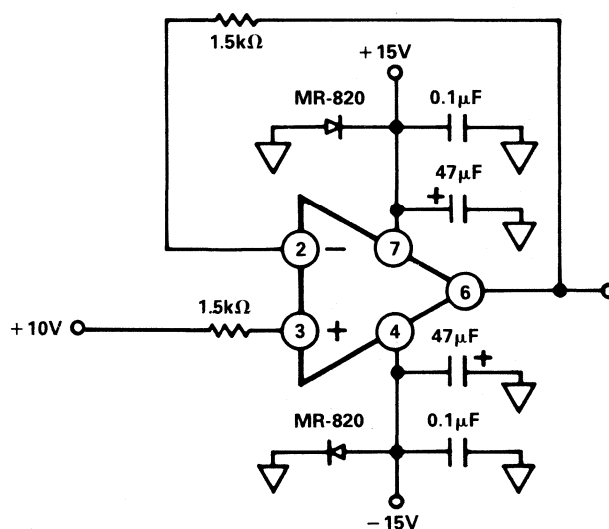


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD549S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

H H-08A 8-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	500 mW
Differential Input Voltage	$+V_S$ and $-V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Package Type		
H-08A	80°C	$7.1\text{ mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$ for H-08A
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$ for H-08A

AD549 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Bias Current ¹	I_B	-1	100	100		Either Input $V_{CM} = 0$	$\pm$ fA max
			100			Either Input $V_{CM} = 10$ V	
Input Offset Current ¹	I_{OS}	-1	30				$\pm$ fA max
Input Offset Voltage ²	V_{OS}	-1	0.5	0.5	2		$\pm$ mV max
Input Offset Voltage Drift	TCV_{OS}	-1	15	15			$\pm$ μ V/°C max
Power Supply Rejection Ratio	PSRR	-1	32	32	50		$\pm$ μ V/V max
Open Loop Gain	A_{OL}	-1	300	300	100	$V_O @ \pm 10$ V, $R_L = 10$ k	V/mV min
Common Mode Voltage Range	CMVR	-1	10	10			$\pm$ V
Common Mode Rejection Ratio	CMRR	-1	90	90	80	$V = \pm 10$ V	dB min
Gain Bandwidth Product	GPW	-1	0.7				MHz min
Slew Rate	t_{SR}	-1	2				V/ μ s min
Output Voltage Swing	V_{OUT}	-1	12		12	$R_L = 10$ k Ω	$\pm$ V min
			10		10	$R_L = 2$ k Ω	
Short Circuit Current	I_{SC}	-1	15	15	6		mA min
Power Supply Current	I_Q	-1	0.7	0.7			mA max

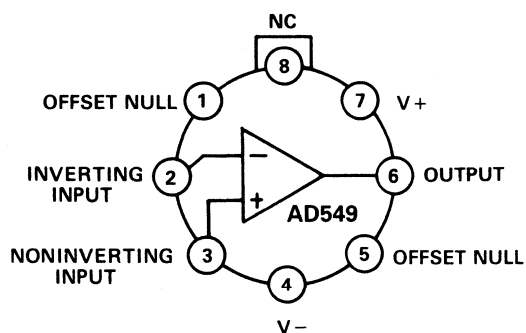
NOTES

¹ $T_A = +25^\circ\text{C}$, $V_S = \pm 15$ V unless otherwise noted. Bias current specifications are guaranteed after 5 minutes of operation at $T_A = +25^\circ\text{C}$. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.

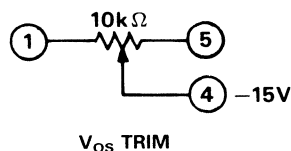
²Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25^\circ\text{C}$.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



NOTE: PIN 4 CONNECTED TO CASE

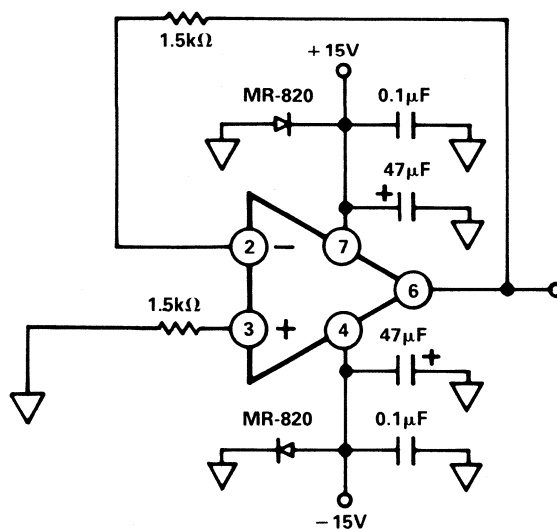


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a 8-bit resolution D/A converter complete with output amplifier, full microprocessor interface, precision reference and requiring only +5V.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD558S(X)/883B
-2	AD558T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-16	16-Pin DIP (TO-116 Style)
E	E-20A	20-Terminal Leadless Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Ground	0 to +18V
Digital Inputs (Pins 1-10)	0 to +7.0V
V_{OUT}	Indefinite Short to Ground Momentary Short to V_{CC}
Power Dissipation	450mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering 10sec)	300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 100^\circ\text{C/W}$

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AD558 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	- 1 - 2	1/2 1/4	1/2 1/2	3/4 3/8	1/4	All Bits with Positive Errors On and All Bits with Negative Errors On	± LSB max
Differential Nonlinearity	DNL	- 1, 2	1	1	1		All Major Carriers	± LSB max
Zero Error	V _{OS}	- 1 - 2	1 1/2	1 1	2 1	1 1/2	All Bits Off	± LSB max
Gain Error	A _E	- 1 - 2	1.5 0.5	1.5 1.5	2.5 1.0	1.5 0.5	No Load and 5mA Load All Bits On	± LSB max
Output Voltage Settling Time		- 1, 2	3.0 1.5				0 to 10V Range ² 0 to 2.56V Range ²	µs max
Power Supply Rejection Ratio	PSRR	- 1, 2	0.03	0.03	0.03		Note 3	%/% max
Power Supply Current	I _{CC}	- 1, 2	25	25	25		All Bits On	± mA max
Power Dissipation	PD	- 1, 2	125 375	125 375	125 375		V _{CC} = + 5V All Bits On V _{CC} = + 15V All Bits On	mW max
Digital Input High Voltage	V _{IH}	- 1, 2	2.0	2.0	2.0			+ V min
Digital Input Low Voltage	V _{IL}	- 1, 2	0.8	0.8	0.8			+ V max
Digital Input High Current	I _{IH}	- 1, 2	100	100	100		V _{IH} = 7V	± µA max
Digital Input Low Current	I _{IL}	- 1, 2	100	100	100		V _{IL} = 0V	± µA max
Write Pulse Width ⁴	t _{WR}	- 1, 2	200		270			ns min
Data Setup Time ⁴	t _{DS}	- 1, 2	200		270			ns min
Data Hold Time ⁴	t _{DH}	- 1, 2	10		10			ns min

NOTES

¹ V_S = + 5V for 0 to 2.56V range, V_S = + 15V for 0 to 10V range (unless otherwise noted).

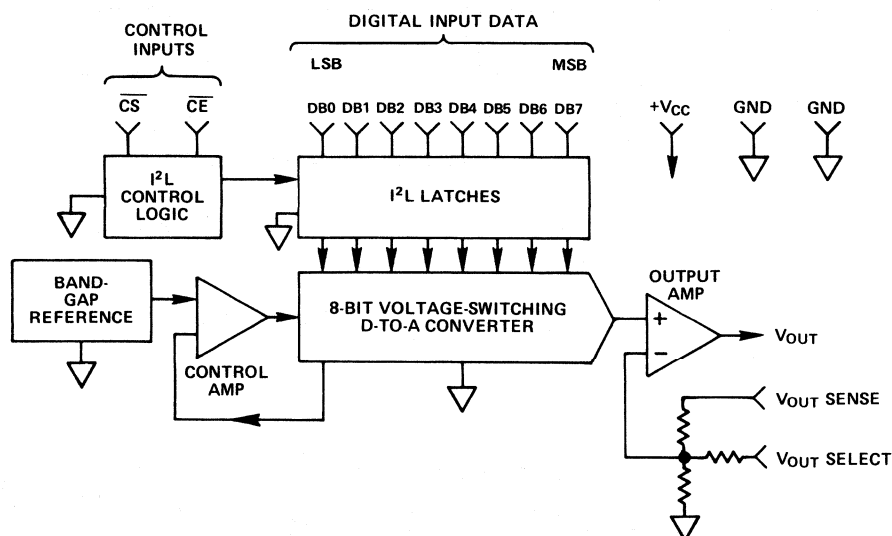
² Settling time is specified for a positive full scale step to ± 1/2LSB.

³ V_{CC} = 4.5V to 5.5V for 0 to 2.56V range, V_{CC} = 11.4V to 16.5V for 0 to 10V range.

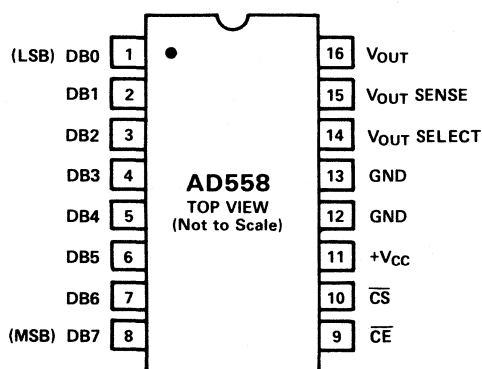
⁴ Timing per Figure 1.

Table 1.

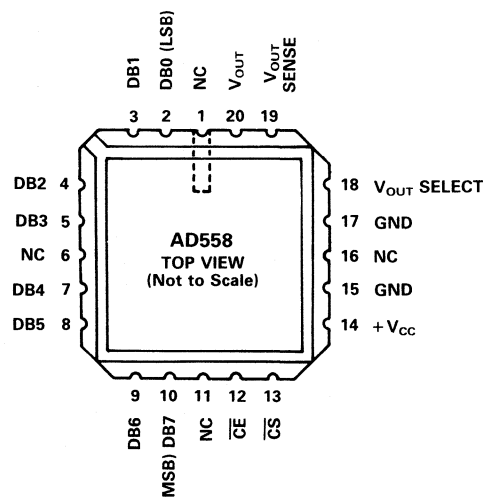
3.2.1 Functional Block Diagram and Terminal Assignments.



D Package (DIP)



E Package (LCC)

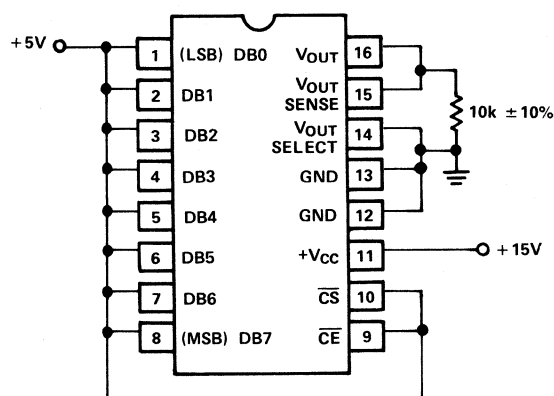


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



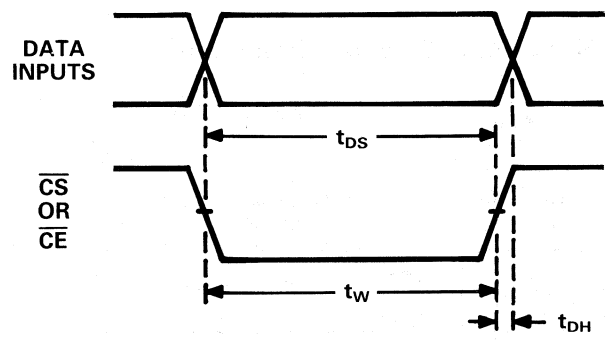


Figure 1. AD558 Timing Diagram

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	“transparent”
1	0	0	1	“transparent”
0	$\overline{\text{f}}$	0	0	latching
1	$\overline{\text{f}}$	0	1	latching
0	0	$\overline{\text{f}}$	0	latching
1	0	$\overline{\text{f}}$	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
 $\overline{\text{f}}$ = Logic Threshold at Positive-Going Transition

Table 2. AD558 Control Logic Truth Table

1.1 Scope.

This specification covers the detail requirements for a precision 10-bit resolution current output D/A converter with an internal precision reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD561SD/883B
-2	AD561TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage (V_{CC})	+16.5V
Supply Voltage (V_{EE})	-16.5V
Digital Input Voltage (V_{IN})	V_{CC} to Ground
Output Voltage Compliance (V_{OUT})	-2V to +10V
10V Span Resistor to Ground	V_{CC} to V_{EE}
Bipolar Offset Resistor to Ground	V_{CC} to V_{EE}
Junction Temperature (T_J)	175°C
Maximum Power Dissipation	500mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 100^\circ\text{C/W}$

AD561 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1/2	1/2			All Bits with + Errors On	± LSB max
		– 2	1/4	1/2		1/4	All Bits with – Errors On	
Differential Nonlinearity	DNL	– 1	1	1	1		Major Carry Transitions	± LSB max
		– 2	1/2	1	1	1/2		
Gain Error	A _E	– 1, 2	0.5	0.5			With Fixed 25Ω Resistor ²	± % of FS max
Gain Error Temperature Coefficient	TCA _E	– 1			60			± ppm of FS/°C
		– 2			30			
Unipolar Offset Error	V _{OS}	– 1, 2	0.05	0.05			See Note 2	± % of FS max
Unipolar Error Temperature Coefficient	TCV _{OS}	– 1			10			± ppm of FS/°C max
		– 2			5			
Bipolar Zero Error	B _{PZE}	– 1, 2	3.5	3.5			With 10Ω Resistor	± LSB max
B/P Zero Error Temperature Coefficient	TCB _{PZE}	– 1			20			± ppm of FS/°C max
		– 2			10			
Output Current	I _{OUT}	– 1, 2	1.5	1.5			Digital Inputs at Logic “1”	– mA min
			2.4	2.4			V _{CC} = + 5V	– mA max
Power Supply Gain Sensitivity	P _{SS1}	– 1, 2	10	10			V _{CC} , + 4.5V to + 5.5 V dc	± ppm of FS/%
							V _{CC} , + 13.5V to + 16.5V dc	
	P _{SS2}	– 1, 2	25	25			V _{EE} , – 10.8V to – 13.2V dc	± ppm of FS/%
							V _{EE} , – 13.2V dc to – 16.5V dc	
Power Supply Current ²	I _{CC}	– 1, 2	10	10			V _{CC} , + 4.5V dc to + 16.5V dc	+ mA max
	I _{EE}	– 1, 2	16	16			V _{EE} , – 10.8V dc to – 16.5V dc	– mA max
Power Dissipation	P _D	– 1, 2	500	500				mW max
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0				+ V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8				+ V max
Digital Input High Current	I _{IH}	– 1, 2	100	100			Digital “1” = 15V	± nA max
Digital Input Low Current	I _{IL}	– 1, 2	25	25			Digital “0” = 0V	± μA max

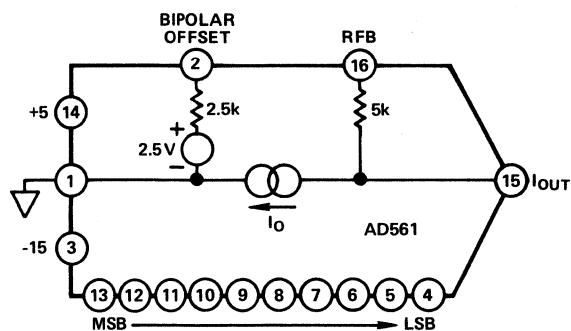
NOTES

¹T_A = 25°C, V_{CC} = + 5V dc, V_{EE} = – 15V dc unless otherwise specified.

²Also tested in CMOS mode. V_{CC} = + 15V dc. V_{EE} = – 15V dc, V_{IH} = 10.5V dc, V_{IL} = 4.5V dc.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

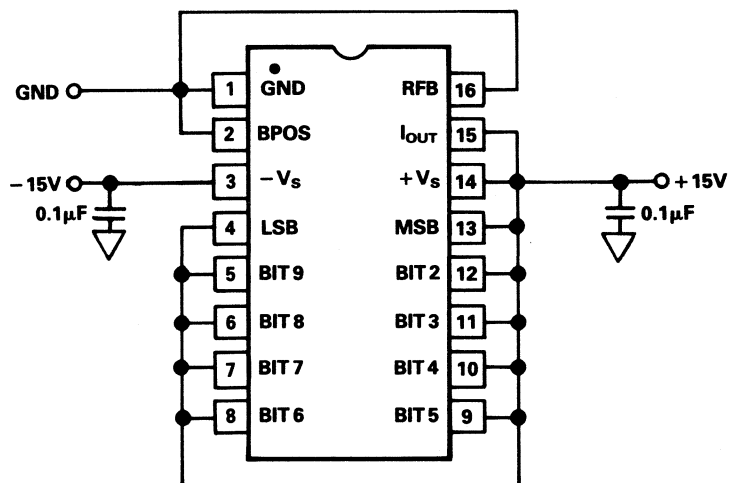


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, current output 12-bit resolution D/A converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD562SD/BIN/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24.

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Supply Voltage ($\pm V_S$)	$\pm 18\text{V dc}$
Reference Voltage, Hi Input	$\pm V_S$
Reference Voltage, Lo Input	$\pm V_S$
Digital Inputs	$\pm V_S$
CMOS/TTL Logic Select	$\pm V_S$
Outputs Pins 7, 8, 10, 11	$\pm V_S$
Outputs Pin 9	$\pm V_S - 5\text{V dc}$
Storage Temperature Range	$-65^\circ\text{C to } +150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 48^\circ\text{C/W}$

AD562 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1/4	1/2		1/4	All bits with positive errors on. All bits with negative errors on.	± LSB max
Differential Nonlinearity	DNL	– 1	1/2	1/2	1		Major Transitions	± LSB max
Gain Error	A _E	– 1	0.20	0.25		0.20	R _{REF} = 50Ω fixed ^{1,2}	± % of FS max
Gain Error Temperature Coefficient	TCA _E	– 1			5			± ppm of FS/°C max
Offset Error	V _{OS}	– 1	0.05	0.05			Notes 1 and 2	± % of FS max
Offset Error Temperature Coefficient	TCV _{OS}	– 1			2			± ppm of FS/°C max
Bipolar Zero Error	BPZE	– 1	0.20	0.25		0.20	R _{BO} = 50Ω fixed ³	± % of FS max
B/P Zero Error Temperature Coefficient	TCBPZE	– 1			4		Note 3	± ppm of FS max/°C
Output Resistance	R _{OUT}	– 1	5.3 7.9				Exclusive of Span Resistors	kΩ min kΩ max
Output Current	I _{OUT}	– 1	1.6 2.4 0.8 1.2	1.6 2.4 0.8 1.2			Unipolar (All Bits On) Bipolar (All Bits On)	– mA min – mA max – mA min – mA max
Power Supply Rejection Ratio	PSRR	– 1	2 2 6	2 2 6			4.75 ≤ V _{CC} ≤ 5.25V 14.25 ≤ V _{CC} ≤ 15.75V ² – 13.5 ≥ V _{EE} ≥ – 16.5V	± ppm of FS/% max
Power Supply Current	I _{CC} I _{EE}	– 1 – 1	18 25	18 25			All Bits Low Notes 1, 2, 4, 5	+ mA max – mA max
Power Dissipation	P _D	– 1	645	645			Notes 1, 2, 4, 5	mW max
Digital Input High Voltage	V _{IH}	– 1	2.0 70	2.0 70			V _{CC} = +5V ⁴ V _{CC} = +15V ^{2,5}	+ V min % V _{CC} min
Digital Input Low Voltage	V _{IL}	– 1	0.8 30	0.8 30			V _{CC} = +5V ⁴ V _{CC} = +15V ^{2,5}	+ V max % V _{CC} max
Digital Input High Current	I _{IH}	– 1	100	100			V _{IH} = 14V ²	+ nA max
Digital Input Low Current	I _{IL}	– 1	100	100			V _{IL} = 0V ²	– μA max

NOTES

¹T_A = 25°C, V_{CC} = +5V, V_{EE} = –15V unless otherwise specified, V_{IH} = 2.0V, V_{IL} = 0.8V, Pin 2 open.

²Tested in CMOS mode; V_{CC} = +15V, V_{EE} = –15V, V_{IH} = 10.5V, V_{IL} = 4.5V, Pin 2 tied to Pin 1.

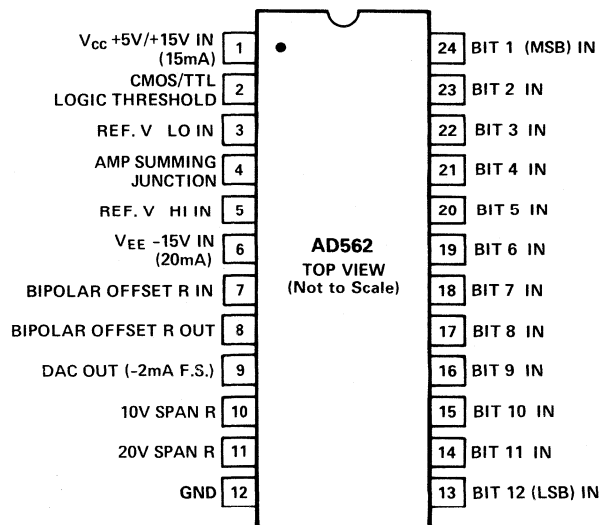
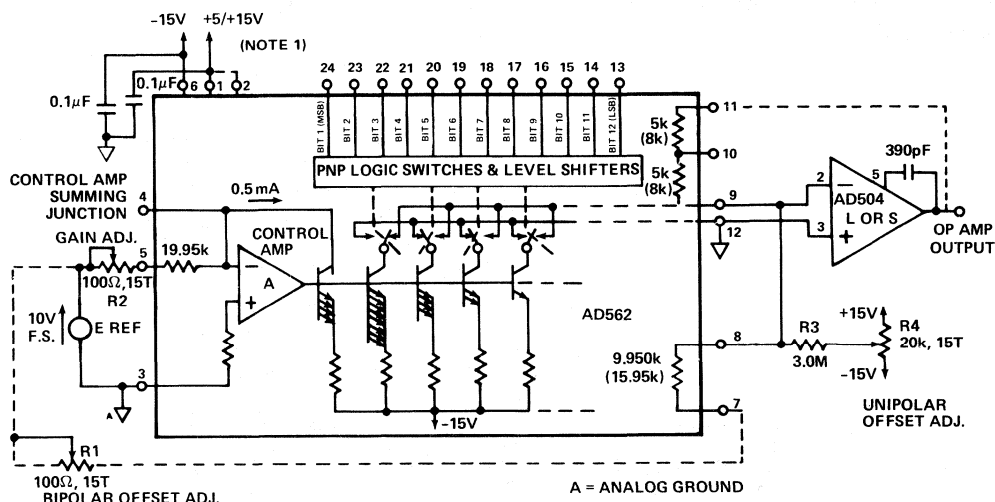
³MSB on; all other bits off.

⁴Guaranteed in TTL mode, Pin 2 open circuit, with 4.75 ≤ V_{CC} ≤ 5.25V, and –14.25 ≥ V_{EE} ≥ –15.75V.

⁵Guaranteed in CMOS mode, Pin 2 tied to Pin 1, with 4.75 ≤ V_{CC} ≤ 15.8V, and –14.25 ≥ V_{EE} ≥ –15.75V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

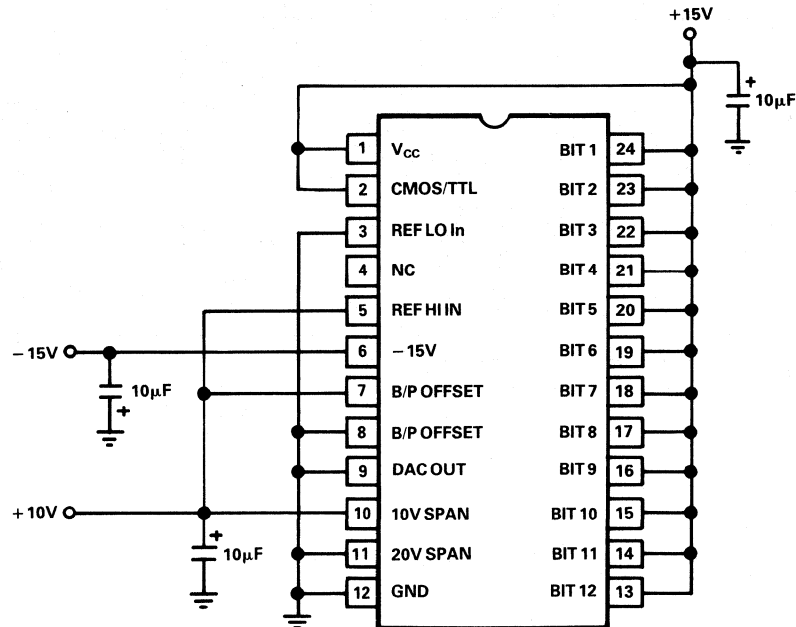


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, current output 12-bit resolution D/A converter with internal buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD563SD/883B
- 2	AD563TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage ($\pm V_S$)	$\pm 18\text{V dc}$
Reference Voltage, High Input	$\pm V_S$
Reference Voltage, Low Input	$\pm V_S$
Digital Inputs	$\pm V_S$
CMOS/TTL Logic Select	$\pm V_S$
Outputs Pins 7, 8, 10, 11	$\pm V_S$
Outputs Pin 9	$\pm V_S - 5\text{V dc}$
Storage Temperature Range	$-65^\circ\text{C to } +150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 48^\circ\text{C/W}$

AD563 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1, 2	1/4	1/2		1/4	All Bits with Positive Errors On. All Bits with Negative Errors On.	± LSB max
Differential Nonlinearity	DNL	– 1, 2	1/2	1/2	1		Major Transitions	± LSB max
Gain Error	A _E	– 1, 2	0.20	0.25		0.20	R _{REF} = 50Ω Fixed ^{1,2}	± % of FS max
Gain Error Temperature Coefficient	TCA _E	– 1 – 2			30 10		See Note 4	± ppm of FS/ °C max
Offset Error	V _{OS}	– 1, 2	0.05	0.05			See Notes 1 and 2	± % of FS max
Offset Error Temperature Coefficient	TCV _{OS}	– 1, 2			2			± ppm of FS/ °C max
Bipolar Zero Error	B _{PZE}	– 1, 2	0.20	0.25		0.20	R _{BO} = 50Ω Fixed ³	± % of FS max
B/P Zero Error Temperature Coefficient	TCB _{PZE}	– 1, 2			10		See Notes 3 and 4	± ppm of FS/ °C max
Output Resistance	R _{OUT}	– 1, 2	5.3 7.9				Exclusive of Span Resistors	kΩ min kΩ max
Output Current	I _{OUT}	– 1, 2	1.6 2.4 0.8 1.2	1.6 2.4 0.8 1.2			Unipolar (All Bits On) Bipolar (All Bits On)	– mA min – mA max – mA min – mA max
Reference Output Voltage	V _{REF}	– 1, 2	2.425 2.575	2.425 2.575	2.425 2.575			+ V min + V max
Power Supply Rejection Ratio	PSRR	– 1, 2	10 10 25	10 10 25			4.75 ≤ V _{CC} ≤ 5.25V 14.25 ≤ V _{CC} ≤ 15.75V ² – 13.5 ≥ V _{EE} ≥ – 16.5V	± ppm of FS/ % max
Power Supply Current	I _{CC} I _{EE}	– 1, 2 – 1, 2	20 25	20 25			See Notes 1, 2, 5 and 6 All Bits Low	+ mA max – mA max
Power Dissipation	P _D	– 1, 2	675	675			Notes 1, 2, 5 and 6	mW max
Digital Input High Voltage	V _{IH}	– 1, 2	2.0 70	2.0 70			V _{CC} = +5V ⁵ V _{CC} = +15V ^{2,6}	+ V min % V _{CC} min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8 30	0.8 30			V _{CC} = +5V ⁵ V _{CC} = +15V ^{2,6}	+ V max % V _{CC} max
Digital Input High Current	I _{IH}	– 1, 2	100	100			V _{IH} = 14V ²	+ nA max
Digital Input Low Current	I _{IL}	– 1, 2	100	100			V _{IL} = 0V ²	– μA max

NOTES

¹T_A = 25°C, V_{CC} = +5V, V_{EE} = –15V unless otherwise specified, V_{IH} = 2.0V, V_{IL} = 0.8V, pin 2 open.

²Tested in CMOS mode; V_{CC} = +15V, V_{EE} = –15V, V_{IH} = 10.5V, V_{IL} = 4.5V, pin 2 tied to pin 1.

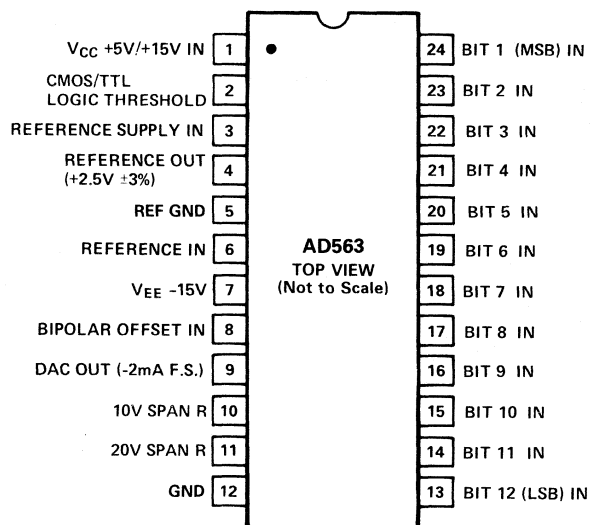
³MSB on; all other bits off.

⁴Including internal reference drift.

⁵Guaranteed in TTL mode, pin 2 open circuit, with 4.75 ≤ V_{CC} ≤ 5.25V, and –14.25 ≥ V_{EE} ≥ –15.75V.

⁶Guaranteed in CMOS mode, pin 2 tied to pin 1, with 4.75 ≤ V_{CC} ≤ 15.8V, and –14.25 ≥ V_{EE} ≥ –15.75V.

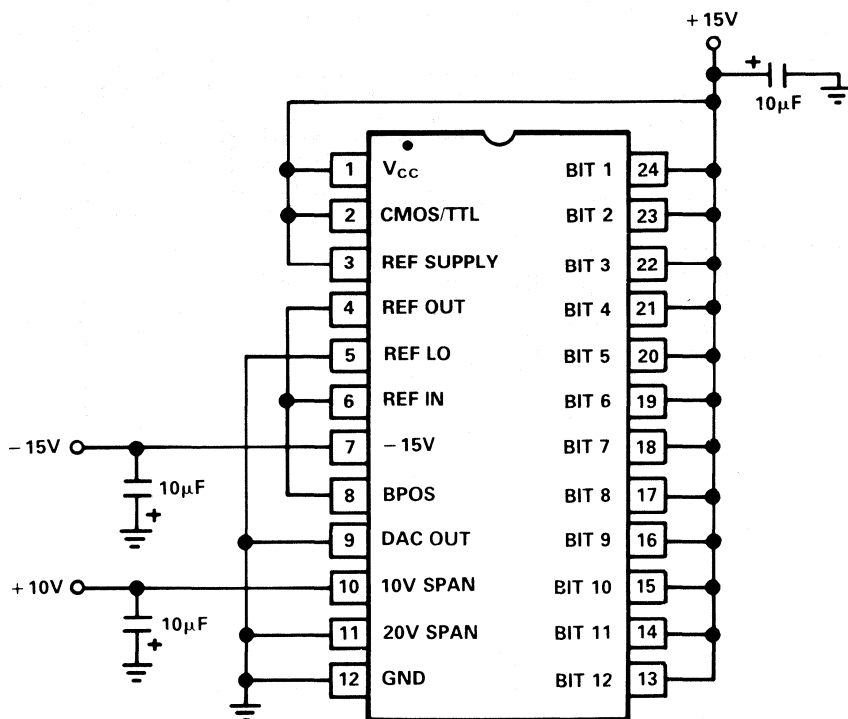
Table 1.



This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, high speed, current output 12-bit resolution D/A converter with internal high stability buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD565ASD/883B
- 2	AD565ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Power Ground	0 to +18V
V_{EE} to Power Ground	0 to -18V
Voltage on DAC Output (Pin 9)	-3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground	-1.0V to +7.0V
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 48^\circ\text{C/W}$

AD565A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1/2	1/2	3/4		All Bits with Positive Errors On. All Bit with Negative Errors On.	± LSB max
		– 2	1/4	1/2	1/2	1/4		
Differential Nonlinearity	DNL	– 1	3/4	3/4	1		Major Transitions	± LSB max
		– 2	1/2	3/4	1	1/2		
Gain Error	A _E	– 1, 2	0.25	0.25			R _{REF} = 50Ω Fixed	± % of FS max
Gain Error Temperature Coefficient	TCA _E	– 1			30			± ppm of FS/ °C max
		– 2			15			
Offset Error	V _{OS}	– 1, 2	0.05	0.05				± % of FS max
Offset Error Temperature Coefficient	TCV _{OS}	– 1, 2			2			± ppm of FS/ °C max
Bipolar Zero Error ²	B _{PZE}	– 1	0.15	0.15			R _{BO} = 50Ω Fixed	± % of FS max
		– 2	0.10	0.15		0.10		
B/P Zero Error Temperature ² Coefficient	TCB _{PZE}	– 1, 2			10			± ppm of FS/ °C max
Input Resistance	R _{IN}	– 1, 2	15					kΩ min
			25					kΩ max
Reference Output Voltage ³	V _{REF}	– 1, 2	9.90	9.90	9.90			+ V min
			10.10	10.10	10.10			+ V max
Reference Output Current ⁴	I _{REF}	– 1, 2	1.5	1.5				+ mA min
Full Scale Transition	t _{FS}	– 1, 2	30				10% to 90% Delay Plus Rise Time	ns max
		– 1, 2	50				90% to 10% Delay Plus Fall Time	ns max
Output Current Settling Time	t _{SL}	– 1, 2	250					ns max
Compliance Voltage	CV	– 1, 2	1.5				– 55°C to + 125°C	– V min
			10					+ V max
Output Resistance	R _{OUT}	– 1, 2	6				Exclusive of Span Resistors	kΩ min
			10					kΩ max
Output Current	I _{OUT}	– 1, 2	1.6	1.6			Unipolar (All Bits On)	– mA min
			2.4	2.4				– mA max
			0.8	0.8			Bipolar (All Bits On)	– mA min
			1.2	1.2				– mA max
Power Supply Rejection Ratio	PSRR	– 1, 2	10	10			V _{CC} = + 11.4V to + 16.5V dc	± ppm of FSR/ % max
			25	25			V _{EE} = – 11.4V to – 16.5V dc	
Power Supply Current ^{4,5}	I _{CC}	– 1, 2	5	5				+ mA max
	I _{EE}	– 1, 2	18	18				– mA max
Power Dissipation	P _D	– 1, 2	345	345				mW max
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0				+ V min
			5.5	5.5				+ V max
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8				+ V max
Digital Input High Current	I _{IH}	– 1, 2	300	300			V _{IH} = 5.5V	+ μA max
Digital Input Low Current	I _{IL}	– 1, 2	100	100			V _{IL} = 0V	+ μA max

NOTES

¹V_{CC} = + 15V, V_{EE} = – 15V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = 25°C unless otherwise indicated. V_{IH} = 2.0V, and V_{IL} = 0.8V guaranteed design limits at – 55°C and + 125°C.

²MSB on; all other bits off.

³In subgroup 1, the reference output is loaded with 0.5mA reference input current, 1.0mA bipolar offset current, and 1.5mA additional current. In subgroups 2 and 3, only the 0.5mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

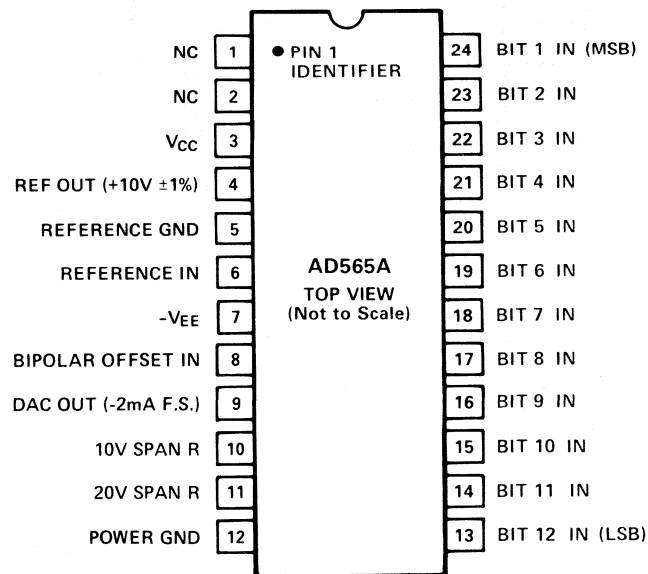
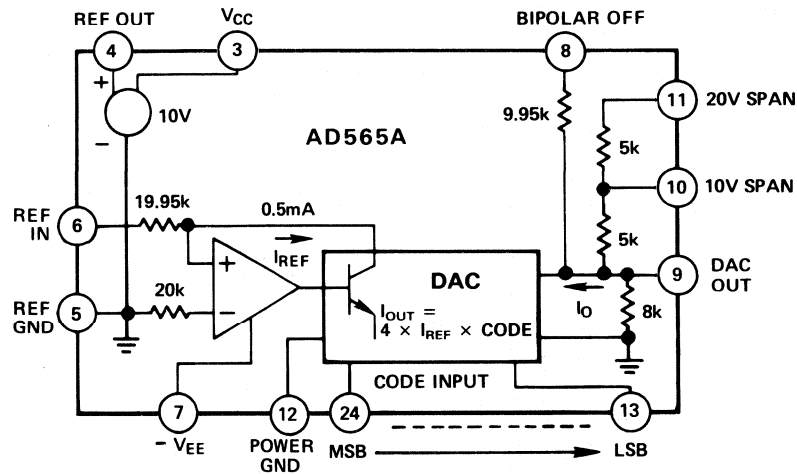
⁴Guaranteed for + 11.4 ≤ V_{CC} ≤ + 16.5V.

⁵Guaranteed for – 11.4 ≥ V_{EE} ≥ – 16.5V.

Table 1.

REV. C

3.2.1 Functional Block Diagram and Terminal Assignments.



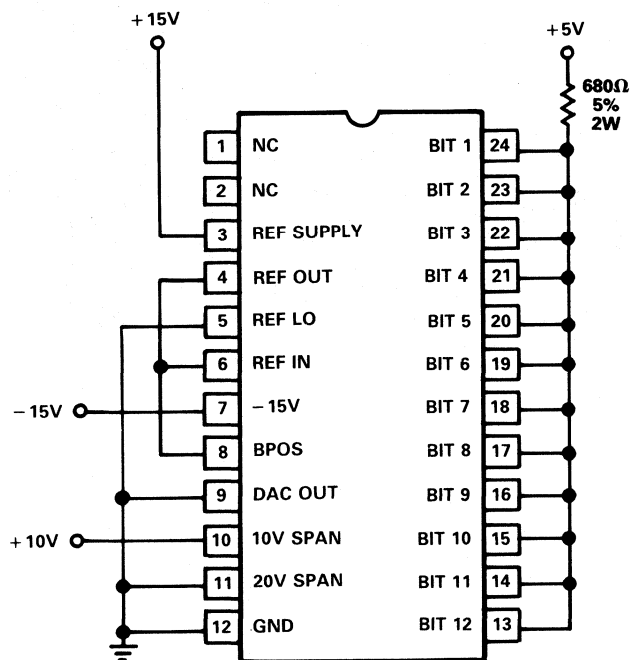
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

AD565A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, high speed current output 12-bit resolution D/A converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD566ASD/883B
-2	AD566ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{EE} to Power Ground	0 to -18V
Voltage on DAC Output (Pin 9)	-3V to $+12\text{V}$
Digital Inputs (Pins 13 to 24) to Power Ground	-1.0V to $+7.0\text{V}$
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Power Dissipation	1000mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 48^\circ\text{C/W}$

AD566A — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	-1	1/2	1/2	3/4		All Bits with Positive Errors On. All Bits with Negative Errors On.	± LSB max
		-2	1/4	1/2	1/2	1/4		
Differential Nonlinearity	DNL	-1	3/4	3/4	1		Major Transitions	± LSB max
		-2	1/2	3/4	1	1/2		
Gain Error	A _E	-1, 2	0.25	0.25			R _{REF} = 50Ω Fixed	± % of FS max
Gain Error Temperature	TC _{AE}	-1			10			± ppm of FS/°C max
		-2			5			
Offset Error	V _{OS}	-1, 2	0.05	0.05				± % of FS max
Offset Error Temperature Coefficient	TCV _{OS}	-1, 2			2			± ppm of FS/°C max
Bipolar Zero Error ²	B _{PZE}	-1	0.15	0.15			R _{BO} = 50Ω Fixed	± % of FS max
		-2	0.10	0.15		0.10		
B/P Zero Error ² Temperature Coefficient	TCB _{PZE}	-1, 2			10			± ppm of FS/°C max
Input Resistance	R _{IN}	-1, 2	15					kΩ min
			25					kΩ max
Full Scale Transition	t _{FS}	-1, 2	30				10% to 90% Delay Plus Rise Time	ns max
			50				90% to 10% Delay Plus Fall Time	
Output Current Settling Time	t _{SL}	-1, 2	350					ns max
Compliance Voltage	CV	-1, 2	1.5				-55°C to +125°C	- V min
			10					+ V max
Output Resistance	R _{OUT}	-1, 2	6				Exclusive of Span Resistors	kΩ min
			10					kΩ max
Output Current	I _{OUT}	-1, 2	1.6	1.6			Unipolar (All Bits On)	- mA min
			2.4	2.4				- mA max
			0.8	0.8			Bipolar (All Bits On)	- mA min
			1.2	1.2				- mA max
Power Supply Rejection Ratio ³	PSRR	-1, 2	25	25				± ppm of FS/% max
Power Supply Current ³	I _{EE}	-1, 2	18	18				- mA max
Power Dissipation	P _D	-1, 2	300	300				mW max
Digital Input High Voltage	V _{IH}	-1, 2	2.0	2.0				+ V min
			5.5	5.5				+ V max
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8				+ V max
Digital Input High Current	I _{IH}	-1, 2	300	300			V _{IH} = 5.5V	+ μA max
Digital Input Low Current	I _{IL}	-1, 2	100	100			V _{IL} = 0V	+ μA max

NOTES

¹V_{EE} = -15V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = +25°C unless otherwise indicated.

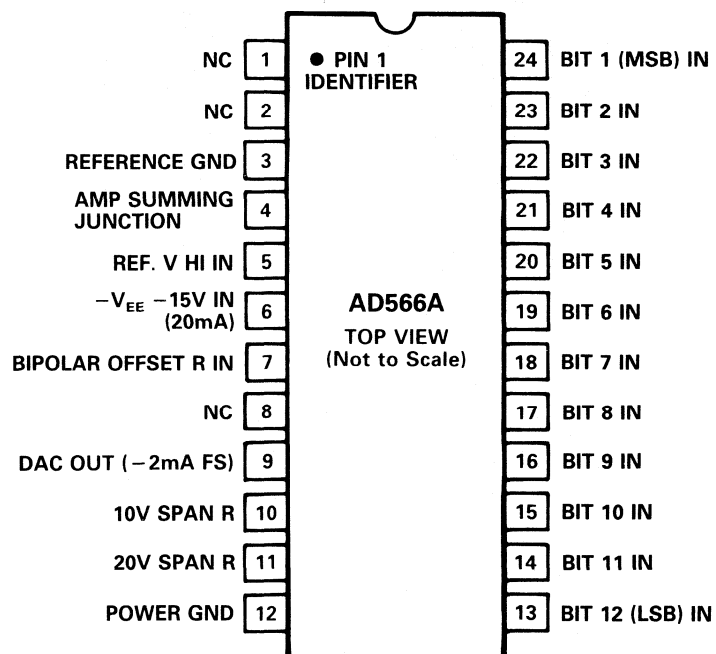
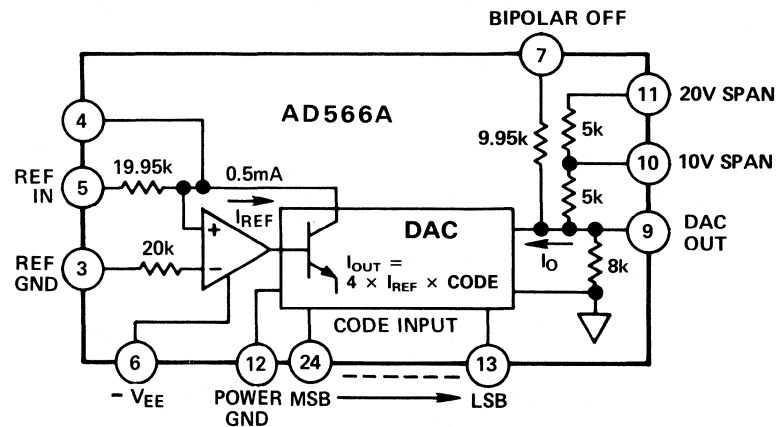
V_{IH} = 2.0V, V_{IL} = 0.8V guaranteed design limits at -55°C to +125°C.

²MSB on; all other bits off.

³Guaranteed for -11.4 ≥ V_{EE} ≥ -16.5V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



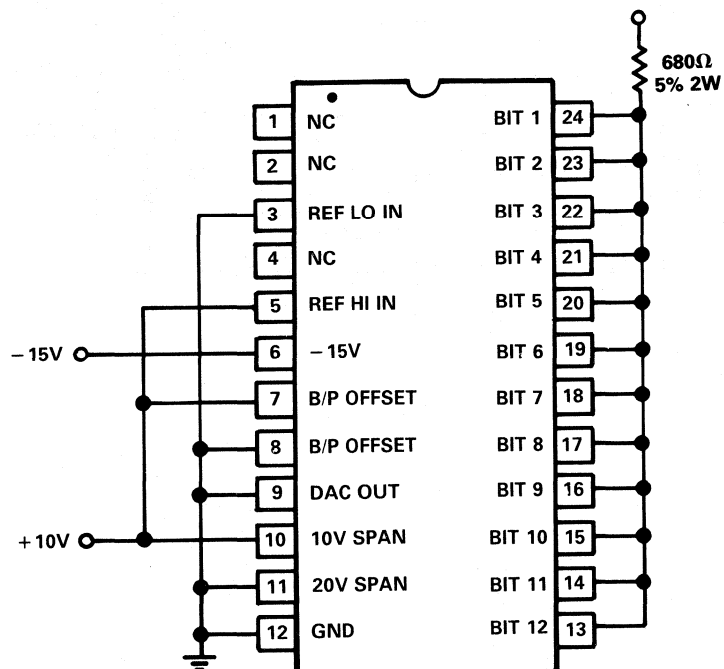
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

AD566A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for a high speed 12-bit resolution bipolar current output D/A converter with double buffered latch and high stability buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD567SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-28.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Power Ground	0 to +18V
V_{EE} to Power Ground	0 to –18V
Voltage on DAC Output (Pin 2)	–3V to +12V
Digital Inputs (Pins 10-15, 17-28) to Power Ground	–1.0V to +7.0V
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 60^\circ\text{C/W}$

AD567 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1/2	1/2	3/4	All Bits with Positive Errors On. All Bits with Negative Errors On.	± LSB max
Differential Nonlinearity	DNL	– 1	3/4	3/4	1	Major Carry Errors	± LSB max
Gain Error ²	A _E	– 1	0.25	0.25		All Bits On	± % FSR max
Gain Temperature Coefficient	TCA _E	– 1	30		30	All Bits On	± ppm/°C max
Unipolar Offset Error	V _{OS}	– 1	0.05	0.05		All Bits Off	± % FSR max
Temperature Coefficient Unipolar Offset	TCV _{OS}	– 1	2		2	All Bits Off	± ppm/°C max
Bipolar Zero Error ³	B _{PZE}	– 1	0.15	0.15		MSB On, All Other Bits Off Bipolar	± % FSR max
B/P Zero Temperature Coefficient	TCB _{BZE}	– 1	10		10	MSB On, All Other Bits Off Bipolar	± ppm/°C max
Reference Input Resistance	R _{IN}	– 1	15				kΩ min
			25				kΩ max
Output Resistance	R _{OUT}	– 1	6			Exclusive of Span Resistor	kΩ min
			10				kΩ min
Reference Output Voltage	V _{REF}	– 1	9.9	9.9	9.9	Bipolar, 0.1mA External Load	V min
			10.10	10.10	10.10	V _{CC} = +12V, V _{EE} = –12V ⁴	V max
Compliance Voltage	V _{CPL}	– 1	1.5				– V min
			10.0				V max
Output Current Settling Time	t _{SL}	– 1	500			See Figure 1	ns max
Output Current	I _{OUT}	– 1	1.6	1.6		Unipolar All Bits On	– mA min
			2.4	2.4		V _{IH} + 5.0V	– mA max
			0.8	0.8		Bipolar All Bits On	– mA min
			1.2	1.2		V _{IH} + 5.0V	– mA max
Power Supply Rejection Ratio	PSRR	– 1	10	10		+11.4V ≤ V _{CC} ≤ +16.5V,	ppm of FSR/
			25	25		–16.5V ≤ V _{EE} ≤ –11.4V	% max
Power Supply Current	I _{CC}	– 1	5	5		V _{CC} = +16.5V, V _{EE} = –16.5V	mA max
	I _{EE}	– 1	25	25		All Bits Low	– mA max
Power Dissipation	P _D	– 1	495	495		V _{CC} = +16.5V, V _{EE} = –16.5V All Bits Low	mW max
Digital Input High Voltage	V _{IH}	– 1	2.0	2.0			V min
			5.5				V max
Digital Input Low Voltage	V _{IL}	– 1	0.8	0.8			V max
Digital Input High Current	I _{IH}	– 1	300	300		V _{IH} = 5.5V	μA max
Digital Input Low Current	I _{IL}	– 1	100	100		V _{IL} = 0.0V	μA max
Write Pulse Width	t _{WR}	– 1	100			See Note 5	ns min
Data Setup Time	t _{OW}	– 1	50			See Note 5	ns min
Data Hold Time	t _{DH}	– 1	10			See Note 5	ns min
$\overline{\text{CS}}$ Valid to End of $\overline{\text{WR}}$	t _{CW}	– 1	100			See Note 5	ns min
Address Valid End of $\overline{\text{WR}}$	t _{AW}	– 1	100			See Note 5	ns min
Latch Functionality	A _{EA}	– 1	1	1	1	See Notes 6 and 7	± LSB max
Latch Functionality	V _{OSA}	– 1	1	1	1	See Note 6	± LSB max

Table 1. (Continued on next page)

REV. C

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

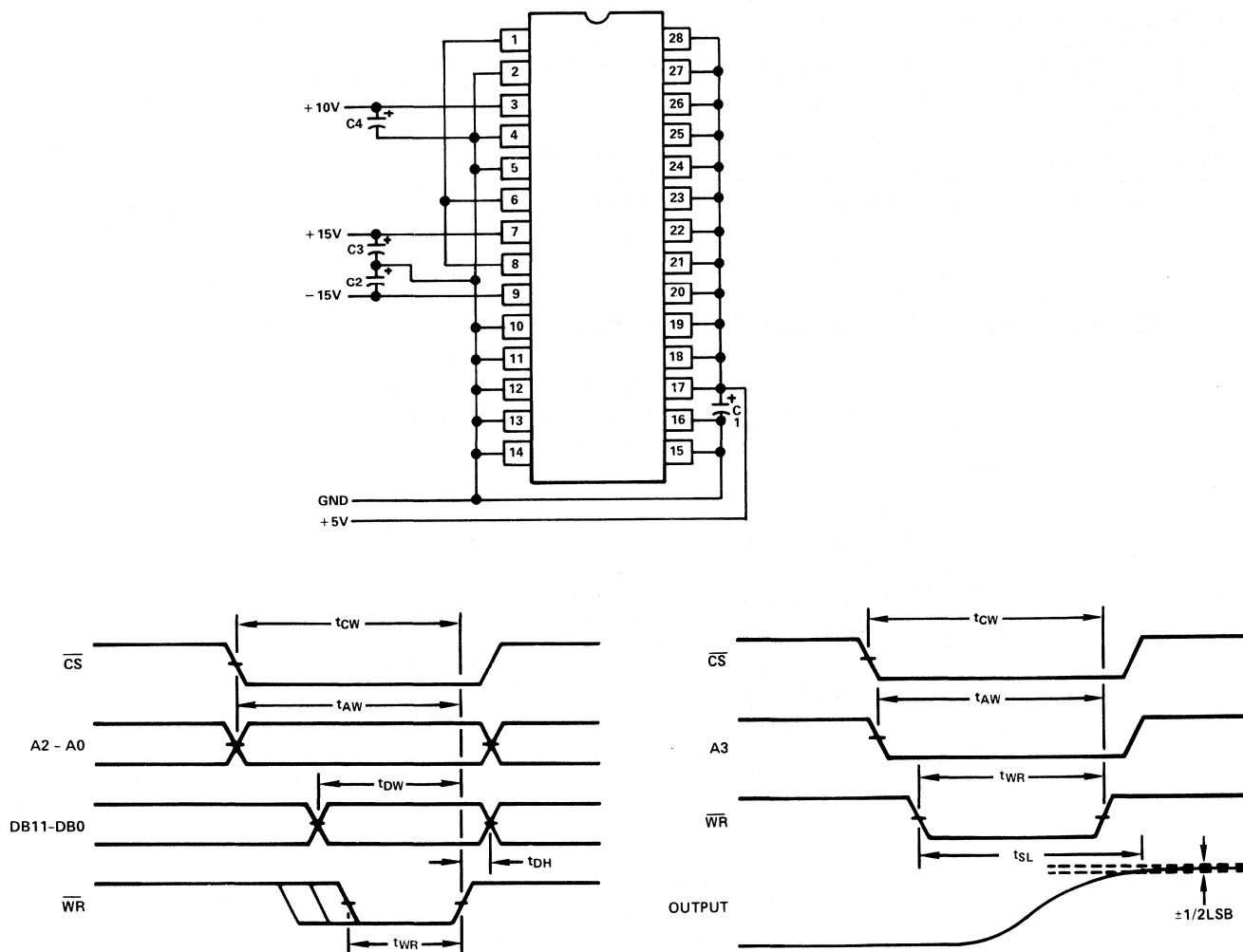


Figure 1.

$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No Operation
X	1	X	X	X	X	No Operation
0	0	1	1	1	0	Enable 4 LSBs of First Rank
0	0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table 2. AD567 Truth Table

1.1 Scope.

This specification covers the detail requirements for a precision, ultrahigh speed, current/voltage output 12-bit resolution D/A converter with internal high stability buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD568SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-24.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to RefCOM	0V to +18V
V_{EE} to RefCOM	0V to -18V
RefCOM to LCOM	+100mV to -10V
ACOM to LCOM	$\pm 100\text{mV}$
THCOM to LCOM	$\pm 500\text{mV}$
SPANs to LCOM	$\pm 12\text{V}$
I_{BPO} to LCOM	$\pm 5\text{V}$
I_{OUT} to LCOM	-5V to V_{TH}
Digital Inputs to THCOM	-500mV to +7V
Voltage Across Span Resistors	12V
V_{TH} to THCOM	-0.7V to +1.4V
Logic Threshold Control Input Current	5mA
Power Dissipation	1000mW
Storage Temperature Range Q (Cerdip) Package	-65°C to $+150^\circ\text{C}$
Junction Temperature	175°C
Lead Temperature (Soldering, 10secs)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 75^\circ\text{C/W}$

AD568 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Relative Accuracy ²	RA	– 1	1/2	1/2	3/4	All Bits with Positive Errors On, All Bits with Negative Errors On	± LSB max
Differential Nonlinearity ²	DNL	– 1	1	1	1	Major Carry Errors	± LSB max
Gain Error ²	A _E	– 1	1.0	1.0		All Bits On	± % FSR max
Gain Temperature Coefficient	TCA _E	– 1	50		50	All Bits On, V _{OUT} Mode	± ppm/°C max
			150		150	All Bits On, I _{OUT} Mode	
Unipolar Offset Error ²	V _{OS}	– 1	0.20	0.20		All Bits Off	± % FSR max
Unipolar Offset TC ³	TCV _{OS}	– 1	5		5	All Bits Off	± ppm/°C max
Bipolar Offset Error ²	B _{POE}	– 1	1.0	1.0		All Bits Off, Bipolar	± % FSR max
Bipolar Offset TC ³	TCB _{POE}	– 1	30		30	All Bits Off, Bipolar	± ppm/°C max
Bipolar Zero Error ²	B _{PZE}	– 1	0.20	0.20		MSB On, All Other Bits Off, Bipolar	± % FSR max
Bipolar Zero TC ³	TCB _{PZE}	– 1	15		15	MSB On, All Other Bits Off, Bipolar	± ppm/°C max
Output Resistance	R _{OUT}	– 1	160				Ω min
			240				Ω max
Voltage Settling Time	t _{SV}	– 1	50				ns typ to 0.025%
Current Settling Time	t _{SI}	– 1	35				ns typ to 0.025%
Full-Scale Transition	t _{FS}	– 1	11			10% to 90% Reset Time 90% to 10% Fall Time	ns typ
Glitch Impulse	GI	– 1	350				pV-sec typ
Compliance Voltage	CV	– 1	2				– V min
			1.2				+ V max
Output Current	I _{OUT}	– 1		10.137 10.343		Unipolar All Bits On	+ mA min + mA max
				5.017 5.223		Bipolar All Bits On	+ mA min + mA max
Power Supply Rejection Ratio	PSRR	– 1	0.05	0.05		V _{CC} = +13.5V to +16.5V V _{EE} = –13.5V to –16.5V	± % FS/V max
Power Supply Current ^{4, 5}	I _{CC}	– 1	32	32		All Bits High	+ mA max
	I _{EE}	– 1	8	8			– mA max
Power Consumption	P _C	– 1	625				mW max
Digital Input High Voltage	V _{IH}	– 1	2.0	2.0	2.0		+ V min
Digital Input Low Voltage	V _{IL}	– 1	0.8	0.8	0.8		+ V max
Digital Input High Current	I _{IH}	– 1	10	10	10	V _{IH} = 2V	± μA max
Digital Input Low Current	I _{IL}	– 1	0.5	0.5	0.5	V _{IL} = 0.0V	– μA min
			100	100	200		– μA max

NOTES

¹V_{CC} = +15V, V_{EE} = –15V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = +25°C unless otherwise specified.

V_{IH} = +2.0V and V_{IL} = 0.8V guaranteed design limits at –55°C and +125°C.

²Measured in I_{OUT} mode.

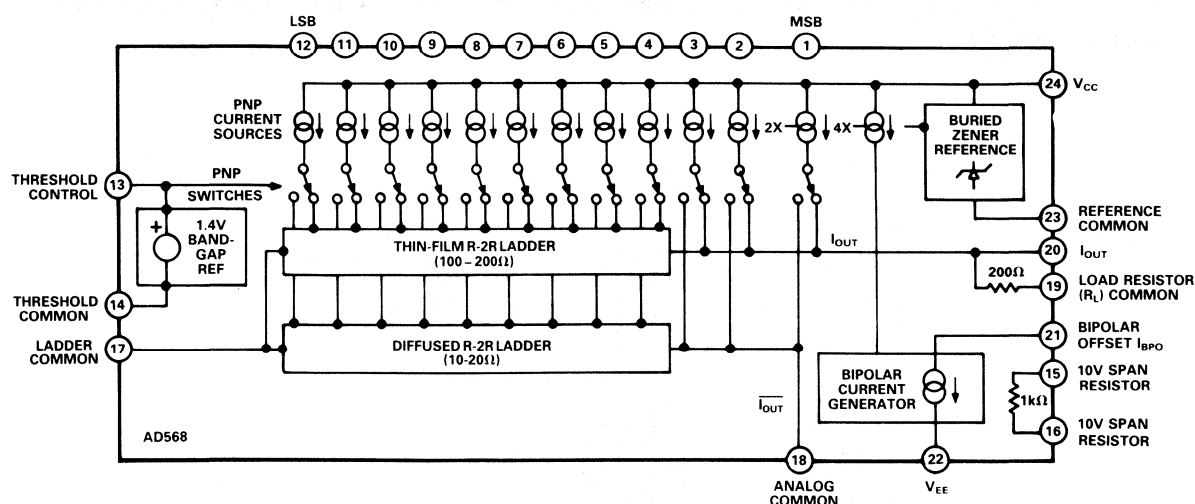
³Measured in V_{OUT} mode.

⁴Guaranteed for +13.5 ≤ V_{CC} ≤ +16.5V.

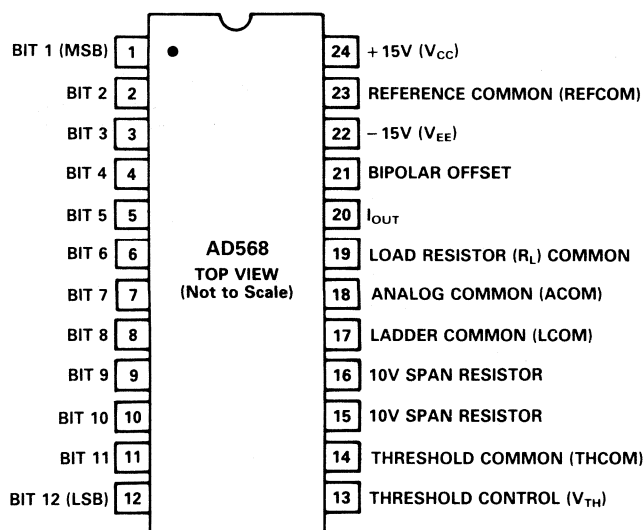
⁵Guaranteed for –13.5 ≤ V_{EE} ≤ –16.5V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



24-Lead "Skinny" Cerdip Package



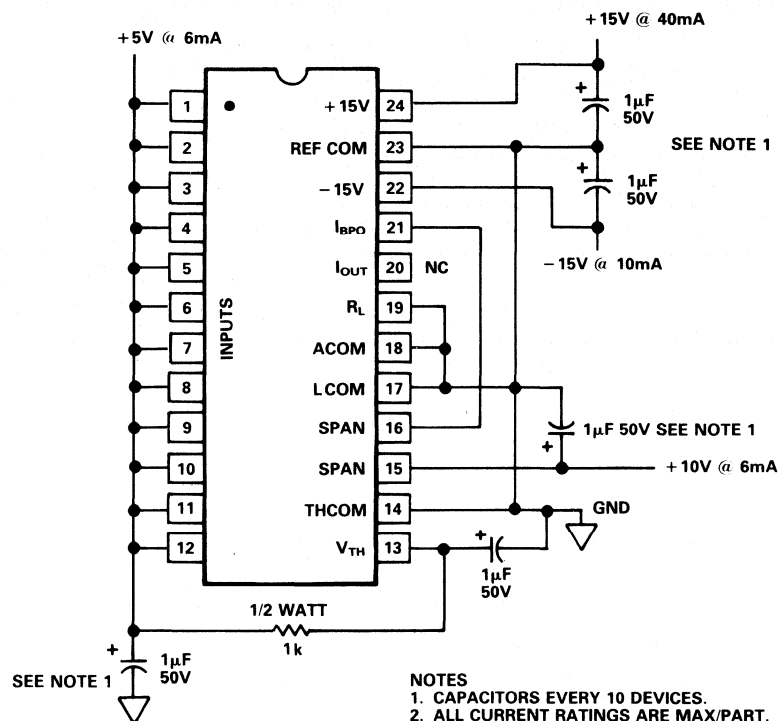
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

AD568

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for complete 8-bit and 10-bit resolution A/D converters with the three state logic outputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD570SD/883B
-2	AD571SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-18.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Digital Common	+7V
V_{EE} to Digital Common	-16.5V
Analog Common to Digital Common	$\pm 1\text{V}$
Analog Input to Analog Common	$\pm 15\text{V}$
Control Inputs	0 to V_{CC}
Digital Outputs (Blank Mode)	0 to V_{CC}
Power Dissipation	800mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 88^\circ\text{C/W}$

AD570/AD571 – SPECIFICATIONS

Test	Symbol	Device ²	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1	0.195	0.195	0.195		Unipolar and Bipolar	± % of FS max
		– 2	0.098	0.195	0.098	0.098	Major Transitions ± 3 Codes	
Differential Nonlinearity ³	DNL	– 1	8	8	8		All Codes Test	Bits min
		– 2	10	8	10	10	Unipolar and Bipolar	
Full-Scale Error ⁴	A _E	– 1, 2	40	40			Unipolar	± mV max
		– 1, 2	20	20			Bipolar	
Full-Scale Temperature Drift	TCA _E	– 1			0.781			± % of FS max
		– 2			0.488			
Offset Error	V _{OS}	– 1	20	20			First Transition	± mV max
		– 2	10	20		10		
Offset Temperature Drift	TCV _{OS}	– 1			0.391			± % of FS max
		– 2			0.195			
Bipolar Zero Error	B _{PZE}	– 1	20	20			Low Side MSB, Transition Bipolar	± mV max
		– 2	10	20		10	Bipolar	
Bipolar Zero Temperature Drift	TCB _{PZE}	– 1			0.391		Bipolar	± % of FS max
		– 2			0.195			
Input Resistance	R _{IN}	– 1, 2	3	3	3			kΩ min
			7	7	7			kΩ max
Conversion Time ⁵	TC	– 1, 2	15	15	15			μs min
			40	40	40			μs max
Three-State Leakage Current	I _{OLT}	– 1	40	40	40		V _{OL} = 0.0V, Bit 1–Bit 8	± μA max
		– 2	40	40	40		V _{OL} = 0.0V, Bit 1–Bit 10	
Power Supply Rejection Ratio	PSRR	– 1	78.1	78.1	78.1		– 16.0V ≤ V _{EE} ≤ – 13.5, V _{CC} = +15V	± mV max
		– 2	19.5	78.1	78.1	19.5	+ 4.5V ≤ V _{CC} ≤ 5.5V, V _{EE} = – 15V	
Power Supply Current	I _{CC}	– 1, 2	10	10			Convert	+ mA max
			10	10			Blank	
	I _{EE}	– 1, 2	15	15				– mA max
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0		Blank and $\overline{\text{Convert}}$	+ V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8		Blank and $\overline{\text{Convert}}$	+ V max
Digital Input High Current	I _{IH}	– 1, 2	100	100	100		Blank and $\overline{\text{Convert}}$, V _{IH} = 5.0V	± μA max
Digital Input Low Current	I _{IL}	– 1, 2	100	100	100		Blank and $\overline{\text{Convert}}$, V _{IL} = 0.0V	± μA max
Digital Output Low Voltage	V _{OL}	– 1	0.4	0.4	0.4		$\overline{\text{DR}}$, Bit 1–Bit 8, I _{OL} = + 3.2mA	+ V max
		– 2	0.4	0.4	0.4		I _{OL} = + 3.2mA, $\overline{\text{DR}}$, Bit 1–Bit 10	
Digital Output High Voltage	V _{OH}	– 1	2.4	2.4	2.4		Bit 1–Bit 8, I _{OH} = – 0.5mA	+ V min
		– 2	2.4	2.4	2.4		I _{OH} = – 0.5mA, Bit 1–Bit 10	

NOTES

¹V_{CC} = + 5V, V_{EE} = – 15V, V_{IH} = + 2.0V, V_{IL} = + 0.8V, analog input through 15Ω to Pin 13, Unipolar configuration.

T_A = 25°C unless otherwise indicated.

Unipolar configuration Pin 15 (Bipolar Offset Control) is grounded.

Bipolar configuration Pin 15 is not connected.

²For – 1 (8-bit resolution device), 0.391% of full scale = 1LSB (Least Significant Bit).

For – 2 (10-bit resolution device), 0.098% of full scale = 1LSB.

³Minimum resolution for which no missing codes are guaranteed.

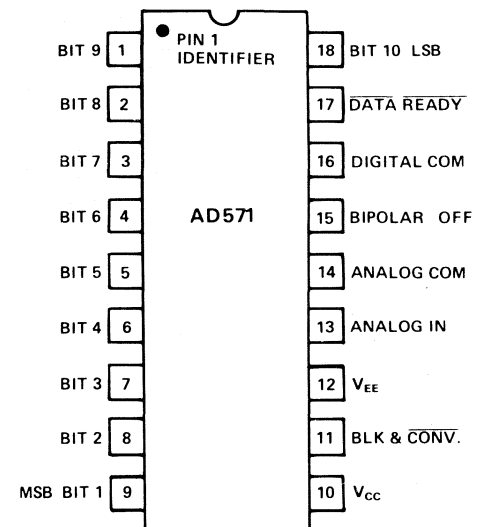
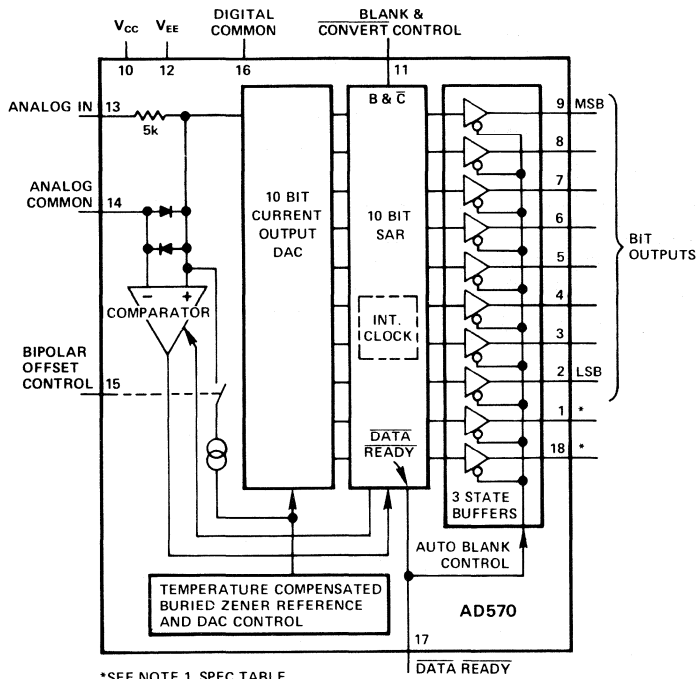
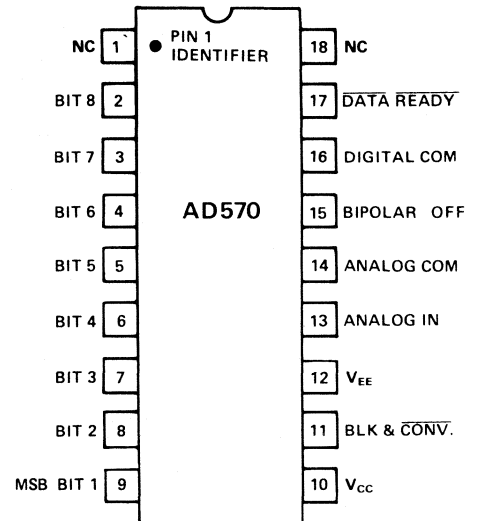
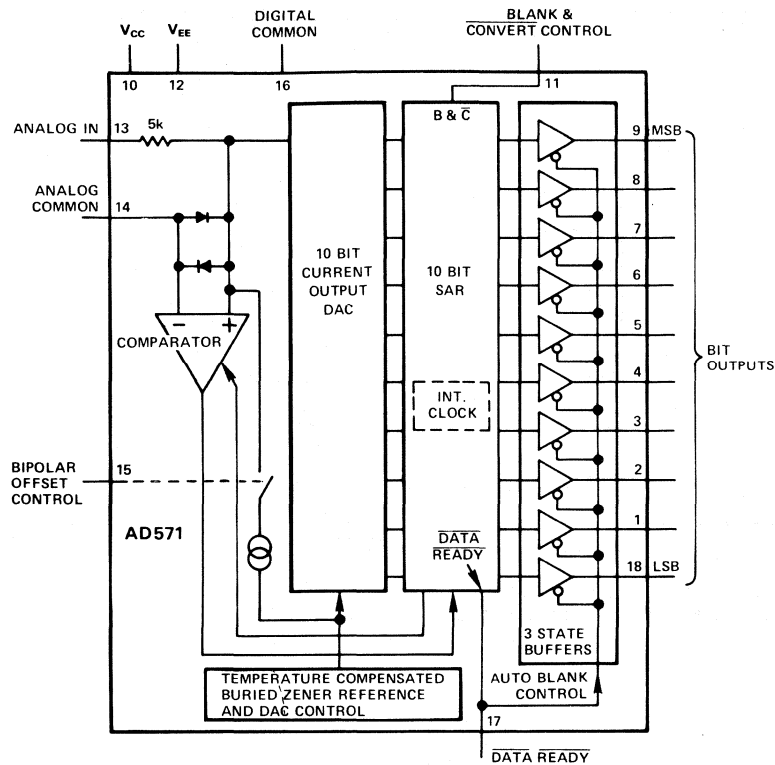
⁴For – 1 device Full Scale Error guaranteed trimmable with 200Ω potentiometer.

For – 2 device Full Scale Error guaranteed trimmable with 50Ω potentiometer.

⁵See Figure 1.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



*SEE NOTE 1, SPEC TABLE

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

AD570/AD571

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

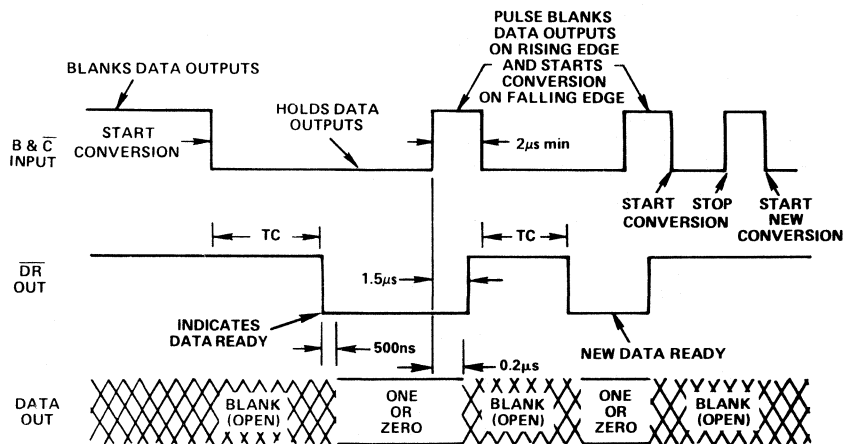
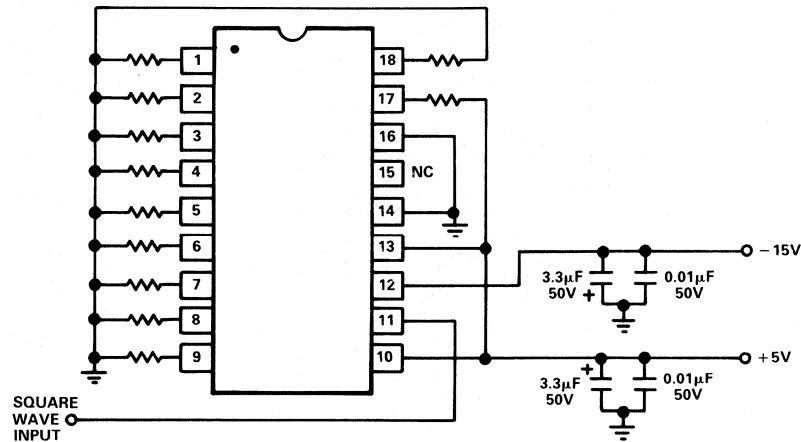


Figure 1. AD570 and AD571 Timing Control Sequences



Fast, Complete 8-/10-Bit A/D Converter with Microprocessor Interface

AD573/AD673

1.1 Scope.

This specification covers the detail requirements for complete 8-bit and 10-bit resolution A/D converters with full microprocessor interface.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD673SD/883B
-2	AD573SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-20.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Digital Common	+7V
V_{EE} to Digital Common	-16.5V
Analog Common to Digital Common	$\pm 1\text{V}$
Analog Input to Analog Common	$\pm 15\text{V}$
Control Inputs	0 to V_{CC}
Digital Outputs (High Impedance State)	0 to V_{CC}
Power Dissipation	800mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 85^\circ\text{C/W}$

AD573/AD673 – SPECIFICATIONS

Test	Symbol	Device ²	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1	0.195	0.195	0.195		Unipolar and Bipolar Major Transitions ± 3 Codes	± % of FS max
		– 2	0.098	0.195	0.098	0.098		
Differential Nonlinearity ³	DNL	– 1	8	8	8		All codes test Unipolar and Bipolar	Bits min
		– 2	10	8	10	10		
Full-Scale Error ⁴	A _E	– 1, 2	40	40			Unipolar	± mV max
		– 1, 2	20	20			Bipolar	± mV max
Full-Scale Temperature Drift	TCA _E	– 1	0.781		0.781			± % of FS max
		– 2	0.488		0.488			
Offset Error	V _{OS}	– 1	20	20			First Transition	± mV max
		– 2	10	20		10		
Offset Temperature Drift	TCV _{OS}	– 1	0.391		0.391			± % of FS max
		– 2	0.195		0.195			
Bipolar Zero Error	B _{PZE}	– 1	20	20			Low Side MSB Transition Bipolar	± mV max
		– 2	10	20		10		
Bipolar Zero Temperature Drift	TCB _{PZE}	– 1	0.391		0.391		Low Side MSB Transition Bipolar	± % of FS max
		– 2	0.195		0.195			
Input Resistance	R _{IN}	– 1, 2	3	3	3			kΩ min
			7	7	7			kΩ max
Conversion Time ⁵	t _C	– 1, 2	10	10	10			μs min
			30	30	30			μs max
Three-State Leakage Current	I _{OLT}	– 1	40	40	40		V _{OH} = 5.0V V _{OL} = 0.0V, DB0-DB7	± μA max
		– 2	40	40	40		V _{OH} = 5.0V V _{OL} = 0.0V, DB0-DB9	
Power Supply Rejection Ratio	PSRR	– 1	78.1	78.1	78.1		V _{CC} = 5V, – 15.75V ≤ V _{EE} ≤ – 14.25V V _{CC} = 5V, – 12.6V ≤ V _{EE} ≤ – 11.4V	± mV max
		– 2	19.5	78.1	78.1	19.5	V _{EE} = – 15V, 4.5V ≤ V _{CC} ≤ 5.5V	
Power Supply Current	I _{CC}	– 1, 2	15	15			DR LOW	+ mA max
			15	15			DR HIGH (During Conversion)	
	I _{EE}	– 1, 2	15	15				– mA max
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0		Convert, $\overline{\text{HBE}}$, $\overline{\text{LBE}}$, $\overline{\text{DE}}$	+ V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8		Convert, $\overline{\text{HBE}}$, $\overline{\text{LBE}}$, $\overline{\text{DE}}$	+ V max
Digital Input High Current	I _{IH}	– 1, 2	100	100	100		Convert, $\overline{\text{HBE}}$, $\overline{\text{LBE}}$, $\overline{\text{DE}}$ V _{IH} = 5.0V	± μA max
Digital Input Low Current	I _{IL}	– 1, 2	100	100	100		Convert, $\overline{\text{HBE}}$, $\overline{\text{LBE}}$, $\overline{\text{DE}}$ V _{IL} = 0.0V	± μA max
Digital Output Low Voltage	V _{OL}	– 1	0.4	0.4	0.4		I _{OL} = + 3.2mA, $\overline{\text{DR}}$, DB0-DB7	+ V max
		– 2	0.4	0.4	0.4		I _{OL} = + 3.2mA $\overline{\text{DR}}$, DB0-DB9	
Digital Output High Voltage	V _{OH}	– 1	2.4	2.4	2.4		I _{OH} = – 0.5mA, DB0-DB7	+ V min
		– 2	2.4	2.4	2.4		I _{OH} = – 0.5mA, DB0-DB9	

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Convert Pulse Width ⁵	t_{CS}	– 1, 2	500		500	500		ns min
DR Delay Convert ⁵	t_{DSC}	– 1, 2	1.5			1.5		μs max
Data Valid After $\overline{DE}$, $\overline{HBE}$ or $\overline{LBE}$ High ⁶	t_{HD}	– 1, 2	50					ns min
Output Float Delay ⁶	t_{HL}	– 1, 2	200			200		ns max
Data Access Time ⁶	t_{DD}	– 1, 2	250			250		ns max

NOTES

¹ $V_{CC} = +5V$, $V_{EE} = -15V$, analog input through 15Ω resistor to Pin 13, Unipolar configuration.

$T_A = 25^\circ C$ unless otherwise indicated.

Unipolar configuration Pin 16 (Bipolar Offset Control) is grounded.

Bipolar configuration Pin 16 is not connected.

²For – 1 (8-Bit resolution Device), 0.391% of full scale = 1 LSB (least significant bit). For – 2 (10-Bit resolution device), 0.098% of full scale = 1 LSB.

³Minimum resolution for which no missing codes are guaranteed.

⁴– 1 device full scale error guaranteed trimmable with 500Ω potentiometer.

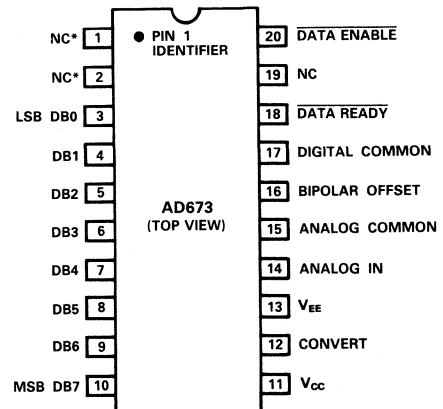
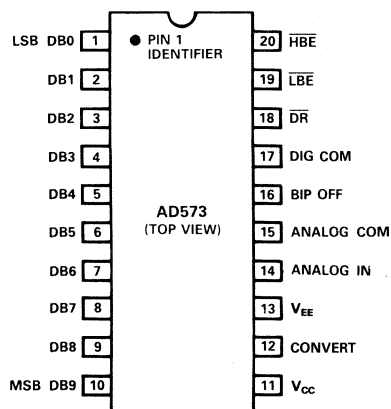
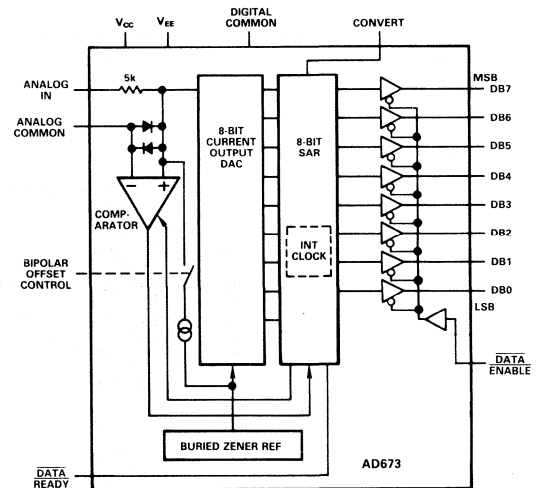
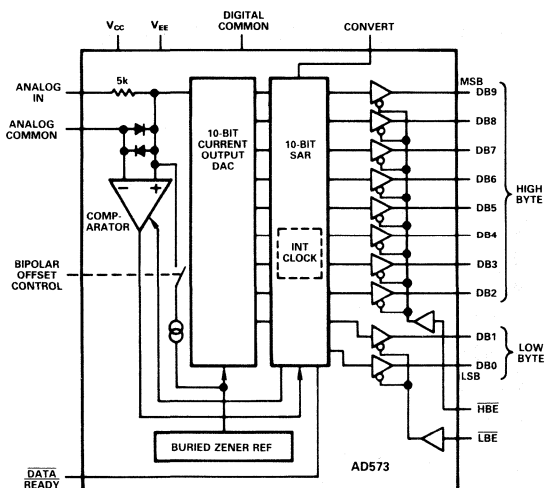
– 2 device full scale error guaranteed trimmable with 200Ω potentiometer.

⁵See Figure 1.

⁶See Figures 2 and 3.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



*PINS 1 & 2 ARE INTERNALLY CONNECTED TO TEST POINTS AND SHOULD BE LEFT FLOATING

AD573/AD673

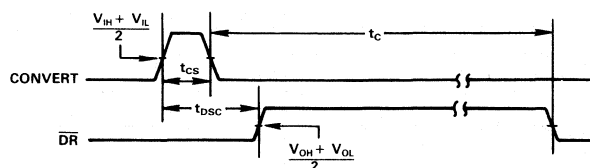


Figure 1. AD573 and AD673 CONVERT Timing

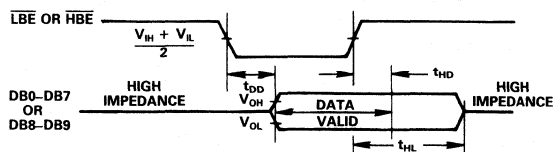


Figure 2. AD573 READ Timing

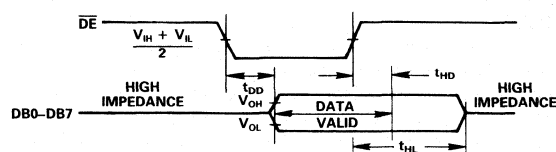


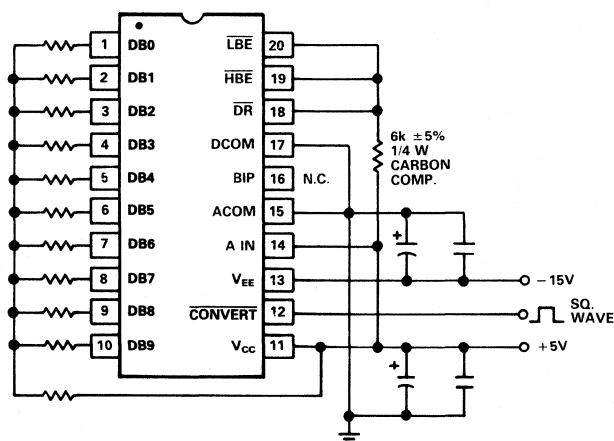
Figure 3. AD673 READ Timing

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574A

1.1 Scope.

This specification covers the detail requirements for a 12-bit resolution A/D converter with complete microprocessor interface and a high performance buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD574AS(X)/883B
-2	AD574AT(X)/883B
-3	AD574AU(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28A	28-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Digital Common	+16.5V
V_{EE} to Digital Common	-16.5V
V_{LOGIC} to Digital Common	+7V
Analog Common to Digital Common	$\pm 1V$
Control Inputs ($\overline{CE}$, $\overline{CS}$, A_O , $12/\overline{8}$, $R/\overline{C}$) to Digital Common	-0.5V to $V_{LOGIC} + 0.5V$
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common	$\pm 16.5V$
$20V_{IN}$ to Analog Common	$\pm 24V$
REF OUT	Indefinite Short to Common Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$ for D-28 or E-28A
 $\theta_{JA} = 60^\circ\text{C/W}$ for D-28 or E-28A

AD574A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Power Dissipation	P _D	– 1, 2, 3	725	725			Tristated Outputs	mW max
Input Resistance	R _{IN}	– 1, 2, 3	3	3			10V Span	kΩ min
			7	7				kΩ max
			6	6			20V Span	kΩ min
			14	14				kΩ max
Internal 10V Reference Output Voltage Error	V _{REF}	– 1, 2	± 20	± 20			Bipolar 1.5mA External Load	mV
		– 3	± 10	± 20		± 10		
Logic Input High ² CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O	V _{IH}	– 1, 2, 3	2.0	2.0				+ V min
			5.5					+ V max
Logic Input Low ² CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O	V _{IL}	– 1, 2, 3	0.5					– V min
			0.8	0.8				+ V max
Logic Input Current CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O	I _{LIN}	– 1, 2, 3	20	20	20		V _{IH} = 5.0V V _{IL} = 0.0V	± μA max
Logic Output High DB11-DB0	V _{OH}	– 1, 2, 3	2.4	2.4	2.4		I _{SOURCE} = 500μA	+ V min
Logic Output Low DB11-DB0, STS	V _{OL}	– 1, 2, 3	0.4	0.4	0.4		I _{SINK} = 1.6mA	+ V max
Three-State Output Leakage DB11-DB0	I _{OLT}	– 1, 2, 3	20	20	20		Outputs Tristated V _{IH} = 5.0V	± μA max
Power Supply Current	I _L	– 1, 2, 3	40	40			Outputs Tristated	mA max
	I _{CC}	– 1, 2, 3	5	5				
	I _{EE}	– 1, 2, 3	30	30				
Full-Scale Calibration Drift	TCA _E	– 1			20			± LSB max
		– 2			10			
		– 3			5			
Linearity	LE	– 1	1	1	1		10V Unipolar, 20V Bipolar Major Transitions	± LSB max
		– 2, 3	1/2	1	1	1/2		
Differential Nonlinearity ³	DNL	– 1	11	11	11		All Codes Tested	Bits min
		– 2, 3	12	11	12	12		
Power Supply Rejection Ratio ⁴	PSRR	– 1	2	2			See Note 5	± LSB max
		– 2, 3	1	2		1		
	PSRR	– 1, 2, 3	1/2	1/2			See Note 6	
	PSRR	– 1	2	2			See Note 7	
		– 2, 3	1	2		1		
Unipolar Offset Error	V _{OSE}	– 1	2	2	4			± LSB max
		– 2, 3	1	2	2	1		
Unipolar Offset Drift	TC _{VOS}	– 1 – 2, 3			2 1			± LSB max
Bipolar Offset Error	B _{POE}	– 1	4	4	8		Bipolar 20V Span	± LSB max
		– 2	4	4	6			
		– 3	2	4	3	2		
Bipolar Offset Drift	TCB _{POE}	– 1			4		Bipolar 20V Span	± LSB max
		– 2			2			
		– 3			1			
Full-Scale Error	A _B	– 1, 2	0.25	0.25			Bipolar 20V Span	± %/FSR max
		– 3	0.125	0.25		0.125		
	A _U	– 1, 2 – 3	0.25 0.125				Unipolar 10V Span	± %/FSR max

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Test Condition ¹	Units
Full-Control Mode¹								
STS Delay from CE	t_{DSC}	-1, 2, 3	400			350	Timing Per Figure 1	ns max
CE Pulse Width	t_{HEC}	-1, 2, 3	300			300	Timing Per Figure 1	ns min
Access Timing (from CE) ⁸	t_{DD}	-1, 2, 3	200			200	Timing Per Figure 2	ns max
Output Float Delay	t_{HL}	-1, 2, 3	100			100	Timing Per Figure 2	ns max
Data Valid After CE Low	t_{HD}	-1, 2, 3	25			25	Timing Per Figure 2	ns min
Stand-Alone Mode¹								
Low R/C Pulse Width	t_{HRL}	-1, 2, 3	250			250	Timing Per Figure 3	ns min
STS Delay from R/C	t_{DS}	-1, 2, 3	600			600	Timing Per Figure 3	ns max
Data Access Time ⁸	t_{DDR}	-1, 2, 3	250			250	Timing Per Figure 3	ns max
Data Valid After R/C Low	t_{HDR}	-1, 2, 3	25			25	Timing Per Figure 3	ns min
Conversion Time	t_C	-1, 2, 3	35			35	To 12 Bits	μs max
			24			24	To 8 Bit	

NOTES

¹ $V_{CC} = +15V$, $V_{EE} = -15V$, $V_{LOGIC} = +5V$, 12/8 connected to V_{LOGIC} , A_0 and $\overline{CS}$ at logic "0", CE at logic "1." 10V unipolar configuration unless otherwise noted.

10V Unipolar: 50 Ω resistor Pin 8 to Pin 10, 50 Ω resistor Pin 12 to ground, analog input to Pin 13.

20V Bipolar: 50 Ω resistor Pin 8 to Pin 12, 50 Ω resistor Pin 8 to Pin 10, analog input to Pin 14.

See Figures 1, 2, and 3 for timing information.

² $V_{IH} = 2.0V$ min and $V_{IL} = 0.8V$ max, guaranteed design limits -55°C to +125°C.

³Minimum resolution for which no missing codes are guaranteed.

⁴Change in unipolar 10V span with full-scale (Code 4095) transition voltage.

⁵Test Conditions for PSRR:

13.5V $\leq V_{CC} \leq 16.5V$, $V_{LOGIC} = 5V$, $V_{EE} = -15V$

11.4V $\leq V_{CC} \leq 12.6V$, $V_{LOGIC} = 5V$, $V_{EE} = -12V$

4.5V $\leq V_{LOGIC} \leq 5.5V$, $V_{CC} = 15V$, $V_{EE} = -15V$

⁷-16.5 $\leq V_{EE} \leq -13.5V$, $V_{LOGIC} = 5V$, $V_{CC} = 15V$

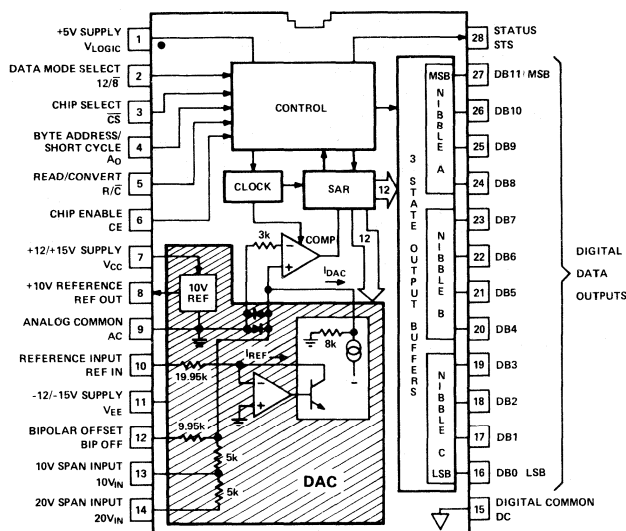
-12.6V $\leq V_{EE} \leq -11.4V$, $V_{LOGIC} = 5V$, $V_{CC} = 12V$

⁸See Figure 4.

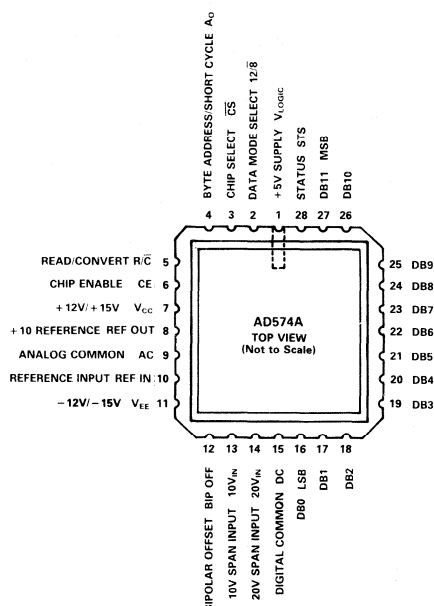
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

D Package (DIP)



E Package (LCC)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

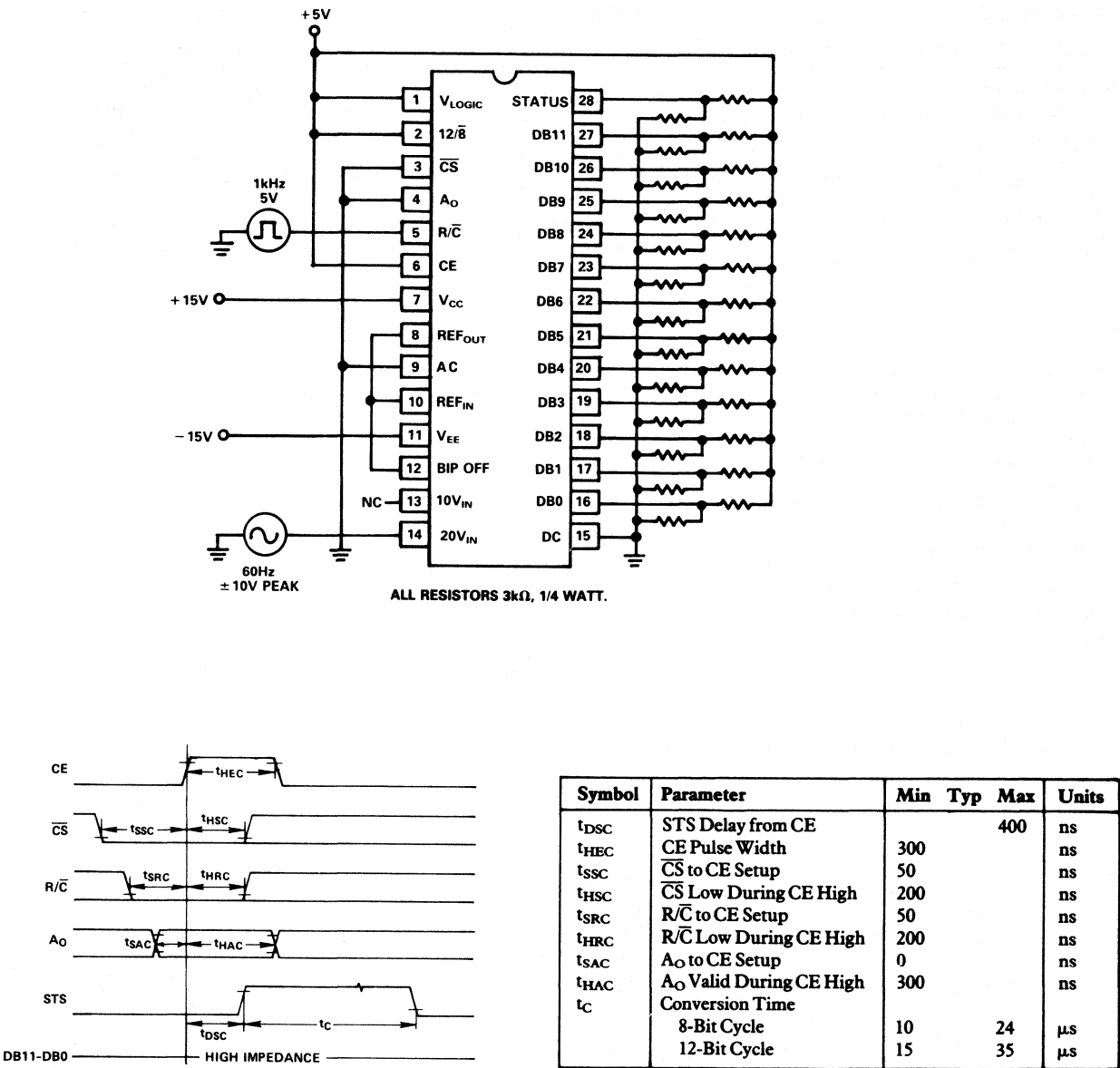
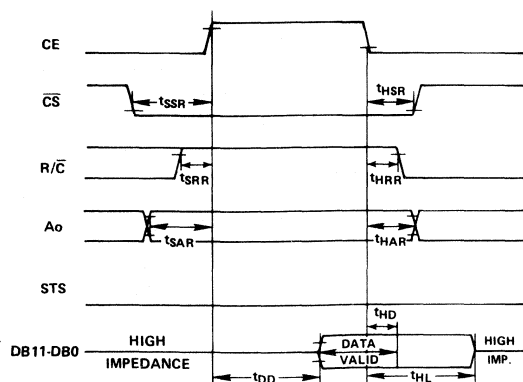


Figure 1. Convert Start Timing

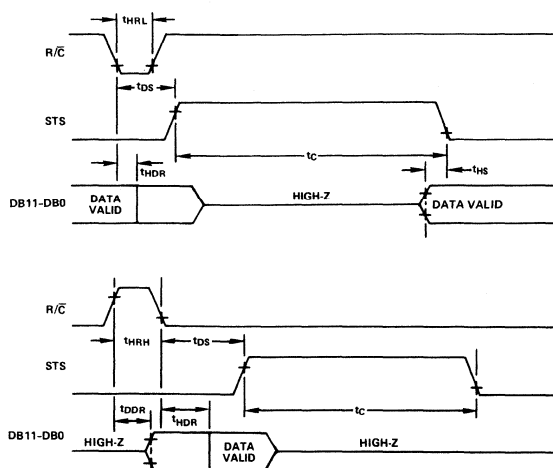


Symbol	Parameter	Min	Typ	Max	Units
t_{DD}^1	Access Time (from CE)			200	ns
t_{HD}^2	Data Valid after CE Low	25			ns
t_{HL}^2	Output Float Delay		100		ns
t_{SSR}	CS to CE Setup	150			ns
t_{SRR}	R/C to CE Setup	0			ns
t_{SAR}	A ₀ to CE Setup	150			ns
t_{HSR}	CS Valid After CE Low	50			ns
t_{HRR}	R/C High After CE Low	0			ns
t_{HAR}	A ₀ Valid After CE Low	50			ns

¹ t_{DD} is measured with the load circuit of Figure 4 and defined as the time required for an output to cross 0.4V to 2.4V.

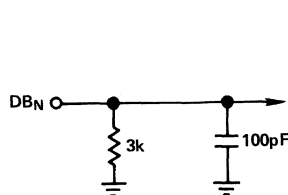
² t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 5.

Figure 2. Read Timing

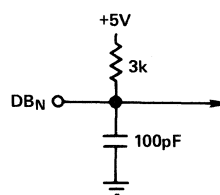


Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/C Pulse Width	250			ns
t_{DS}	STS Delay from R/C			600	ns
t_{HDR}	Data Valid After R/C Low	25			ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/C Pulse Width	300			ns
t_{DDR}	Data Access Time		250		ns

Figure 3. Stand-Alone Mode Timing

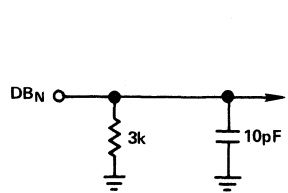


a. High-Z to Logic 1

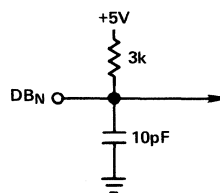


b. High-Z to Logic 0

Figure 4. Load Circuit for Access Timing Test



a. Logic 1 to High-Z



b. Logic 0 to High-Z

Figure 5. Load Circuit for Output Float Delay Test

1.1 Scope.

This specification covers the detail requirements for a high precision 2.5V IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD580SH/883B
- 2	AD580TH/883B
- 3	AD580UH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-03A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{CC} to Ground	40V
Power Dissipation	350mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

AD580 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	– 1, 2, 3	1.5	1.5				+ mA max
Output Voltage Error	V _{OUT}	– 1	25	25				± mV max
		– 2, 3	10	25		10		
Line Regulation	VR _{LINE1}	– 1	6	6			V _{CC} = 7V to 30V	± mV max
		– 2, 3	2	6		2		
Line Regulation	VR _{LINE2}	– 1	3	3			V _{CC} = 4.5V to 7V	± mV max
		– 2, 3	1	3		1		
Load Regulation	VR _{LOAD}	– 1, 2, 3	10	10			I _L = 0mA to 10mA	± mV max
Output Voltage Temperature Coefficient	TCV _{OUT}	– 1	25		25		T _A = – 55°C to + 125°C	± mV max
		– 2	11		11			
		– 3	4.5		4.5			

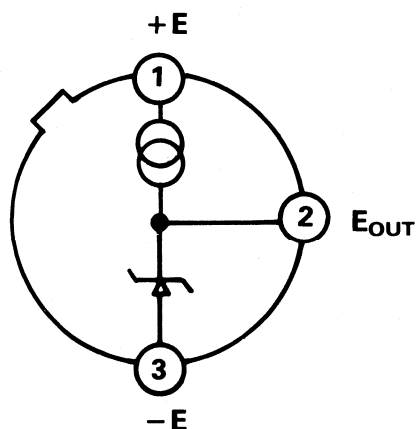
NOTE

¹V_{CC} = + 15V, I_L = 0mA, unless otherwise indicated.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Bottom View



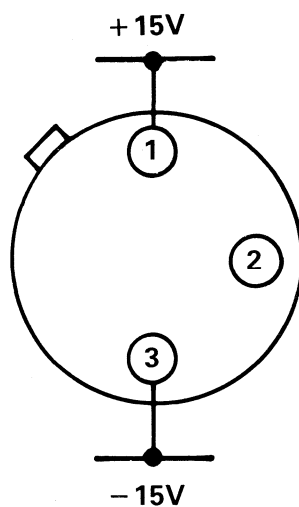
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

Bottom View



1.1 Scope.

This specification covers the detail requirements for a high precision 10 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD581SH/883B
-2	AD581TH/883B
-3	AD581UH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-03B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{CC} to Ground	40V
Power Dissipation (25°C)	600mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

AD581— SPECIFICATIONS

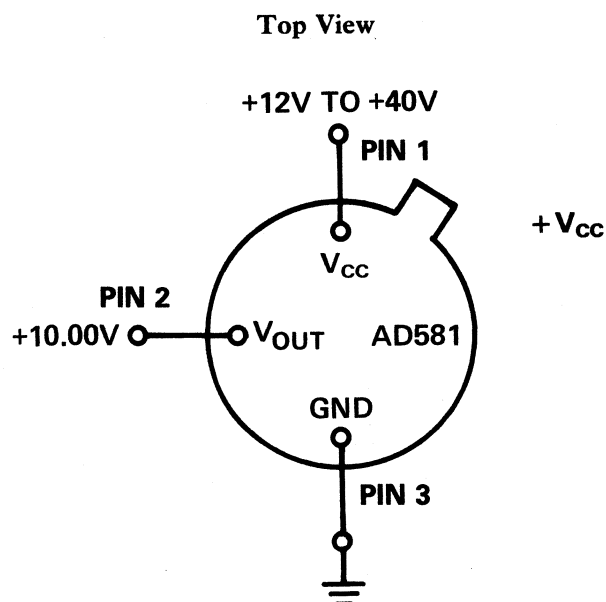
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	- 1, 2, 3	1.0	1.0				+ mA max
Output Voltage Error	V _{OUT}	- 1	30	30				± mV max
		- 2	10	30		10		
		- 3	5	30		5		
Line Regulation	V _{RLINE1}	- 1, 2, 3	3.0	3.0			V _{CC} = 15V to 30V	± mV max
Line Regulation	V _{RLINE2}	- 1, 2, 3	1.0	1.0			V _{CC} = 13V to 15V	± mV max
Load Regulation	V _{RLOAD}	- 1, 2, 3	500	500			I _L = 0mA to 5mA	± μV/mA
Output Voltage Temperature Coefficient	ΔV _O /ΔT	- 1	30		30		T _A = 25°C to 125°C	± mV max
		- 2	15		15		T _A = 25°C to - 55°C	
		- 3	10		10			
Output Current Source	I _{OUT}	- 1, 2, 3	10				T _A = + 25°C	mA min
			5				T _{min} to T _{max}	mA min
Output Current Sink	I _{OUT}	- 1, 2, 3	0.2				+ 80°C to + 125°C	mA min
			5.0				- 55°C to + 80°C	mA min
Output Short Circuit Current	I _{OS}	- 1, 2, 3	55	55				- mA max

NOTE

¹V_{CC} = + 15V, I_L = 0mA, unless otherwise indicated.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

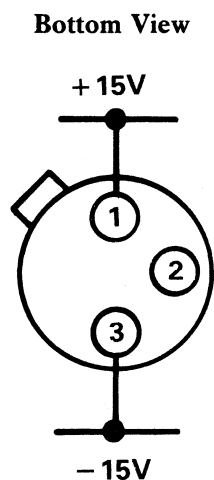


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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1.1 Scope.

This specification covers the detail requirements for a monolithic sample-and-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD582S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-14	14-Pin DIP
H	H-10A	10-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supplies ($+V_S$, $-V_S$)	$\pm 22\text{V}$
Logic Inputs	$\pm V_S$
Logic Inputs, Differential Voltage	$+15\text{V}/-6\text{V}$
Analog Inputs	$\pm V_S$
Analog Inputs, Differential Voltage	30V
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 25^\circ\text{C}/\text{W}$ for D-14
θ_{JA}	$= 95^\circ\text{C}/\text{W}$ for D-14
θ_{JC}	$= 25^\circ\text{C}/\text{W}$ for H-10A
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-10A

AD582 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Logic Input High	V _{IH}	– 1	2	2	2		See Notes 2 & 3	V min
Logic Input Low	V _{IL}	– 1	0.8	0.8	0.8		See Notes 2 & 4	V max
Logic Current High	I _{IH}	– 1	5	5			See Notes 2 & 3	μA max
Logic Current Low	I _{IL}	– 1	1	1			See Notes 2 & 4	μA max
Operating Voltage	V _S	– 1	22	22			Open Loop Swing V _{IN} = ± 100mV	± V max
Supply Current	I _S	– 1	4.5	4.5				mA max
Power Supply Rejection	PSR	– 1	60	60			See Note 5	dB min
Droop Current	I _{DRP}	– 1	0.1	0.1	150		C _H = 200pF	nA max
Charge Transfer	QT	– 1	5	5			C _H = 200pF	pC max
Open Loop Gain	A _{OL}	– 1	25	25			V _{OUT} = 20V p-p, R _L = 2kΩ	k min
Common-Mode Rejection	CMR	– 1	60	60			V _{CM} = 20V p-p	dB min
Output Short Circuit Current	I _{SC}	– 1	40	40				± mA max
Offset Voltage	V _{OS}	– 1	6	6	8			± mV max
Bias Current	I _B	– 1	3	3				± μA max
Offset Current	I _{OS}	– 1	300	300	400			± nA max

NOTES

¹V_S = ± 15V, C_H = 1000pF, R_L = infinite, A = 1 unless otherwise noted.

²– Logic = 0V.

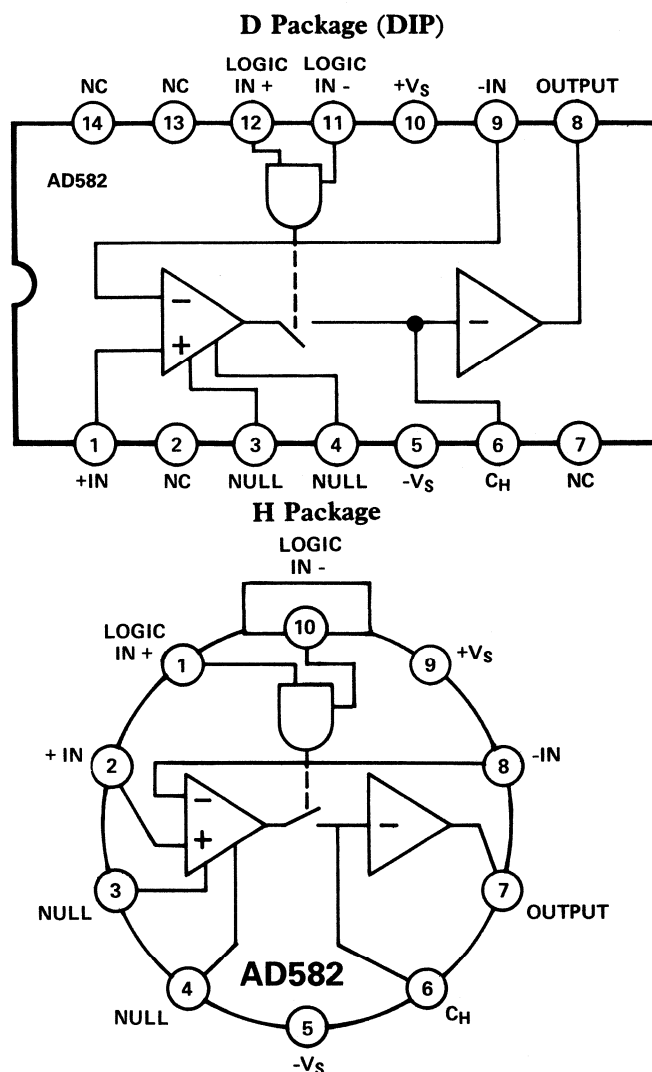
³Hold mode.

⁴Sample mode.

⁵ΔV_S = 5V, Sample mode.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

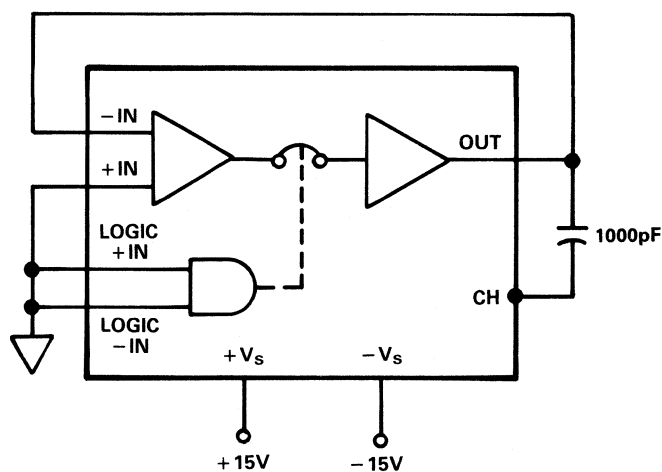


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (60).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a pin programmable precision voltage reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD584S(X)/883B
– 2	AD584T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000:

(X)	Package	Description
H	H-08A	8-Pin Metal Package
E	E-20A	20-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{CC} to Ground	40V
Power Dissipation (25°C)	600mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 40^\circ\text{C/W}$ for H-08A
θ_{JA}	$= 150^\circ\text{C/W}$ for H-08A
θ_{JC}	$= 35^\circ\text{C/W}$ for E-20A
θ_{JA}	$= 120^\circ\text{C/W}$ for E-20A

AD584 – SPECIFICATIONS

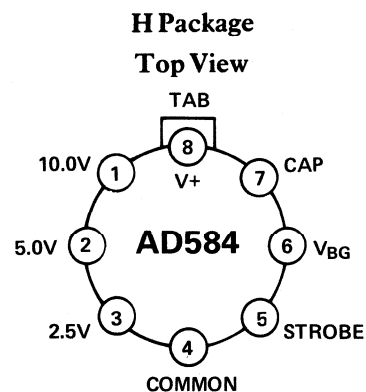
Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	– 1, 2	1.0	1.0				mA max
Output Voltage Error	V _{OUT1}	– 1	30	30				± mV max
		– 2	10	30		10		
Output Voltage Error	V _{OUT2}	– 1	20	20			7.5V Output	± mV max
		– 2	8	20		8		
Output Voltage Error	V _{OUT3}	– 1	15	15			5.0V Output	± mV max
		– 2	6	15		6		
Output Voltage Error	V _{OUT4}	– 1	7.5	7.5			2.5V Output	± mV max
		– 2	3.5	7.5		3.5		
Line Regulation	VR _{LINE1}	– 1, 2	0.005	0.005	0.010 ²		V _{OUT} = 2.5V, 5.0V, 7.5V, 10.0V, V _{OUT} + 2.5V ≤ V _{CC} < 15V	± %/V max
Line Regulation	VR _{LINE2}	– 1, 2	0.002	0.002	0.005 ²		V _{OUT} = 2.5V, 5.0V, 7.5V, 10.0V, 15V ≤ V _{CC} ≤ 30V	± %/V max
Load Regulation	VR _{LOAD1}	– 1, 2	50	50	100		I _L = 0 to 5mA	± ppm/mA max
Load Regulation	VR _{LOAD2}	– 1, 2	50	50	100		I _L = 0 to 5mA, 7.5V Output	± ppm/mA max
Load Regulation	VR _{LOAD3}	– 1, 2	50	50	100		I _L = 0 to 5mA, 5.0V Output	± ppm/mA max
Load Regulation	VR _{LOAD4}	– 1, 2	50	50	100		I _L = 0 to 5mA, 2.5V Output	± ppm/mA max
Output Short Circuit Current	I _{OS}	– 1, 2	55	55			10V Output Grounded	– mA max
Output Voltage Temperature Coefficient	DV _{OUT1} dT	– 1			30		T _A = 25°C to 125°C	± ppm/°C max
		– 2			15		T _A = 25°C to – 55°C	
Output Voltage Temperature Coefficient	DV _{OUT2} dT	– 1			30		T _A = 25°C to 125°C	± ppm/°C max
		– 2			15		T _A = 25°C to – 55°C 7.5V Output	
Output Voltage Temperature Coefficient	DV _{OUT3} dT	– 1			30		T _A = 25°C to 125°C	± ppm/°C max
		– 2			15		T _A = 25°C to – 55°C 5.0V Output	
Output Voltage Temperature Coefficient	DV _{OUT4} dT	– 1			30		T _A = 25°C to 125°C	± ppm/°C max
		– 2			20		T _A = 25°C to – 55°C 2.5V Output	
Output Current Source @ 25°C Source T _{min} to T _{max} Sink T _{min} to T _{max}	I _{OUT}		10	10				mA min
	I _{OUT}		5		5			mA min
	I _{OUT}		200					μA min

NOTES

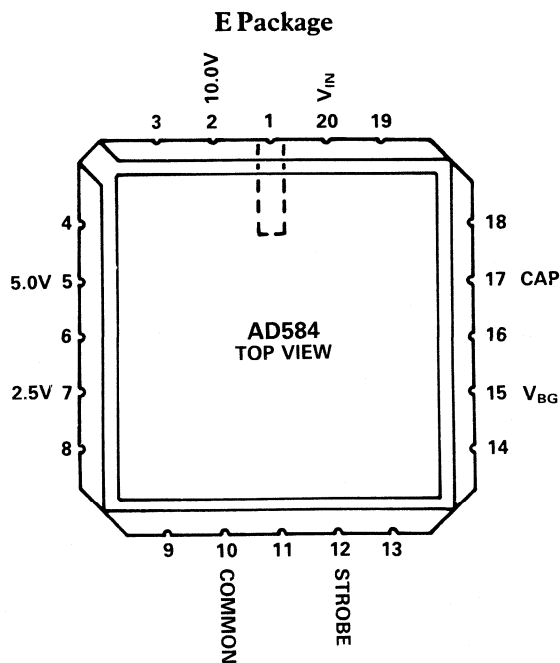
¹V_{CC} = + 15V, 10V output, no load unless otherwise indicated.

²10V output only.

Table 1.



***THE 2.5V TAP IS USED INTERNALLY AS A BIAS POINT
AND SHOULD NOT BE CHANGED BY MORE THAN 100mV
IN ANY TRIM CONFIGURATION.**



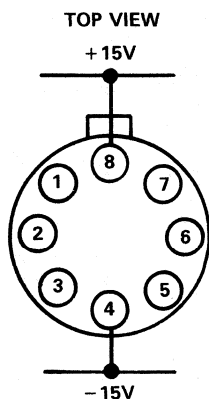
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

AD584

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTES

1. DECOUPLE ONCE PER BOARD WITH $1\mu\text{F}$, 50V CAPACITORS FROM $\pm 15\text{V}$ TO GROUND.
2. I TYPICAL = 0.6mA/DEVICE
SUPPLY MAXIMUM = 1.0mA/DEVICE.

1.1 Scope.

This specification covers the detail requirements for a complete monolithic sample-and-hold circuit with internal holding capacitor and matched application resistors.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD585S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-14	14-Pin Cerdip
E	E-20A	20-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supplies ($+V_S$, $-V_S$)	$\pm 18\text{V}$
Logic Inputs	$\pm V_S$
Analog Inputs	$\pm V_S$
R_{IN} , R_{FB} Pins	$\pm V_S$
Output Short Circuit to Ground	Indefinite
TTL Logic Reference Short Circuit to Ground	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

AD585 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Test Condition ¹	Units
Offset Voltage	V _{OS}	– 1	2	3	3	2		V _{OUT} = 0V	± mV max
Bias Current ²	I _B	– 1	2	2	50			V _{IN} = 0V	± nA max
TTL Reference Output ³	V _{I,REF}	– 1	0.2	0.2	0.6			50µA Load	± V max
Logic Input High Voltage	V _{IH}	– 1	2.0	2.0	2.0			Hold = V _{I,REF}	V min
Logic Input Low Voltage	V _{IL}	– 1	0.8	0.8	0.7			Hold = V _{I,REF}	– V max
Logic Input Current	I _{IL}	– 1	50	50	50			V _S = 18V	µA max
Supply Current	I _{SS}	– 1	10	10	10			R _L = Infinite	mA max
Power Supply Rejection	PSRR	– 1	70	70				+ V _S = 5V to 18V – V _S = – 12V to – 18V	dB min
Acquisition Time	t _{ACQ}	– 1	3				3	10V step to 0.01%	µs max
Acquisition Time	t _{ACQ}	– 1	5					20V step to 0.01%	µs max
Droop Rate ⁴	V _{DRP}	– 1	1			1		V _{IN} = 0V	mV/ms max
Sample-to-Hold Offset	SH _{OS}	– 1	3			3		V _{IN} = 0V	mV max
Application Resistor Mismatch	ΔRM	– 1	0.3	0.3	0.3				% max
Common-Mode Rejection	CMRR	– 1	80	80	77			V _{CM} = ± 10V	dB min
Slew Current ⁵	I _{SL}	– 1	850		600	850			µA min
Output Resistance ⁶	R _{OUT}	– 1	0.05	0.05	0.1			I _{OUT} = ± 10mA	Ω max
Output Current	I _{OUT}	– 1	12 50	12 50				R _L = 100Ω	mA min mA max

NOTES

¹V_S = ± 15V, C_H = Internal, R_L = Infinite, A = + 1 unless otherwise noted.

²Not tested at – 55°C.

³Nominally 1.4V.

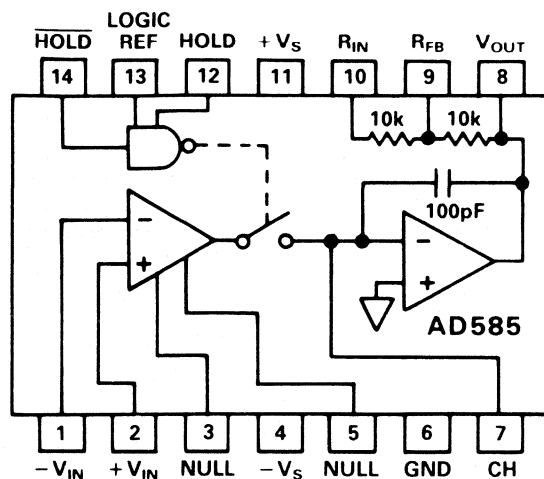
⁴Doubles every 10°C.

⁵V_{OUT} = 20V p-p. Slew rate = Slew Current/C_{II}.

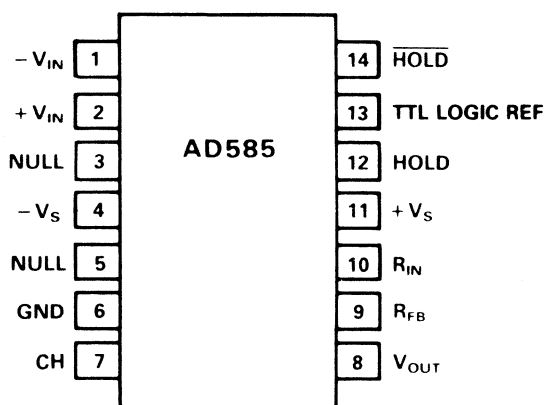
⁶Tested in sample mode.

Table 1.

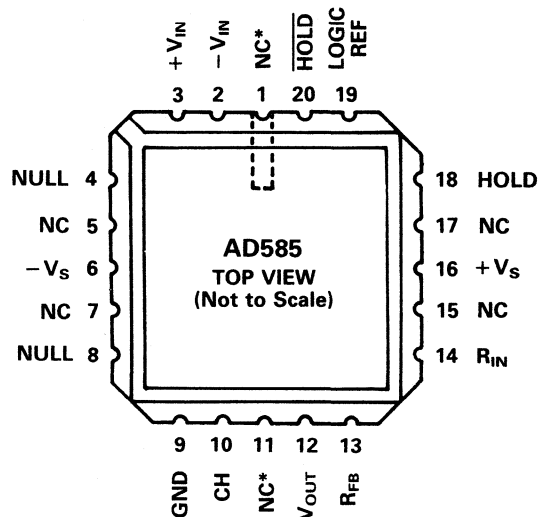
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)



*PERFORMANCE IS ENHANCED IF PINS 1 AND 11 ARE CONNECTED TO GROUND.

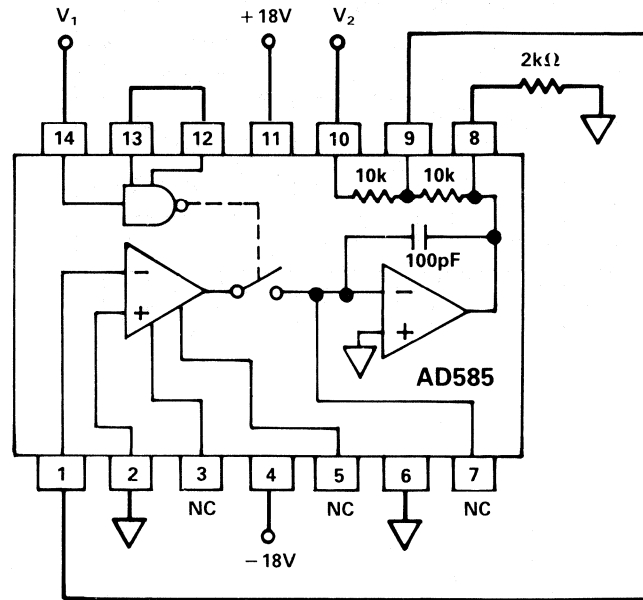
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (60).

AD585

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



$V_1 = 0 \text{ TO } 5\text{V}, 1\text{kHz SQUARE WAVE.}$
 $V_2 = 7\text{V rms, } F = 60\text{Hz}$

1.1 Scope.

This specification covers the detail requirements for a high precision 5 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD586SQ/883B
-2	AD586TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{IN} to Ground	+ 36V
Power Dissipation	500mW
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering 10secs)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

AD586 – SPECIFICATIONS

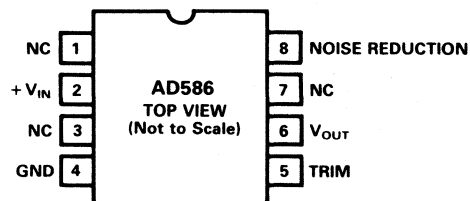
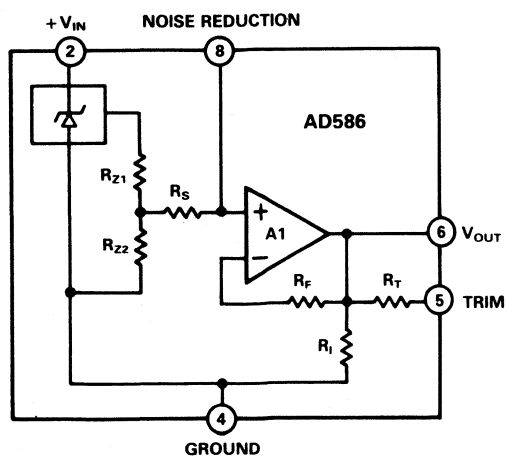
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	– 1, 2	3	3				+ mA max
Output Voltage Error	V _{OUT}	– 1	10	10				± mV max
		– 2	2.5	10		2.5		
Gain Adjustment	V _{ADJ}	– 1, 2	+ 300 – 100	+ 300 – 100				mV min
Line Regulation	VR _{LINE}	– 1, 2	150	150	150		11.4V ≤ V _{IN} ≤ 36V	± μV/V max
Load Regulation, Sourcing	VR _{LOAD}	– 1, 2	150	150	150		I _L = 0 to 10mA	± μV/mA max
Load Regulation, Sinking	I _{OUT}	– 1, 2	400	400			I _L = – 10 to 0mA	± μV/mA max
Output Voltage Temperature Coefficient	DV _{OUT} /dT	– 1	20		20		T _A = – 55°C to + 125°C	± ppm/°C max
		– 2	10		10			
Output Short-Circuit Current	I _{OS}	– 1	50	50			To Ground	+ mA max

NOTE

¹T_A = + 25°C; V_{CC} = + 15V unless otherwise stated.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

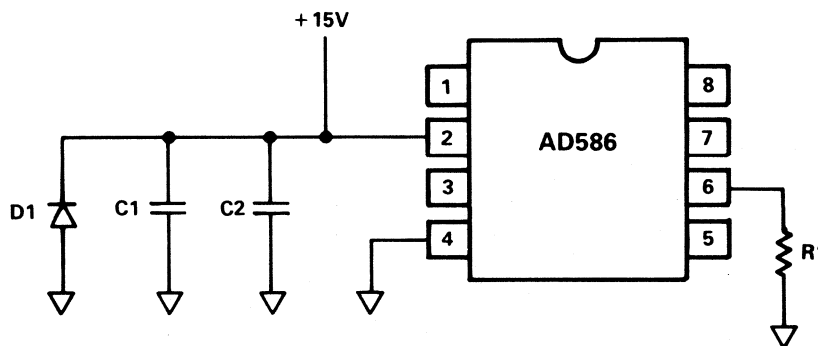


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE: D1 = MR-820
C1 = 0.1 μ F
C2 = 47 μ F
R1 = 500 Ω 1/2 WATT AT 25°C

10011A

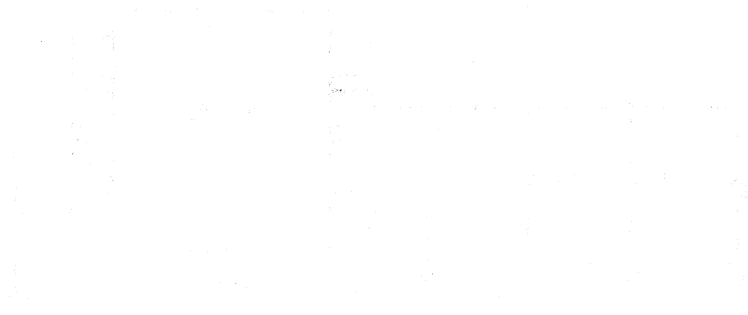
Approximate location of the ...



Approximate location of the ...

Approximate location of the ...

Approximate location of the ...



Approximate location of the ...

1.1 Scope.

This specification covers the detail requirements for a high precision 10 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD587SQ/883B
-2	AD587TQ/883B
-3	AD587UQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{IN} to Ground	+ 36V
Power Dissipation	500mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10secs)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

AD587 — SPECIFICATIONS

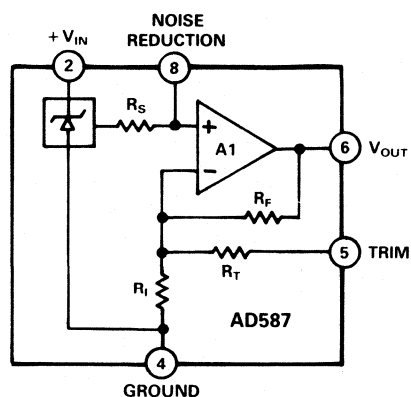
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	–1, 2, 3	4	4				+ mA max
Output Voltage Error	V _{OUT}	–1	10	10				± mV max
		–2	5	10		5		
		–3	5	10		5		
Output Voltage Temperature Coefficient	V _{OUT} /dT	–1	20		20		T _A = –55°C to +125°C	± ppm/°C max
		–2	10		10			
		–3	5		5			
Gain Adjustment	V _{ADJ}	–1, 2, 3	+300	+300				mV min
			–100	–100				
Line Regulation	VR _{LINE}	–1, 2, 3	100	100	100		13.5V ≤ V _{IN} ≤ 36V	± μV/V max
Load Regulation, Sourcing	VR _{LOAD}	–1, 2, 3	100	100	100		I _L = 0 to 10mA	± μV/mA max
Load Regulation, Sinking	I _{OUT}	–1, 2, 3	100	100	100		I _L = –10 to 0mA	± μV/mA max
Output Short-Circuit Current	I _{OS}	–1, 2, 3	50	50			To Ground	+ mA max
Output Short-Circuit Current	I _{OS}	–1, 2, 3	50	50			To V _{IN}	– mA max

NOTE

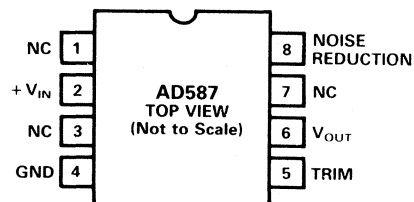
¹T_A = +25°C; V_{CC} = +15V unless otherwise stated.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



NOTE: MAKE NO CONNECTIONS TO PINS 1, 3, AND 7.

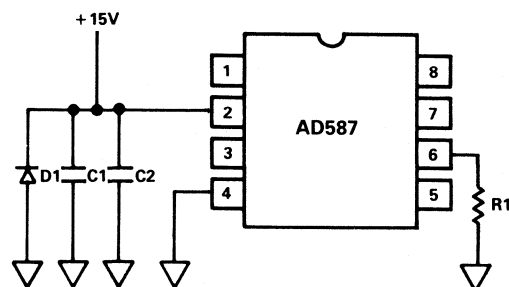


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE: D1 = MR-820
C1 = 0.1 μ F
C2 = 47 μ F
R1 = 1k Ω 1/2 WATT AT 25°C

1.1 Scope.

This specification covers the detail requirements for a monolithic high precision voltage reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD588SD/883B
-2	AD588TD/883B
-3	AD588SE/883B
-4	AD588TE/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16 and E-20

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_S$ to $-V_S$	$+36\text{V}$
Power Dissipation	600mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 90^\circ\text{C/W}$

AD588 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Output Voltage Error +10V, -10V Outputs		-1, 3	5	5		3	A ₃ = +10V	± mV max
		-2, 4	3	5			A ₄ = -10V	
Output Voltage Error +5V, -5V Outputs		-1, 3	5	5		3	A ₃ = +5V	± mV max
		-2, 4	3	5			A ₄ = -5V	
Tracking Mode	V _{SYM}	-1, 2, 3, 4	1.5	1.5			V _{OUT} = +5V, -5V	± mV
Output Voltage Drift	D _{VO} /DT	-1, 3	6		6		V _{OUT} = +10V	± ppm/°C
		-2, 4	4		4			
Gain Adjust	Gain ADJ	-1, 2, 3, 4	4	4				± mV
Balance Adjust	Bal ADJ	-1, 2, 3, 4	4	4				± mV
Line Regulation ²	VR _{LINE}	-1, 2, 3, 4	200	200	200		V _{OUT} = +10V, -10V, +5V, -5V	± μV/V
Load Regulation	VR _{LOAD1}	-1, 2, 3, 4	50	50	50		V _{OUT} = +10V 0 ≤ I _{OUT} ≤ 10mA	μV/mA
Load Regulation	VR _{LOAD2}	-1, 2, 3, 4	50	50	50		V _{OUT} = -10V -10 ≤ I _{OUT} ≤ 0mA	μV/mA
Supply Current	I _{CC}	-1, 2, 3, 4	10	10	10		V _{OUT} = +10V	mA
Supply Current	I _{EE}	-1, 2, 3, 4	10	10	10		V _{OUT} = +10V	- mA

NOTE

¹V_{CC} + 15V, V_{EE} = -15V, Pin 4 (A₃ IN) connected to Pin 6 (V_{HIGH}), Pin 13 (A₄ IN) connected to Pin 8 (V_{LOW}).

²13.5V ≤ V_{CC} ≤ 18V, -13.5V ≤ V_{EE} ≤ -18V.

Table 1.

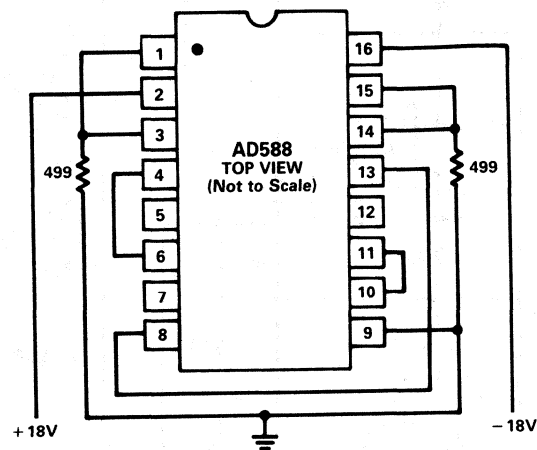


This microcircuit is covered by technology group (59).

AD588

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision 1.2 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD589SH/883B
- 2	AD589TH/883B

1.2.3 Case Outline.

See Figure 1, package outline: H-2A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Current to Ground	10mA
Reverse Current	10mA
Power Dissipation (25°C)	125mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

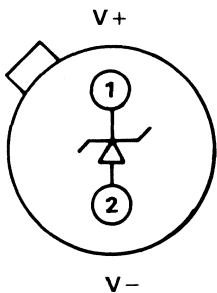
AD589 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition	Units
Output Voltage Error	V_{OUT}	- 1, 2 - 1, 2 - 1, 2	25 30 30	25 30 30			$V = 1.225V, I_{IN} = 500\mu A$ $I_{IN} = 50\mu A$ $I_{IN} = 5mA$	$\pm mV \text{ max}$
Output Voltage Change vs. Current	$\Delta V_O / \Delta I_{IN}$	- 1, 2	5	5	7.5		$50\mu A \leq I_{IN} \leq 5mA$	$\pm mV \text{ max}$
Output Voltage Temperature Coefficient	$\Delta V_O / \Delta T$	- 1 - 2	100 50		100 50		$T_A = +25^\circ C \text{ to } +125^\circ C$ $T_A = +25^\circ C \text{ to } -55^\circ C$	$\pm ppm/^\circ C \text{ max}$
Dynamic Output Resistance	R_O	- 1, 2	2	2	4		$450\mu A \leq I_{IN} \leq 550\mu A$	$\Omega \text{ max}$

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Bottom View



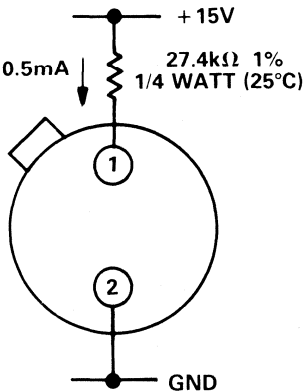
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

Bottom View



BOTTOM VIEW

1.1 Scope.

This specification covers the requirements for a two-terminal monolithic temperature transducer which produces an output current proportional to absolute temperature (PTAT).

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD590J(X)/883B
-2	AD590K(X)/883B
-3	AD590L(X)/883B
-4	AD590M(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: F-2A or H-3A.

(X)	Package	Description
F	F-2A	2-Pin Flat Pack
H	H-3A	3-Pin Metal Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Forward Voltage (E^+ to E^-)	+44V
Reverse Voltage (E^+ to E^-)	-20V
Breakdown Voltage (Case to E^+ or E^-)	$\pm 200\text{V}$
Rated Performance Temperature Range	-55°C to $+150^\circ\text{C}$
Storage Performance Temperature Range	-65°C to $+155^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

MEDIUM	$\theta_{JC} + \theta_{CA} (^\circ\text{C}/\text{watt})$		$\tau \text{ sec}^1$	
	H ²	F ²	H ²	F ²
Aluminum Block	30	10	0.6	0.1
Stirred Oil ³	42	60	1.4	0.6
Moving Air ⁴				
With Heat Sink	45	—	5.0	—
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	—	108	—
Without Heat Sink	480	650	60	30

NOTES

¹The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

²H - 3-pin can; F - 2-pin flat pack.

³ τ is dependent upon velocity of oil; average of several velocities listed above.

⁴Air velocity $\approx 9\text{ft}/\text{sec}$.

AD590 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Ambient Error	E	-1	5.0	5.0		5.0	Normal Output Current is 298.15µA @ +25.00°C	± °C max
		-2	2.5	5.0		2.5		
		-3	1.0	5.0		1.0		
		-4	0.5	5.0		0.5		
Absolute Error	E _A	-1	10.0		10.0		-55°C to +150°C without External Calibration	± °C max
		-2	5.5		5.5			
		-3	3.0		3.0			
		-4	1.7		1.7			
Calibrated Absolute Error	E _C	-1	3.0		3.0		-55°C to +150°C with Ambient Error (E) Set to Zero ²	
		-2	2.0		2.0			
		-3	1.6		1.6			
		-4	1.0		1.0			
Nonlinearity	NL	-1	1.5		1.5		-55°C to +150°C with Ambient Error (E) Set to Zero ²	± °C max
		-2	0.8		0.8			
		-3	0.4		0.4			
		-4	0.3		0.3			
Repeatability	RPT	-1, 4	0.1				Max Deviation between +25°C Readings after Temp. Cycling between -55°C and +150°C	± °C
Long-Term Drift	ΔE/ΔT	-1, 4	0.1				Constant +5V; Constant +125°C	± °C/Month
Power Supply Rejection Ratio	PSRR	-1, 4	1.0				+4V ≤ V _S ≤ +5V	°C/V max
		-1, 4	0.4				+5V ≤ V _S ≤ +15V	
		-1, 4	0.2				+15V ≤ V _S ≤ +30V	
Power Supply Voltage Range	V _S	-1, 4	+4					V min
		-1, 4	+30					V max

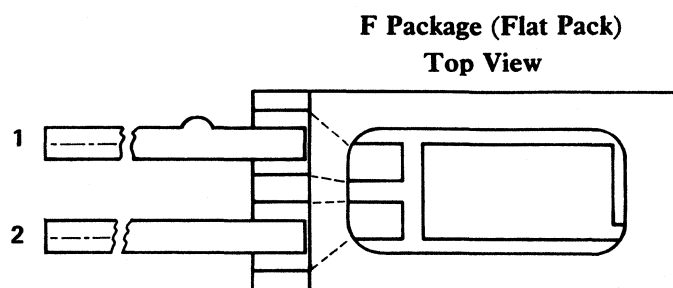
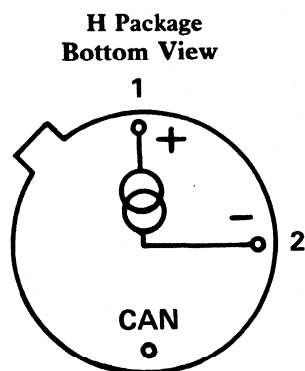
NOTES

¹T_A = +25°C, V_S = ±5V unless otherwise specified.

²See Figure 1.

Table 1.

3.2.1 Functional Block Diagram and Pin Assignments.

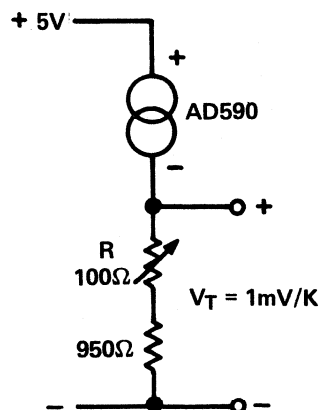
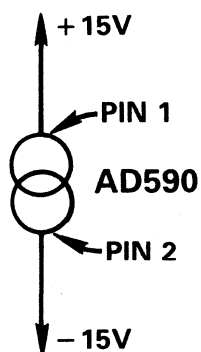


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

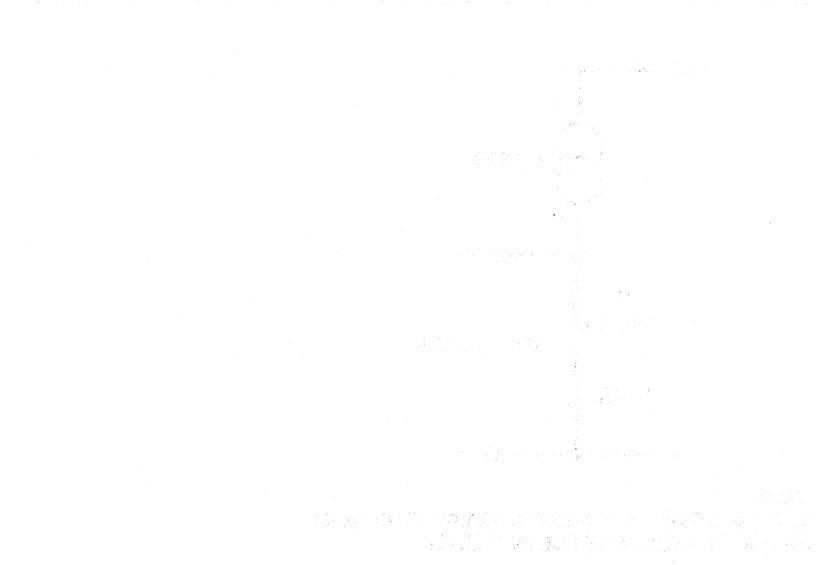
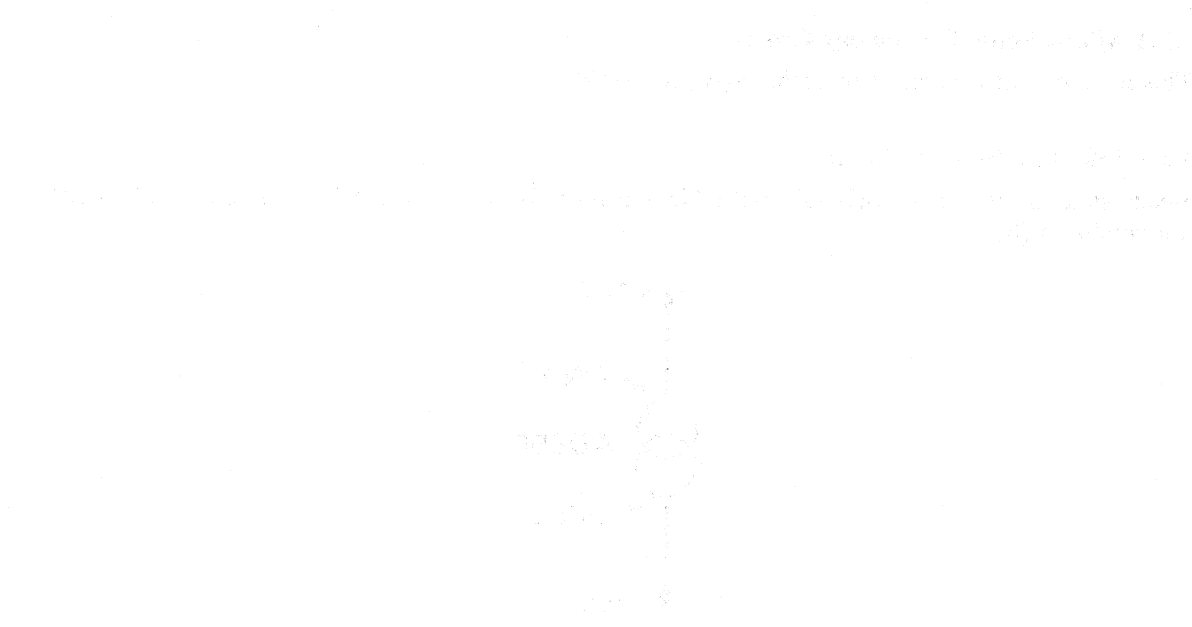
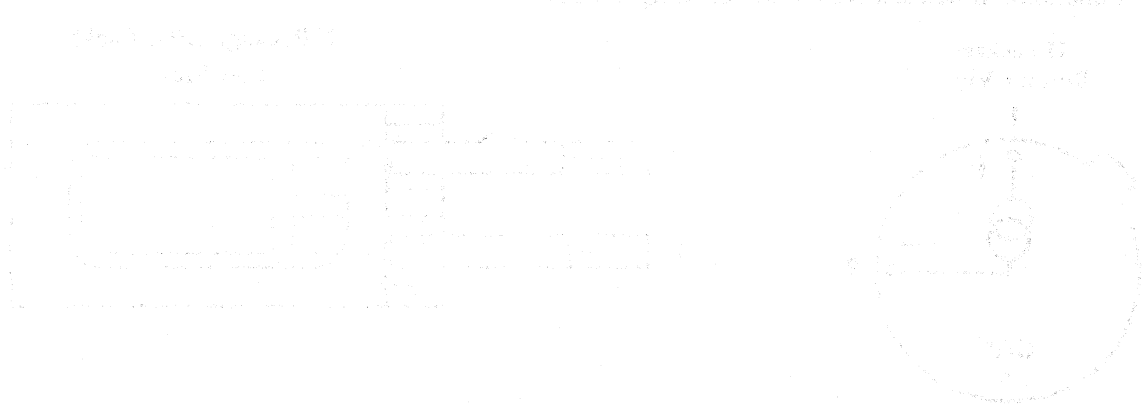
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE
 V_S ACROSS DEVICE MUST REMAIN CONSTANT
OR PSRR ERROR MUST BE INCLUDED.

Figure 1. One Temperature Trim

0200



1.1 Scope.

This specification covers the detail requirements for a monolithic LVDT signal conditioner.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
--1	AD598SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package Description

D-20 20-Lead Side Brazed Ceramic DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Total Supply Voltage $+V_S$ to $-V_S$	36 V
Power Dissipation Up to $+65^\circ\text{C}$	1.2 W
Derates above $+65^\circ\text{C}$	12 mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 85^\circ\text{C/W}$

AD598 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Signal Output Voltage Range		-1	11	11	11		± V min
Signal Output Current		-1	5	5	5		± mA min
Signal Output Nonlinearity ²		-1	500	500	500		± ppm of FS max
Signal Output Gain Error ³		-1	1	1			± % of FS max
Signal Output Gain Drift		-1			50		± ppm/°C of FS max
Signal Output Offset ⁴		-1		1			± % of FS max
Signal Output Offset Drift		-1			50		± ppm/°C of FS max
Signal Output PSRR Gain		-1		400	400	± 12 V dc to ± 18 V dc	± ppm/V max
Signal Output PSRR Offset		-1		200	200	± 12 V dc to ± 18 V dc	± ppm/V max
Signal Output CMRR Gain		-1		200	200	± 3 V dc	± ppm/V max
Signal Output CMRR Offset		-1		200	200	± 3 V dc	± ppm/V max
Excitation Output Voltage ⁵		-1		1.2		R1 = Open, 2.5 kHz	V rms min
				20		R1 = 487 Ω, 2.5 kHz	V rms max
Excitation Output Current		-1	30				mA rms min
Signal Input Bias Current		-1	5				μA max
Signal Reference Bias Current		-1	10				μA max
Power Supply Operating Voltage		-1	36				V max
Power Supply Current		-1		15	18	No Load at Signal and Excitation Outputs	mA max

NOTES

¹T_A = +25°C, V_S = ±15 V dc. C1 = 0.015 μF, R2 = 80 kΩ, R_L = 2 kΩ, unless otherwise noted. See Figure 1.

²Nonlinearity of the AD598 only in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD598 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

³From T_{min} to T_{max} the overall error due to the AD598 alone is determined by combining gain error, gain drift and offset drift. For example, the worst-case overall error for the AD598SD/883B from T_{min} to T_{max} is calculated as follows: Overall error = gain error at +25°C (±1% full scale) + gain drift from +25°C to +125°C (50 ppm/°C of FS × +100°C) + offset drift from +25°C to +125°C (50 ppm/°C of FS × +100°C) = ±2% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale. Full scale is defined as the voltage difference between the maximum positive and the maximum negative output.

⁴This offset refers to the (V_A-V_B)/(V_A+V_B) input spanning a full-scale range of ±1. [For (V_A-V_B)/(V_A+V_B) to equal +1, V_B must equal zero volts; and correspondingly for (V_A-V_B)/(V_A+V_B) to equal -1, V_A must equal zero volts. Note that offset errors do not allow accurate use of zero magnitude inputs; practical inputs are limited to 100 mV rms.] The ±1 span is a convenient reference point to define offset referred to input. For example, with this input span a value of R2 = 20 kΩ would give V_{OUT} span a value of ±10 volts. Caution, most LVDTs will typically exercise less of the (V_A-V_B)/(V_A+V_B) input span and thus require a larger value of R2 to produce the ±10 V output span. In this case the offset is correspondingly magnified when referred to the output voltage. For example, a Schaevitz E100 LVDT requires 80.2 kΩ for R2 to produce a ±10.69 volt output and (V_A-V_B)/(V_A+V_B) equals 0.27. The maximum offset value referred to the ±10.69 volt output may be determined by multiplying the maximum value shown in the data sheet (±1% of FS by 1/0.27) which equals ±3.7% maximum. Similarly, to determine the maximum values of offset drift, offset CMRR and offset PSRR when referred to the ±10.69 V output, these data sheet values should also be multiplied by (1/0.27). For the AD598SD/883B the maximum values of offset drift, PSRR offset and CMRR offset would be: ±185 ppm/°C of FS; ±741 ppm/V and ±741 ppm/V, respectively, when referred to the ±10.69 volt output.

⁵R1 is shown in Figure 1.

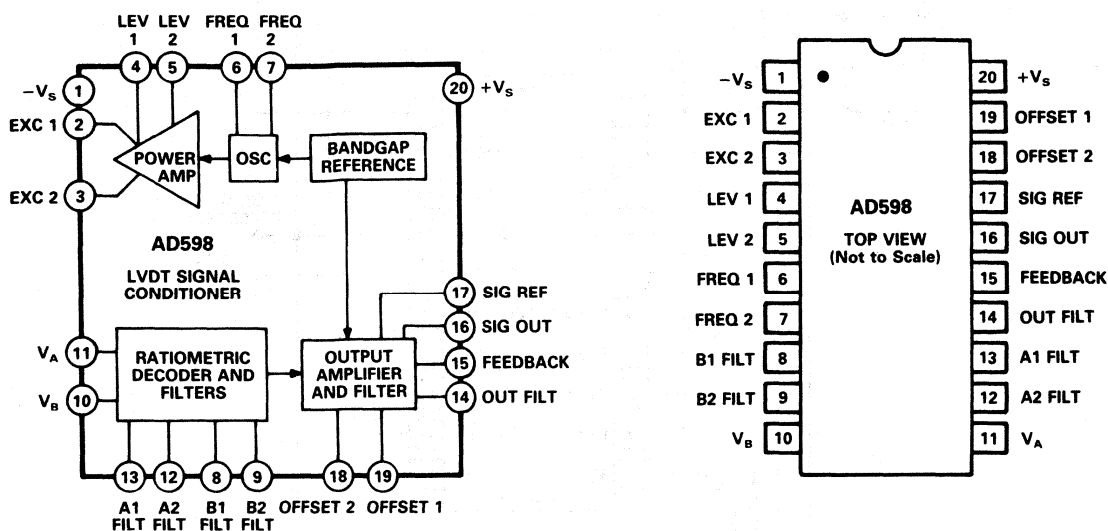
$$\text{Transfer Function: } V_{OUT} = \frac{V_A - V_B}{V_A + V_B} \times 500 \mu A \times R2$$

V_A and V_B represent the mean average deviation (MAD) of the detected sine waves. See Figure 1. Note that for this Transfer Function to linearly represent position displacement, V_A + V_B of the LVDT must remain constant with stroke length.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

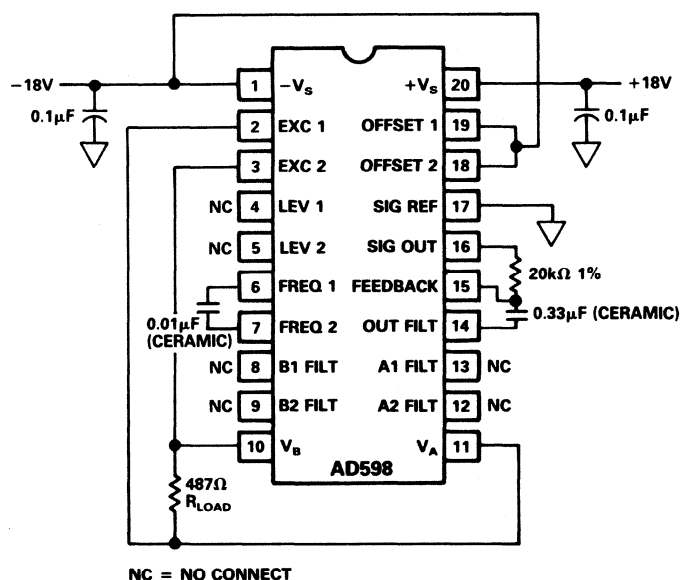


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD598

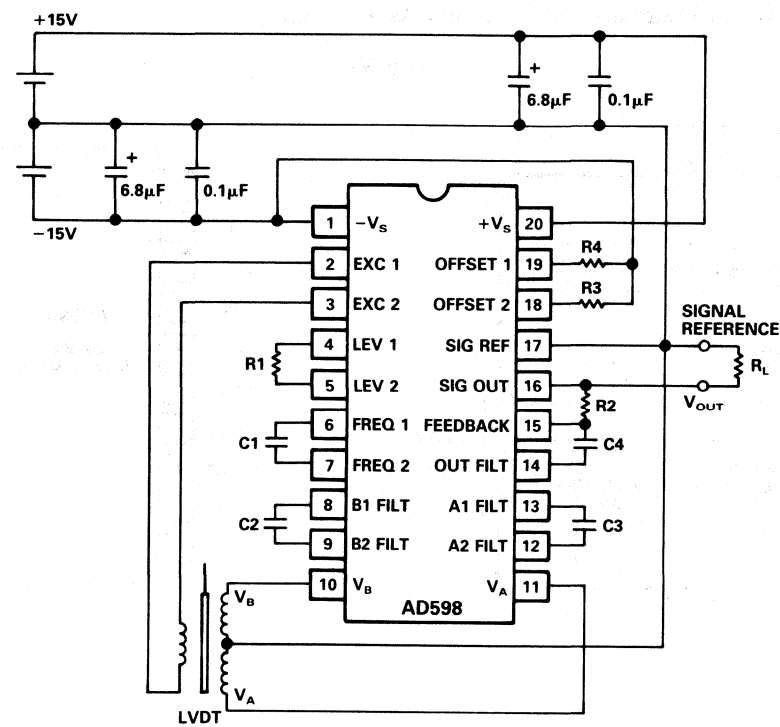


Figure 1. AD598 Interconnection Diagram for Dual Supply Operation

1.1 Scope.

This specification covers the detail requirements for a programmable gain instrumentation amplifier. The gain equation is $\frac{40,000}{R_G} + 1 \pm 20\%$ with external resistor gain programming.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD624SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation	280mW
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C/W}$
θ_{JA}	$= 95^\circ\text{C/W}$

AD624 – SPECIFICATIONS

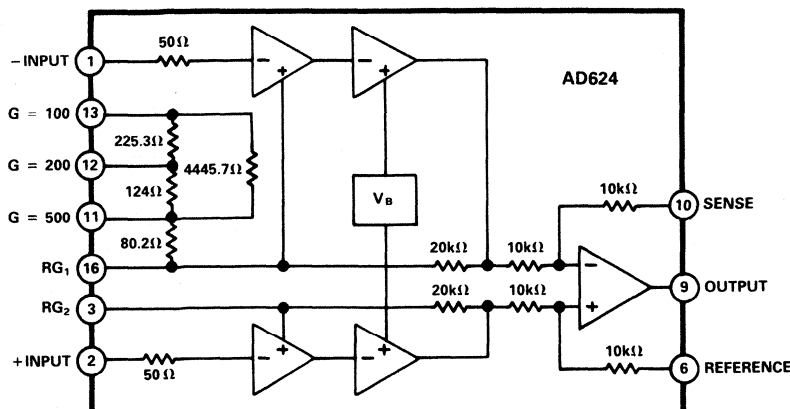
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Error 1	GE ₁	– 1	0.05	0.05			G = 1, V _O = ± 10V	± % max
Gain Error 100	GE ₁₀₀	– 1	0.25	0.25			G = 100, V _O = ± 10V	± % max
Gain Error 200	GE ₂₀₀	– 1	0.5	0.5			G = 200, V _O = ± 10V	± % max
Gain Error 500	GE ₅₀₀	– 1	0.5	0.5			G = 500, V _O = ± 10V	± % max
Gain Error Drift 1	TCGE ₁	– 1	5				G = 1, V _O = ± 10V	± ppm/°C max
Gain Error Drift 100	TCGE ₁₀₀	– 1	10				G = 100, V _O = ± 10V	± ppm/°C max
Gain Error Drift 200	TCGE ₂₀₀	– 1	10				G = 200, V _O = ± 10V	± ppm/°C max
Gain Error Drift 500	TCGE ₅₀₀	– 1	15				G = 500, V _O = ± 10V	± ppm/°C max
Input Offset Voltage	V _{OSI}	– 1	75	75			V _{IN} = 0V	± μV max
Input Offset Voltage Drift	TCV _{OSI}	– 1	2		2		G = 500, V _{IN} = 0V	± μV/°C max
Output Offset Voltage	V _{OSO}	– 1	3	3			V _{IN} = 0V	± mV max
Output Offset Drift	TCV _{OSO}	– 1	50		50		G = 1, V _{IN} = 0V	± μV/°C max
Input Bias Current	I _B	– 1	50	50			G = 1	± nA max
Input Offset Current	I _{OS}	– 1	35	35			G = 1	± nA max
Common-Mode Rejection	+ CMRR ₁	– 1	70	70			G = 1, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₁	– 1	70	70			G = 1, V _{IN} = 0V to – 10V	dB min
Common-Mode Rejection	+ CMRR ₁₀₀	– 1	100	100			G = 100, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₁₀₀	– 1	100	100			G = 100, V _{IN} = 0V to – 10V	dB min
Common-Mode Rejection	+ CMRR ₂₀₀	– 1	100	100			G = 200, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₂₀₀	– 1	100	100			G = 200, V _{IN} = 0V to – 10V	dB min
Common-Mode Rejection	+ CMRR ₅₀₀	– 1	110	110			G = 500, V _{IN} = 0V to + 10V	dB min
Common-Mode Rejection	– CMRR ₅₀₀	– 1	110	110			G = 500, V _{IN} = 0V to – 10V	dB min
Power Supply Current	I _{CC}	– 1	5	5			G = 1	mA max
Power Supply Rejection	PSRR ₁	– 1	75	75			G = 1, V _S = ± 12V, ± 15V	dB min
Power Supply Rejection	PSRR ₁₀₀	– 1	105	105			G = 100, V _S = ± 12V, ± 15V	dB min
Power Supply Rejection	PSRR ₂₀₀	– 1	105	105			G = 200, V _S = ± 12V, ± 15V	dB min
Power Supply Rejection	PSRR ₅₀₀	– 1	110	110			G = 500, V _S = ± 12V, ± 15V	dB min

NOTE

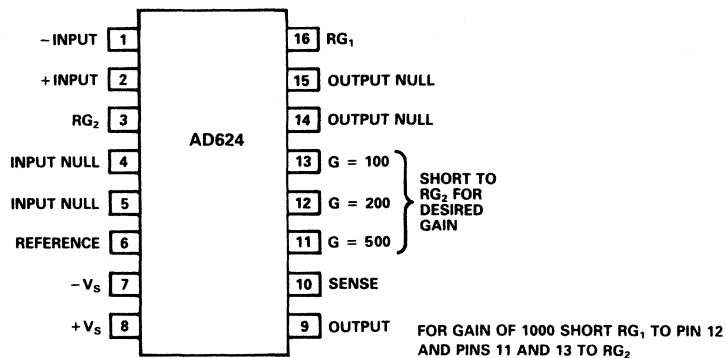
¹V_S = ± 15V, R_L = 2kΩ unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

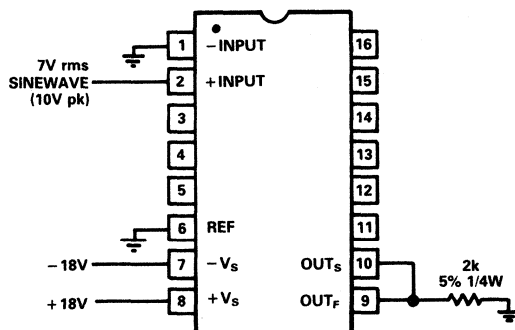


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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1.1 Scope.

This specification covers the detail requirements for a programmable gain instrumentation amplifier. The gain equation is $\frac{2R_F}{R_G} + 1$.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD625SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation	280mW
Input Voltage	$\pm V_S \text{ max}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C/W}$
θ_{JA}	$= 95^\circ\text{C/W}$

AD625 – SPECIFICATIONS

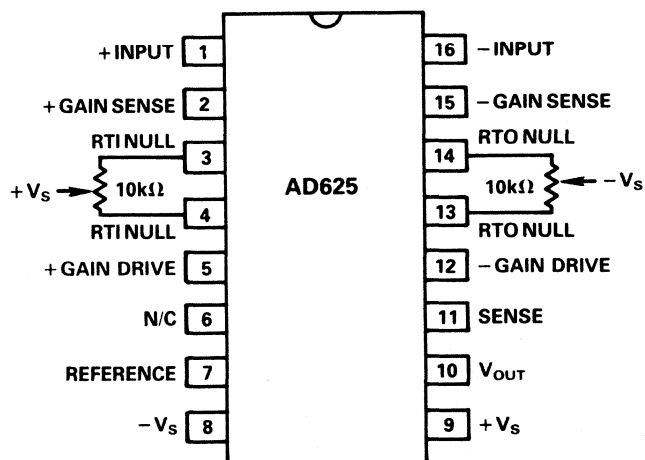
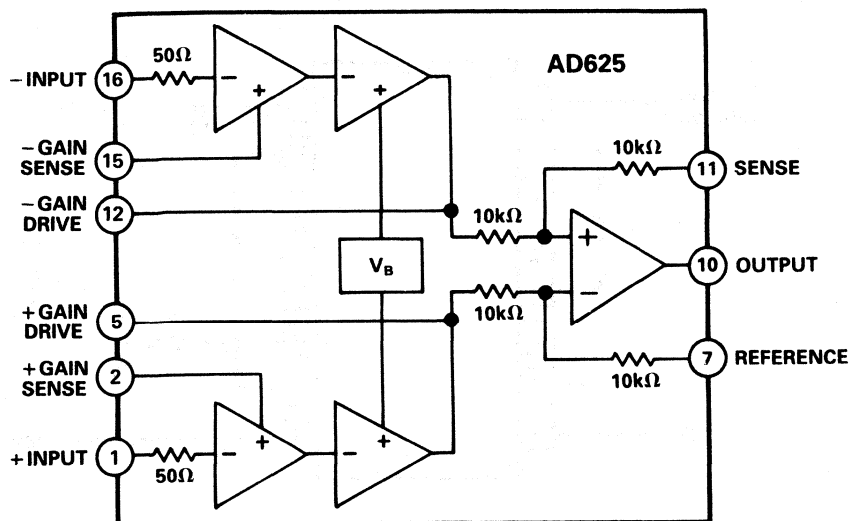
Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Error 1	GE ₁	– 1	0.05	0.05			G = 1	± % max
Gain Error 10	GE ₁₀	– 1	0.05				G = 10	± % max
Gain Error 100	GE ₁₀₀	– 1	0.05				G = 100	± % max
Gain Error 1000	GE ₁₀₀₀	– 1	0.05				G = 1000	± % max
Gain Error Drift	TCGE ₁	– 1	5				G = 1	± ppm/°C max
Gain Error Drift 10	TCGE ₁₀	– 1	5				G = 10	± ppm/°C max
Gain Error Drift 100	TCGE ₁₀₀	– 1	5				G = 100	± ppm/°C max
Gain Error Drift 1000	TCGE ₁₀₀₀	– 1	5				G = 1000	± ppm/°C max
Input Offset Voltage	V _{OSI}	– 1	200	200			V _{IN} = 0V	± μV max
Input Offset Voltage Drift	TCV _{OSI}	– 1	2		2		V _{IN} = 0V	± μV/°C max
Output Offset Voltage	V _{OSO}	– 1	5	5			V _{IN} = 0V	± mV max
Output Offset Drift	TCV _{OSO}	– 1	50		50		V _{IN} = 0V	± μV/°C max
Input Bias Current	I _B	– 1	50	50			G = 1	± nA max
Input Offset Current	I _{OS}	– 1	20	20			I _{OS} = (I _B +) – (I _B –)	± nA max
Common-Mode Rejection	CMRR ₁	– 1	70	70			G = 1	dB min
Common-Mode Rejection	– CMRR ₁	– 1	70	70			G = 1	dB min
Common-Mode Rejection	+ CMRR ₁₀	– 1	90				G = 10	dB min
Common-Mode Rejection	– CMRR ₁₀	– 1	90				G = 10	dB min
Common-Mode Rejection	+ CMRR ₁₀₀	– 1	100				G = 100	dB min
Common-Mode Rejection	– CMRR ₁₀₀	– 1	100				G = 100	dB min
Common-Mode Rejection	+ CMRR ₁₀₀₀	– 1	110	110			G = 1000	dB min
Common-Mode Rejection	– CMRR ₁₀₀₀	– 1	110	110			G = 1000	dB min
Power Supply Current	I _{CC}	– 1	5	5			G = 1	mA max
Power Supply Rejection	PSRR ₁	– 1	70	70			G = 1	dB min
Power Supply Rejection	PSRR ₁₀	– 1	85				G = 10	dB min
Power Supply Rejection	PSRR ₁₀₀	– 1	95				G = 100	dB min
Power Supply Rejection	PSRR ₁₀₀₀	– 1	100	100			G = 1000	dB min

NOTE

¹V_S = ± 15V, R_L = 2kΩ unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



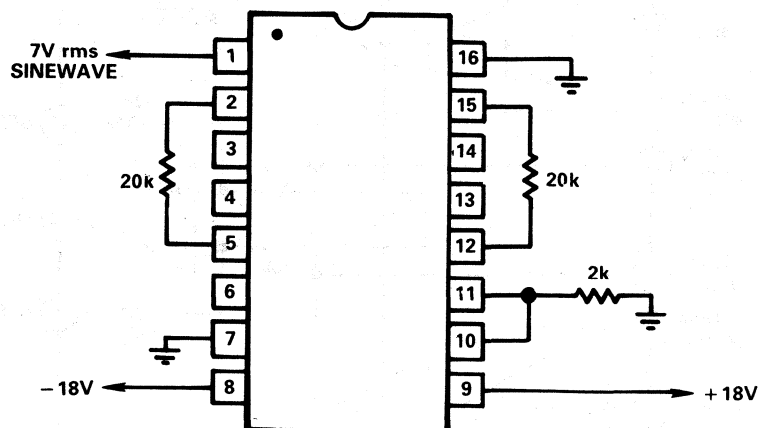
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

AD625

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for a precision laser trimmed balanced modulator/demodulator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD630S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-20	20-Pin DIP
E	E-20A	20 Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation	600mW
Output Short Circuit to Ground	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$
Max Junction Temperature	$+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$ for D-20, E-20A
 $\theta_{JA} = 85^\circ\text{C/W}$ for D-20, E-20A

AD630 – SPECIFICATIONS

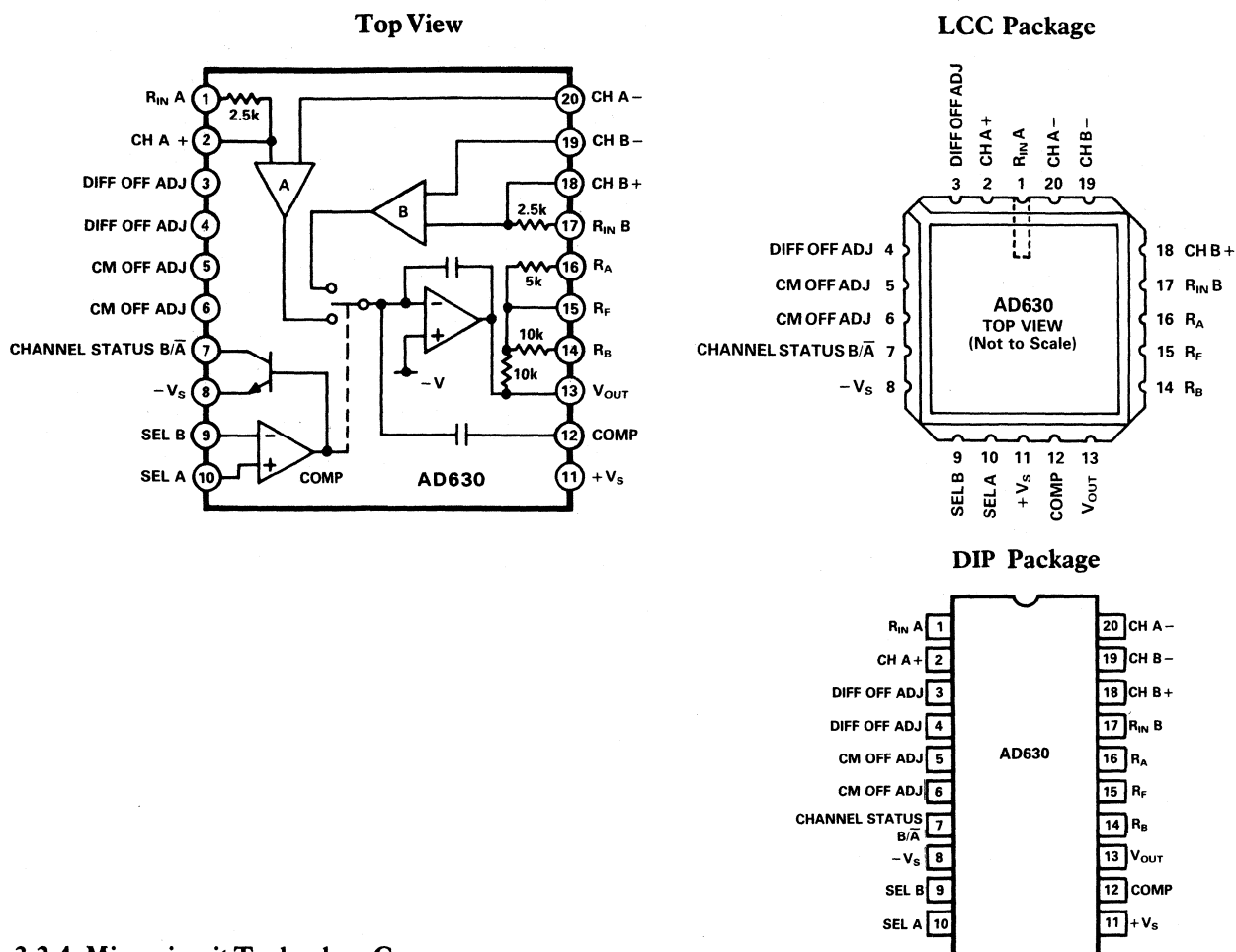
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Output Voltage + Swing (Both Amps)	V _{OUT}	– 1	10	10	10		R _L = 2kΩ	+ V min
Output Voltage – Swing (Both Amps)	V _{OUT}	– 1	10	10	10		R _L = 2kΩ	– V max
Supply Current	I _Q	– 1	5	5				± mA
Amplifier V _{OS} (Both Amps)	V _{OS}	– 1	500	500	1000			± μV
Closed Loop Gain Error (± 1, ± 2) Both Amps	EA _{OL}	– 1	0.5	0.5				± % max
Input Bias Current (Both Amps)	I _B	– 1	300	300				± nA max
Input Offset Current (Both Amps)	I _{OS}	– 1	50	50				± nA max
Comparator Switch Window	CMP _{HYS}	– 1	1.5	1.5	2.5			± mV max
Comparator Bias Current	CMP _{IB}	– 1	300			300		nA max
Comparator Sink Current	I _{SINK}	– 1	1.6	1.6			V _{OL} = – V _S + 0.4V	mA min
Common-Mode Rejection Ratio (Both Amps)	CMRR	– 1	85			85		dB min
Power Supply Rejection Ratio (Both Amps)	PSRR	– 1	90			90		dB min
Short Circuit Current (Both Amps)	I _{SC}	– 1	50	50				± mA max
Output Current (Both Amps)	I _{OUT}	– 1	10	10				± mA min
Open Loop Gain (Both Amps)	A _{OL}	– 1	90			90		dB min

NOTE

¹T_A = +25°C and ± V_S = ± 15V unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

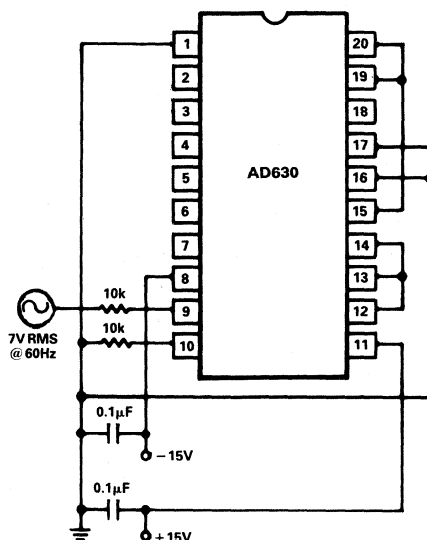


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for an internally trimmed monolithic four-quadrant analog multiplier/divider.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
- 1	AD632S(X)/883B
- 2	AD632T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-14	14-Pin DIP
H	H-10A	10-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltage, $X_1, X_2, Y_1, Y_2, Z_1, Z_2$	$\pm V_S$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14
θ_{JA} = 95°C/W for D-14

AD632 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy ²	RA	-1	1	1	2		$V_X = -10V, -10, +10, +10$	± % FS max
		-2	0.5	1	1	0.5	$V_Y = -10V, +10V, -10, +10$	
Multiplier Accuracy Drift	TC _{MA}	-1	0.02		0.02			± %/°C max
		-2	0.01		0.01			
Nonlinearity, X Input	NL _X	-1	0.6				$V_X = 20V$ pk-pk	± % max
		-2	0.3			0.3	$V_Y = +10V$	
Nonlinearity, Y Input	NL _Y	-1	0.2				$V_Y = 20V$ pk-pk	± % max
		-2	0.10			0.10	$V_X = +10V$	
Output Offset Voltage	V _{OS}	-1	30	30	80		$V_X = V_Y = V_Z = 0V$	± mV max
		-2	15	30	45	15		
Output Offset Voltage Drift	ΔV _{OS} /ΔT	-1	500		500		$V_X = V_Y = V_Z = 0V$	± μV/°C max
		-2	300		300			
Offset Voltage (X)	V _{OSX}	-1	20	20			$V_X = V_Z = 0V$	± mV max
		-2	10	20		10	$V_Y = ±10V$	
Offset Voltage (Y)	V _{OSY}	-1	20	20			$V_Y = V_Z = 0V$	± mV max
		-2	10	20		10	$V_X = ±10V$	
Input Bias Current X, Y or Z Inputs	I _{IB}	-1, 2	2	2			$V_X = V_Y = V_Z = 0V$	± μA max
Input Offset Current X, Y or Z Inputs	I _{IO}	-1, 2	2	2			$V_X = V_Y = V_Z = 0V$	± μA max
Supply Current From V _{CC}	I _{CC}	-1, 2	6.0	6.0			R _L = No Load	+ mA max
Supply Current From V _{EE}	I _{EE}	-1, 2	6.0	6.0				- mA max
Common-Mode Rejection Ratio X, Y, or Z Inputs	CMR _X	-1	60			60	$-10V ≤ V_X ≤ +10V$	dB min
		-2	70			70	$V_Y = +10V$	
	CMR _Y	-1	60			60	$-10V ≤ V_Y ≤ +10V$	dB min
		-2	70			70	$V_X = +10V$	
Output Voltage Swing	V _{OP}	-1, 2	11	11	11			± V min
Slew Rate	SR	-1, 2	18				$V_{OUT} = 20V$ pk-pk	V/μs min
1% Amplitude Error	A _E	-1, 2	50				$V_X = 2V$ pk-pk $C_{LOAD} = 1000pF, V_Y = +10V$	kHz min
Feedthrough, X Input ³	FRR	-1	0.70				Y Nulled, X = 20V	± % FS max
		-2	0.30			0.30	pk-pk @ 50Hz	
Feedthrough, Y Input ³	FRR	-1	0.40				X Nulled, Y = 20V	± % FS max
		-2	0.10			0.10	pk-pk @ 50Hz	

NOTES

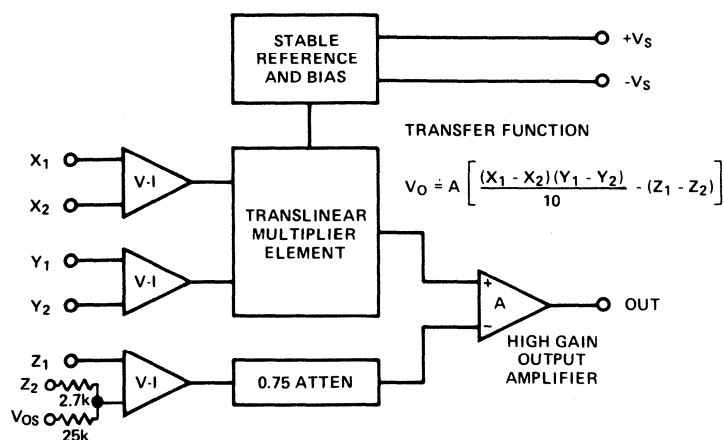
¹T_A = +25°C, V_S = ±15V, unless otherwise noted.

²Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).

³Irreducible component due to nonlinearity: excludes effects of offsets.

Table 1.

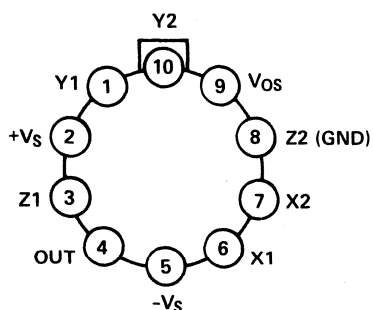
3.2.1 Functional Block Diagram and Terminal Assignments.



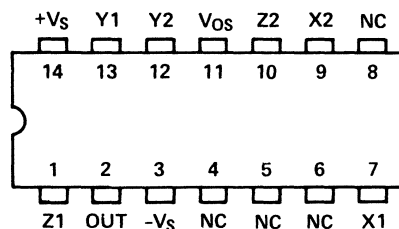
Pin Assignments

Top View

H-Package TO-100



D-Package TO-116

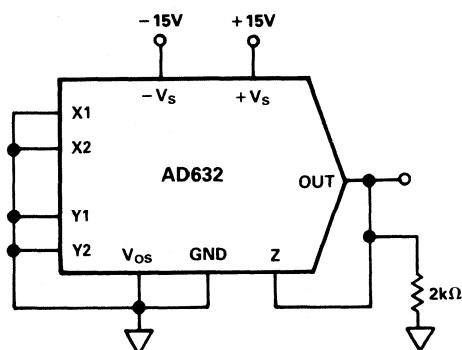


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





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1.1 Scope.

This specification covers the detail requirements for a high precision, monolithic, wideband rms-to-dc converter that computes the true rms value of any complex waveform with the following transfer function:

$$V_{OUT} = \sqrt{AVG. (V_{IN})^2}$$

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD637SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-14.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V dc}$
Internal Quiescent Power Dissipation	108mW
Output Short Circuit Duration	Indefinite
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 95^\circ\text{C/W}$

AD637 – SPECIFICATIONS

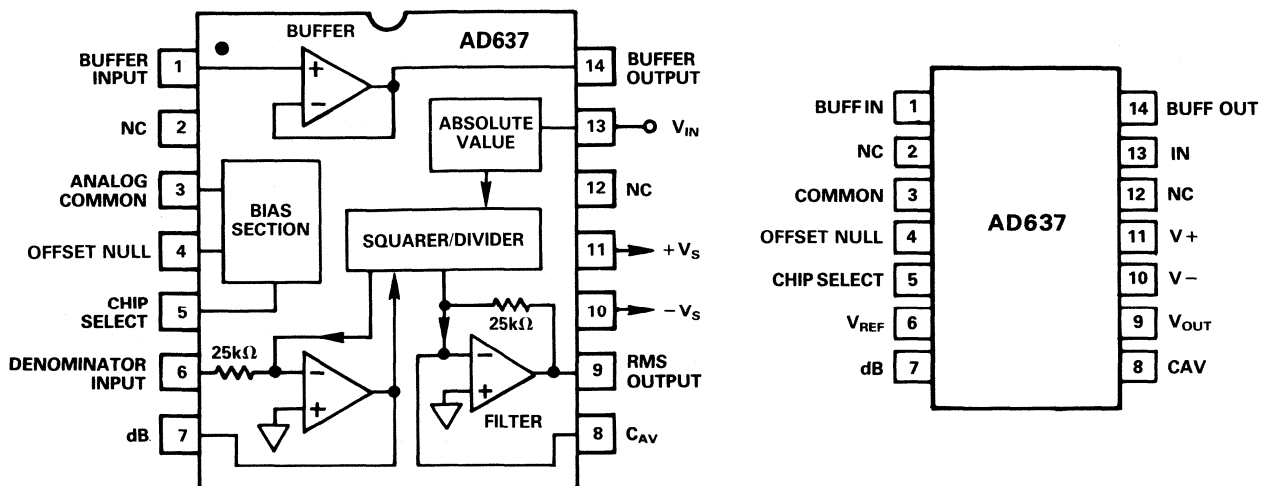
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Total Error	E_T	-1	1 0.5	1 0.5	6 0.7		$V_{IN} = 0$ to $\pm 10V$	$\pm mV \pm \%$ of Reading max
Total Error vs. Supply +	$\Delta E_T/\Delta T$	-1	150	150	150		$+5V \leq V_S \leq +15V$	$\pm \mu V/V$ max
Total Error vs. Supply -	$\Delta E_T/\Delta T$	-1	300	300	500		$-5V \leq V_S \leq -15V$	$\pm \mu V/V$ max
dc Reversal Error	E_{TR}	-1	0.25	0.25			$V_{IN} = \pm 2V$	$\pm \%$ of Reading max
Nonlinearity, 2V FS	NL_1	-1	0.04	0.04	0.06		$10mV \leq V_{OUT} \leq 2V$	$\pm \%$ of FS max
Nonlinearity, 7V FS	NL_2	-1	0.05	0.05	0.14		$10mV \leq V_{OUT} \leq 7V$	$\pm \%$ of FS max
Output Offset Voltage	V_{OSO}	-1	1	1	6		$V_{IN} = GND$	$\pm mV$ max
Output Offset Voltage Drift	$\Delta V_{OSO}/\Delta T$	-1	0.07		0.07		$V_{IN} = GND$	$\pm mV/^{\circ}C$ max
Output Voltage Swing at V_{OUT}	V_{OP}	-1	12	12	12		$R_L = 2k\Omega$	V min
$I_{REF\theta}$ for 0dB = 1V rms	I_{REF}	-1	5 80	5 80				μA min μA max
I_{REF} Range	I_{REF}	-1	1 100					μA min μA max
Buffer Input Offset Voltage	V_{OSO}	-1	2	2				$\pm mV$ max
Buffer Input Current	I_{IN}	-1	10	10				$\pm nA$ max
Denominator Input Resistance	R_{DEN}	-1	20 30					$k\Omega$ min $k\Omega$ max
Denominator Input Offset Voltage	V_{OSD}	-1	0.5					$\pm mV$ max
Power Supply Range	V_S	-1	3 18	3 18				$\pm V$ min $\pm V$ max
Quiescent Current	I_Q	-1	3	3	3		$V_S = \pm 15V$ or $\pm 18V$	mA max
Standby Current	I_{SB}	-1	450	450			$V_{CS} < 0.2V$	μA max

NOTE

¹ $T_A = +25^{\circ}C$ and $V_S = \pm 15V$ dc, unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

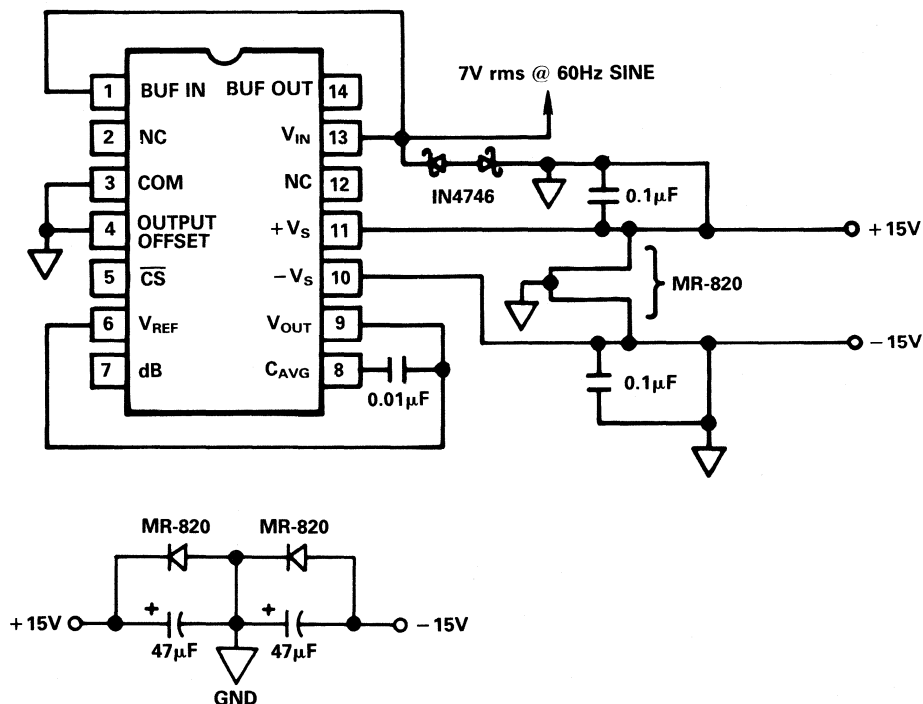


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high-accuracy, monolithic trigonometric function converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD639SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-18.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation	300mW
Short Circuit to Ground	Indefinite
Input Voltages X_1, X_2, Y_1, Y_2 ¹	$\pm 12\text{V}$
Input Voltages U_P, U_1, U_2, Z_1, Z_2 ¹	$\pm 25\text{V}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹These inputs are purely resistive and the maximum inputs are determined by resistor dissipation limits, not the supply voltages.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$

AD639 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1,2}	Units
Peak Absolute Error								
Sine Mode	E_S	-1	0.8	0.8	2.5		-90° to +90°, $U_P = 10V$	% FS max
Cosine Mode	E_C	-1	1.2	1.2	2.7		-90° to +90°, $U_P = 10V$	% FS max
Both Modes	E_{SC}	-1	1.5	1.5	3.0		-180° to +180°, $U_P = 10V$	% FS max
	E_{SC}	-1	2.5	2.5	3.5		-90° to +90°, $U_P = 1V$	% FS max
	E_{SC}	-1	3.0	3.0	4.0		-180° to +180°, $U_P = 1V$	% FS max
Tangent Mode	E_T	-1	2.5	2.5	3.0		-45° to +45°, $U_P = 1V$	% FS max
	E_T	-1	3.5	3.5			-45° to +45°, $U_P = 10V$	% FS max
Angle Input ³	X_{SC}	-1	0.65			0.65	X_1 or X_2	% max
Scaling Error	Y_{SC}	-1	1.0			1.0	Y_1 or Y_2	% max
Angle Input ³	X_{OS}	-1	0.3			0.3	$X_1 = X_2 = 0$	° max
Angular Offset	Y_{OS}	-1	0.5			0.5	$Y_1 = Y_2 = 0$	° max
Amplitude Input Gain Error	U_{SC}	-1	0.5			0.5	$U = 0.1$ to $10V$	% max
Amplitude Input Voltage Offset	U_{OS}	-1	10			10	$U_1 = U_2 = 0V$	mV max
Amplitude Preset Accuracy	U_{LO}	-1	2.0			2.0	$U_P = 1V$	% max
	U_{HI}	-1	0.55			0.55	$U_P = 10V$	% max
Output Voltage Swing	V_O	-1	± 11	± 11				V min
Short-Circuit Current	I_{SC}	-1	45	45				mA max
Output Offset	Z_{OS}	-1	30			30	$Z_1 = Z_2 = 0, U_P = 10V$	mV max
	Z_{OS}	-1	20			20	$Z_1 = Z_2 = 0, U_P = 1V$	mV max
Reference Accuracy	V_{REF}	-1	0.45	0.45	0.6			% max
+ Supply Current	+ I_S	-1	11	11			$U = X = 0, Y = V_R$	mA max
- Supply Current	- I_S	-1	7.5	7.5			$U = X = 0, Y = V_R$	mA max

NOTES

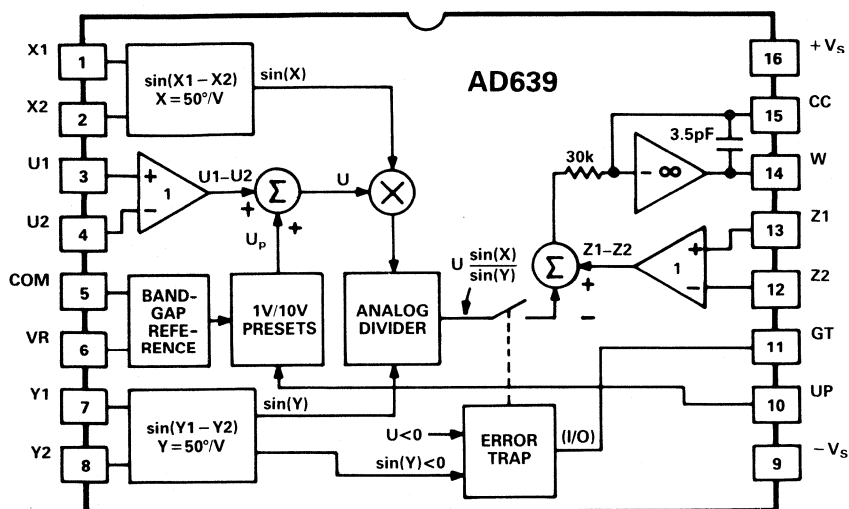
¹ $V_S = \pm 15V, R_L = 2k\Omega$.

²Full scale is defined as the ideal output when the angle input is at either end of the limit specified.

³Specifications for the X inputs apply for the range. $U_P = 1V$ to $10V$ while the Y input errors are specifically given for $U_P = 1V$.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

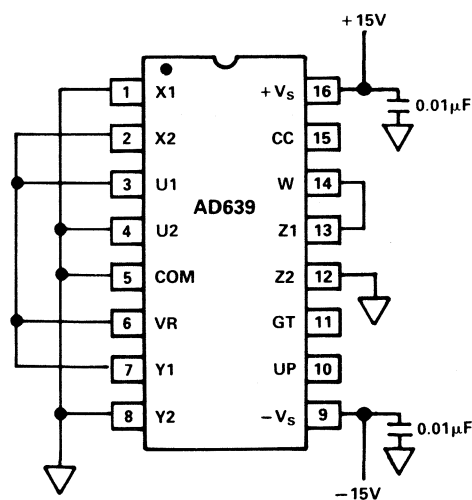


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic, dc-coupled, demodulating, 120 MHz logarithmic amplifier, whose transfer function is

$$I_{OUT} = 1 \text{ mA} \star \left(\text{Log}_{10} \frac{|V_{IN}|}{(1 \text{ mV})} \right)$$

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD640T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-20	20-Pin DIP
E	E-20A	20-Pin Leadless Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltages	$\pm 7.5 \text{ V}$
Input Voltage (Pin 1 or Pin 20 to COM)	-3 V to $+300 \text{ mV}$
Attenuator Input Voltage (Pin 5 to Pin 3/4)	$\pm 3 \text{ V}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

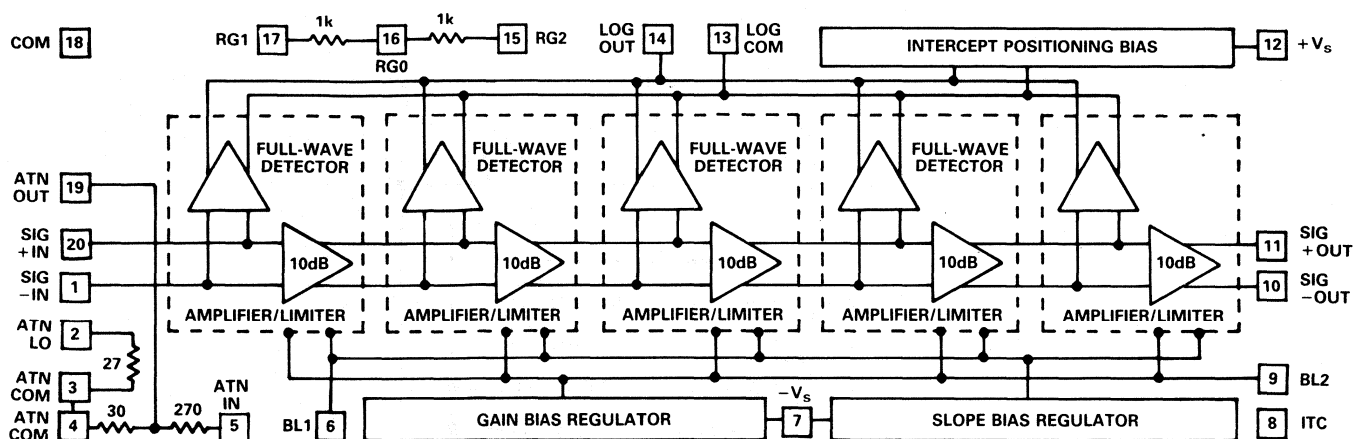
Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$ for D-20, E-20A
 $\theta_{JA} = 95^\circ\text{C/W}$ for D-20, E-20A

AD640 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition	Units
Total Absolute DC Accuracy vs. Supplies	TA	-1	0.9	0.9	1.8		$V_{IN} = \pm 1 \text{ mV to } \pm 100 \text{ mV}$	$\pm \text{dB}$
			2.0			2.0	$V_{IN} = \pm 0.75 \text{ mV to } \pm 200 \text{ mV}$	
			1.5	1.5	2.0		$V_{IN} = \pm 10 \text{ mV to } \pm 1 \text{ V}$ Using Attenuator	
			2.5			2.5	$V_{IN} = \pm 7.5 \text{ mV to } \pm 2 \text{ V}$ Using Attenuator	
			1.0			1.0	$\pm V_S = \pm 4.5 \text{ V to } \pm 7.5 \text{ V}$ $V_{IN} = \pm 1 \text{ mV to } \pm 100 \text{ mV}$	
DC Linearity	LE _{DC}	-1	0.6	0.6			$V_{IN} = \pm 1 \text{ mV to } \pm 100 \text{ mV}$	$\pm \text{dB}$
Input Offset Voltage	V _{OS}	-1	200	200	300		Differential	$\pm \mu\text{V}$
Input Bias Current	I _B	-1	25					$\pm \mu\text{A}$
Slope Current vs. Supplies	IY _{DC}	-1	0.02	0.02	0.02		From Nominal of 1.00 mA	$\pm \text{mA}$
		-1	0.4			0.4	$\pm V_S = \pm 4.5 \text{ V to } \pm 7.5 \text{ V}$	%/V
Intercept Voltage	VX _{DC}	-1	0.05	0.05	0.1		From Nominal of 1.00 mV	$\pm \text{mV}$
			1.0	1.0			From Nominal of 10.0 mV Using Attenuator	$\pm \text{mV}$
Application Resistors	R _A	-1	5			5	From Nominal of 1000 Ω	$\pm \Omega$
AC Linearity	LE _{AC}	-1	1.0 0.5 1.5 1.0				f = 1 MHz, -40 dBm to -2 dBm f = 1 MHz, -35 dBm to -10 dBm f = 1 MHz, -75 dBm to 0 dBm Cascaded Operation f = 1 MHz, -70 dBm to -10 dBm Cascaded Operation	$\pm \text{dB}$
AC Slope Current	IY _{AC}	-1	0.02 0.03 0.04				From Nominal of 1.00 mA f ≤ 1 MHz From Nominal of 0.94 mA f = 30 MHz From Nominal of 0.90 mA f = 60 MHz	$\pm \text{mA}$
AC Intercept Voltage	VX _{AC}	-1	1.0				From Nominal of -88.6 dBm f ≤ 1 MHz	$\pm \text{dBm}$
Supply Current	+I _S -I _S	-1	15 60	15 60	15 60			mA
Supply Voltage	V _S	-1	±4.5 ±7.5					$\pm \text{V min to max}$

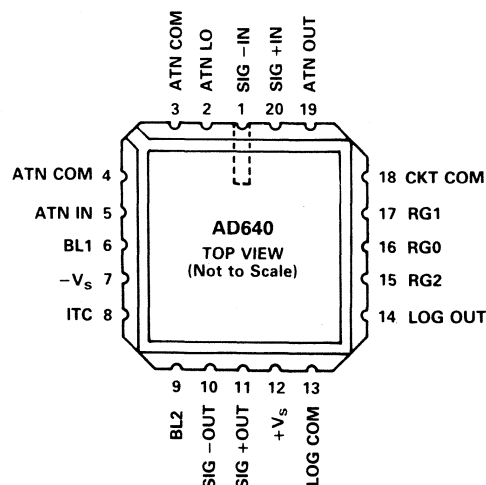
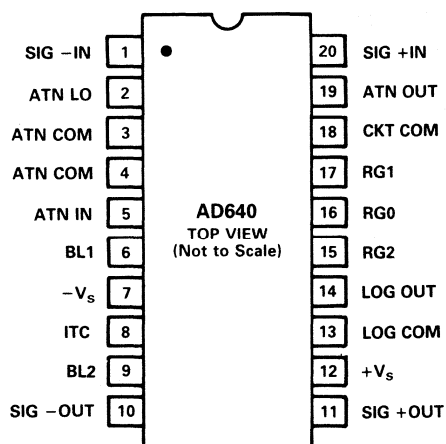
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



20-Pin Ceramic (D) Package

20-Pin LCC (E) Package



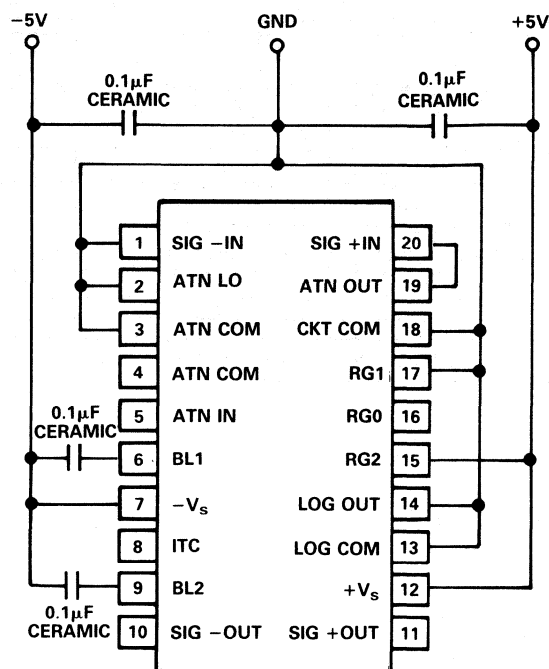
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

AD640

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for a dual precision monolithic BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD642SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline: H-08B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 20\text{V}$
Common-Mode Input Voltage Range	$\pm 12\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT	DERATE ABOVE MAXIMUM
Package Type	Temperature for Rating	Ambient Temperature
TO-99	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$

AD642 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	250	250	100		V _O = ± 10V, R _L ≥ 2kΩ	V/mV max
Slew Rate	t _{SR}	– 1	2.0				Unity Gain	V/μs min
Gain Bandwidth Product	GBW	– 1	0.7					MHz min
Output Voltage Swing	V _{OUT}	– 1	10	10	10		R _L ≥ 2kΩ	± V min
			12	12	12		R _L ≥ 10kΩ	
Input Offset Voltage ²	V _{OS}	– 1	1.0	1.0	3.5			± mV max
Input Offset ^{2,3} Voltage Matching	V _{OSM}	– 1	0.5	0.5	3.5			± mV max
Input Bias Current ⁴	I _B	– 1	35	35				± pA max
Input Bias ³ Current Matching	I _{BM}	– 1	35	35				± pA max
Common-Mode Rejection Ratio	CMRR	– 1	80	80	80			dB min
Common-Mode Voltage Range	CMVR	– 1	10	10	10			± V min
Power Supply Current	I _Q	– 1	2.8	2.8				mA max
Power Supply Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max
Output Short Circuit Current	I _{SC}	– 1	25					mA max

NOTES

¹T_A = +25°C, V_S = ± 15V.

²Input Offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

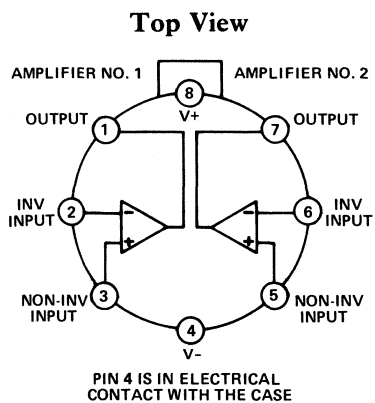
³Matching is defined at the difference between parameters of the two amplifiers.

⁴Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

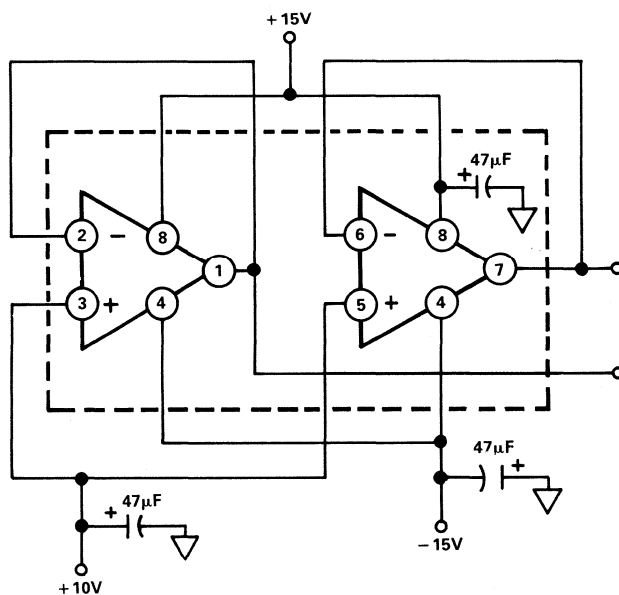


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a dual high speed, precision, monolithic BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD644SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 20\text{V}$
Common-Mode Input Voltage	$\pm 12\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Package Type		
TO-99	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$

AD644 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	50	50	20		V _{OUT} = ± 10V, R _L ≥ 2kΩ	V/mV min
Slew Rate	t _{SR}	– 1	8	8				V/μs min
Gain Bandwidth Product	GBW	– 1	1.5					MHz min
Output Voltage Swing	V _{OUT}	– 1 – 1	10 12	10 12	10 12		R _L ≥ 2kΩ R _L ≥ 10kΩ	± V min
Input Offset Voltage ²	V _{OS}	– 1	1.0	1.0	3.5			+ mV max
Input Offset ^{2,3} Voltage Matching	V _{OSM}	– 1	0.5	0.5	3.5			± mV max
Input Offset Drift	TC V _{OS}	– 1	15					± μV/°C max
Input Bias Current ⁴	I _B	– 1	35	35				± pA max
Input Bias ³ Current Matching	I _{BM}	– 1	35	35				± pA max
Common-Mode Rejection Ratio	CMRR	– 1	80	80	80			dB min
Common-Mode Voltage Range	CMVR	– 1	10	10	10			± V min
Power Supply Current	I _Q	– 1	4.5	4.5				mA max
Power Supply Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max
Output Short Circuit Current	I _{SC}	– 1	25					mA max

NOTES

¹T_A = +25°C, V_S = ± 15V, unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

Nulling will induce an additional ± 3μV/°C.

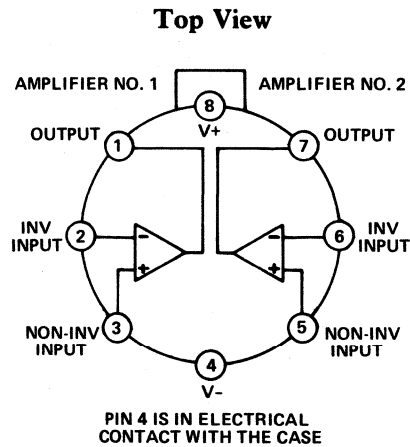
³Matching is defined as the difference between parameters of the two amplifiers.

⁴Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

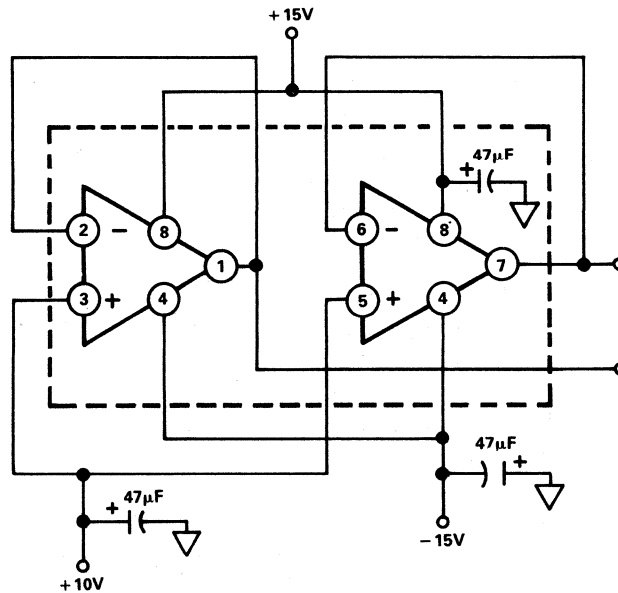


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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1.1 Scope.

This specification covers the detail requirements for a dual ultralow drift, monolithic BiFET amplifier.

1.2 Part Number.

Device	Part Number ¹
– 1	AD647S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
H	H-08B	8-Pin Metal Package
E	E-20A	20 Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 20\text{V}$
Common-Mode Input Voltage Range	$\pm 12\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99	80°C	$7.1\text{mW}/^\circ\text{C}$

1.4 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08B
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08B
θ_{JC}	$= 25^\circ\text{C}/\text{W}$ for E-20A
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for E-20A

AD647 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	250	250	100		V _O = ± 10V, R _L ≥ 2kΩ	V/mV max
Slew Rate	t _{SR}	– 1	2.0				Unity Gain	V/μs min
Gain Bandwidth Product	GBW	– 1	0.7					MHz min
Output Voltage Swing	V _{OUT}	– 1	10 12	10 12	10 12		R _L ≥ 2kΩ R _L ≥ 10kΩ	± V min
Input Offset Voltage ²	V _{OS}	– 1	0.5	0.5				± mV max
Input Offset ^{2, 3} Voltage Matching	V _{OSM}	– 1	0.5	0.5				± mV max
Input Offset Voltage Drift	TCV _{OS}	– 1	5.0		5.0			± μV/°C max
Input Offset ³ Drift Matching	TCV _{OSM}	– 1	10		10			± μV/°C max
Input Bias Current ⁴	I _B	– 1	35	35				± pA max
Input Bias ³ Current Matching	I _{BM}	– 1	25	25				± pA max
Common-Mode Rejection Ratio	CMRR	– 1	80	80	80			dB min
Common-Mode Voltage Range	CMVR	– 1	10	10	10			± V min
Input Noise Voltage	E _{NPP}	– 1	4			4	0.1Hz to 10Hz	μV p-p max
Power Supply Current	I _Q	– 1	2.8	2.8				mA max
Power Supply Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max
Output Short Circuit Current	I _{SC}	– 1	25					mA max

NOTES

¹T_A = +25°C, V_S = ± 15V.

²Input Offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

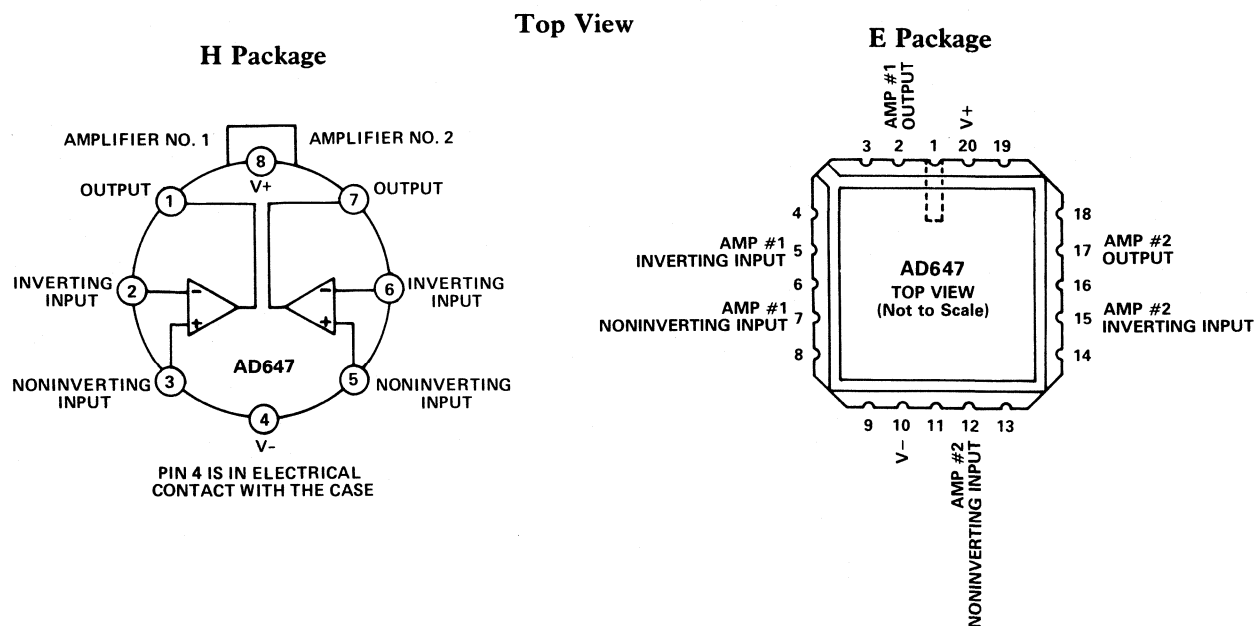
³Matching is defined at the difference between parameters of the two amplifiers.

⁴Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Pin Assignments.

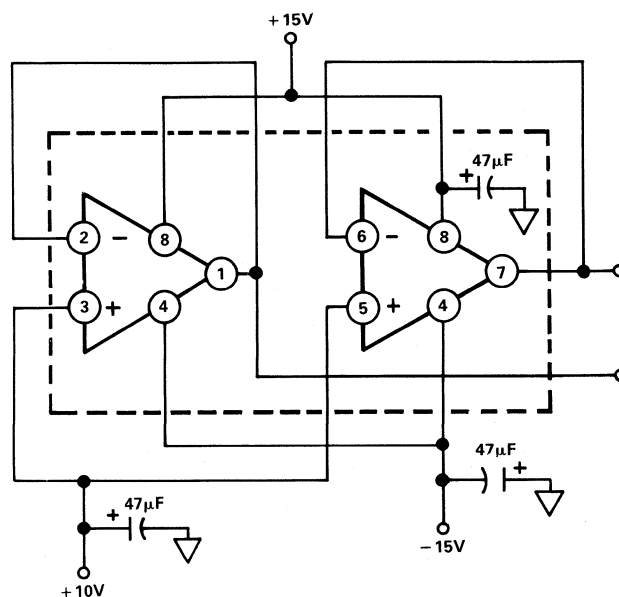


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD648S(X)/883B
- 2	AD648T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip Package
H	H-08B	8-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$+V_S$ and $-V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8A	75°C	$6.7\text{mW}/^\circ\text{C}$
H-08B	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8A
θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08B
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08B

AD648 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Input Offset Voltage	V _{OS}	-1 -2	2.0 1.0	2.0 1.0	3.0 2.0			± mV max
Input Offset Voltage Drift	TCV _{OS}	-1 -2	20 10		20 10			± μV/°C max
Power Supply Rejection Ratio	PSRR	-1 -2	80 86	80 86	76 80			dB min
Input Bias Current ²	I _B	-1 -2 -1 -2	20 10 30 15	20 10 30 15			Either Input, V _{CM} = 0 Either Input, V _{CM} = 0 Either Input, V _{CM} = +10V Either Input, V _{CM} = +10V	± pA max ± pA max
Input Offset Current ²	I _{OS}	-1 -2	10 5	10 5			V _{CM} = 0 V _{CM} = 0	± pA max
Gain Bandwidth Product	GBW	-1, 2	1.0					MHz min
Slew Rate	t _{SR}	-1, 2	1.0	1.0			Unity Gain	V/μs min
Common-Mode Voltage Range	CMVR	-1, 2	-V _S + 4V +V _S - 2V					V
Common-Mode Rejection Ratio	CMRR	-1 -2 -1 -2	76 82 70 76	76 82 70 76	76 82 70 76		V _{CM} = ±10V V _{CM} = ±10V V _{CM} = ±11V V _{CM} = ±11V	dB min dB min
Open Loop Gain	A _{OL}	-1, 2	150/300	150/300	150/300		R _L = 5k/10k	V/mV min
Output Voltage Swing	V _{OUT}	-1, 2	±12/±11	±12/±11	±12/±11		R _L = 10k/5kΩ	± V min
Power Supply Current	I _Q	-1, 2	0.4	0.4				mA max
Input Offset Voltage Match ³	V _{OSM}	-1 -2	2.0 1.0	2.0 1.0	3.0 2.0			± mV max
Input Offset Voltage Drift Match ³	TCV _{OSM}	-1 -2	25 15					± μV/°C max
Input Bias Current Match ³	I _{BM}	-1 -2	10 5	10 5				± pA max

NOTES

¹T_A = +25°C, V_S = ±15V unless otherwise noted.

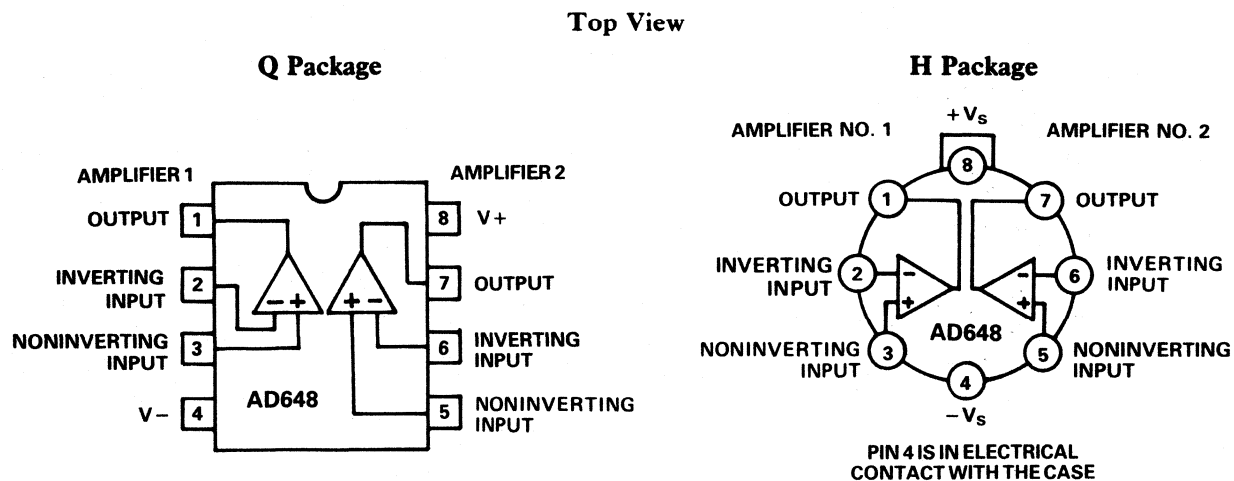
²Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

³Matching is defined as the difference between parameters of the two amplifiers.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

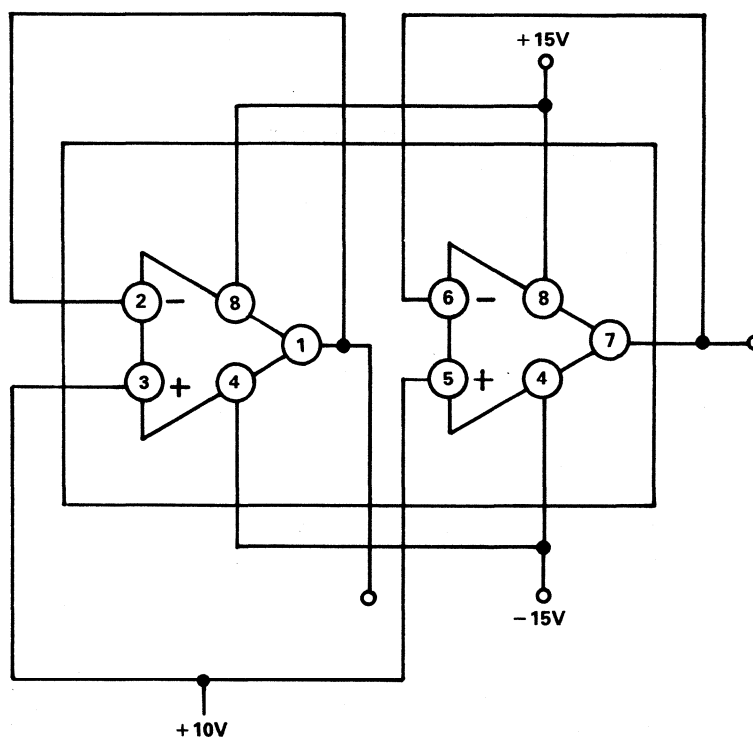


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a voltage-to-frequency converter with full scale range of up to 1MHz.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD650SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-14.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage $+V_S$ to $-V_S$	36V
Differential Input Voltage (Pins 2 & 3)	$\pm 10\text{V}$
Maximum Input Voltage	$\pm V_S$
Open Collector Output Voltage Above Digital GND	+36V
Open Collector Output Current	50mA
Amplifier Short Circuit to Ground	Indefinite
Comparator Input Voltage (Pin 9)	$\pm V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 65^\circ\text{C/W}$
θ_{JA}	$= 150^\circ\text{C/W}$

AD650 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Linearity Error ²	LE	– 1	0.02	0.02			V _{IN} = 10mV, 10V f = 100kHz	% of FS max
			0.1	0.1			V _{IN} = 10mV, 10V f = 1MHz	% of FS max
Gain Error ²	A _E	– 1	10	10			V _{IN} = 10V, f = 100kHz	± % of FS max
			15	15			V _{IN} = 10V, f = 1MHz	± % of FS max
Gain Error vs. Supply	P _{SS}	– 1	0.015	0.015			12.5 ≤ V _S ≤ 17.5V f _{FS} = 100kHz	± % of FS/ % Supply max
Gain Error vs. Temperature	dA _E /dT	– 1			75		V _{IN} = 10V f = 10kHz 25°C to 125°C	± ppm/°C max
					75		– 55°C to 25°C	
					150		f = 100kHz 25°C to 125°C	
					150		– 55°C to 25°C	
Input Offset Voltage ³	V _{IO}	– 1	4	4			V _{IN} = 20mV F = 100kHz	± mV max
Input Offset Voltage vs. Temperature	ΔV _{IO} /ΔT	– 1			30		f = 10kHz 25°C to 125°C	± μV/°C max
					30		– 55°C to 25°C	
Input Bias Current	+ I _{IB}	– 1	100	100			V _{IN} = 100mV	± nA max
	– I _{IB}	– 1	20	20			V _{IN} = 100mV	± nA max
Differential Impedance	Z _{IND}	– 1	2 10					MΩ pF
Low Level Output Voltage	V _{OL}	– 1	0.4	0.4			I _{SINK} = 8mA	V max
Leakage Current	I _{OH}	– 1	100	100			V _{OUT} = 15V	nA max
Dynamic Response Settling Time (See Note 3 for Design Limits)	t _S	– 1	See Note 3				Full Scale Step Input	
Overload Recovery Time (See Note 3 for Design Limits)	OR	– 1	See Note 3					
Quiescent Current	+ I _S	– 1	8	8			V _S = ± 15V, V _{IN} = 0V	mA max
	– I _S	– 1	8	8			V _S = ± 15V, V _{IN} = 0V	– mA min

NOTES

¹V_S = ± 15V, unless otherwise specified.

²Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.

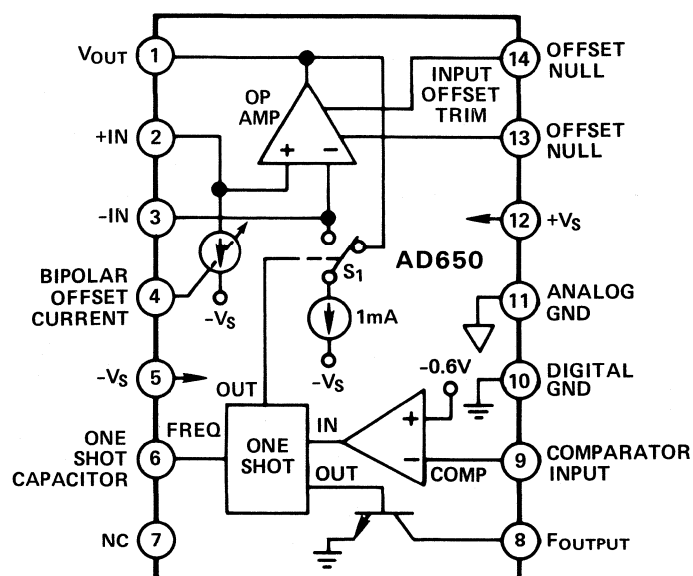
³1 pulse of new frequency plus 1μs.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

D Package

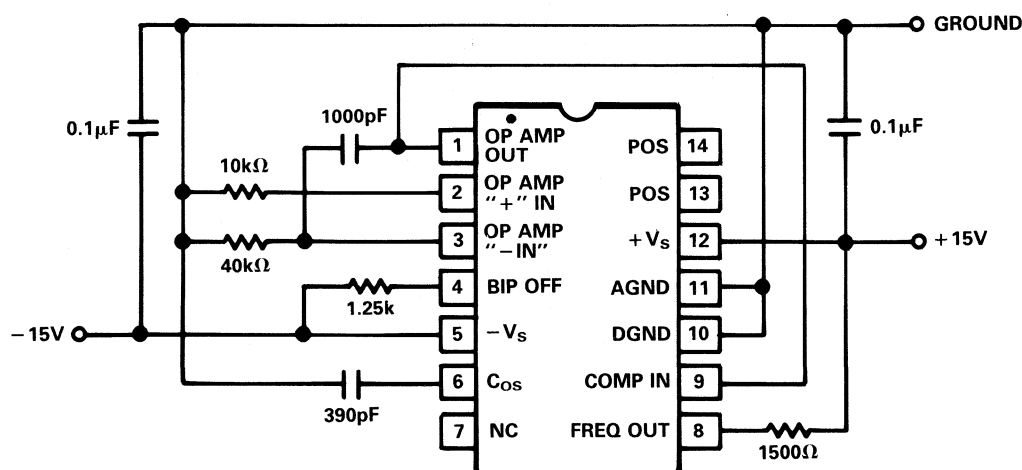


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Synchronous Voltage-to-Frequency and Frequency-to-Voltage Converter

AD652

1.1 Scope.

This specification covers the detail requirements for a voltage-to-frequency with full-scale range of up to 2MHz.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
- 1	AD652S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Lead Ceramic DIP
E	E-20A	20-Terminal Leadless Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Total Supply Voltage $+V_S$ to $-V_S$	36V
Open Collector Output Voltage Above Digital Ground	36V
Open Collector Output Current	50mA
Amplifier Short Circuit to Ground	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C}/\text{W}$ for Q-16
$\theta_{JA} = 100^\circ\text{C}/\text{W}$ for Q-16
$\theta_{JC} = 35^\circ\text{C}/\text{W}$ for E-20A
$\theta_{JA} = 120^\circ\text{C}/\text{W}$ for E-20A

AD652 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Linearity Error ²	LE	– 1	0.02	0.02		$f_{\text{CLOCK}} = 1\text{MHz}$, $V_{\text{IN}} = 0.01, 0.1; 1.0$ to 9.4V in 1.05V Steps	% of FS max
			0.05	0.05		$f_{\text{CLOCK}} = 4\text{MHz}$, $V_{\text{IN}} = 0.01, 0.1; 1.0$ to 9.4V in 1.05V Steps	% of FS max
Gain Error ²	A_E	– 1	1	1		$f_{\text{CLOCK}} = 1\text{MHz}$, $V_{\text{IN}} = 0.01, 9.4\text{V}$	% of FS max
			1.5	1.5		$f_{\text{CLOCK}} = 4\text{MHz}$, $V_{\text{IN}} = 0.01, 9.4\text{V}$	% of FS max
Gain Temperature Coefficient	TCA	– 1			50	$f_{\text{CLOCK}} = 1\text{MHz}$, $V_{\text{IN}} = 0.01, 9.4\text{V}$	± ppm/°C max
					75	$f_{\text{CLOCK}} = 4\text{MHz}$, $V_{\text{IN}} = 0.01, 9.4\text{V}$	± ppm/°C max
Power Supply Rejection Ratio	P_{SRR}	– 1	0.01	0.01		$12\text{V} \leq V_S \leq 18\text{V}$, $f_{\text{CLOCK}} = 4\text{MHz}$	%/V
Offset Voltage ³ (Transfer Function, RTI)	V_{IO}	– 1	3	3		$f_{\text{CLOCK}} = 1\text{MHz}$, $V_{\text{IN}} = 0.01, 9.4\text{V}$ $f_{\text{CLOCK}} = 4\text{MHz}$, $V_{\text{IN}} = 0.01, 9.4\text{V}$	± mV max
Input Offset Voltage Temperature Coefficient (RTI)	TCV_{IO}	– 1			50	$f_{\text{CLOCK}} = 1\text{MHz}$	± $\mu\text{V}/^\circ\text{C}$ max
Input Resistor	R_{I}	– 1	20.2	20.2			k Ω max
			19.8	19.8			k Ω min
Input Resistor Temperature Coefficient	TCR_{IN}	– 1			100		± ppm/°C max
Op Amp Input Bias Current	I_{IB}	– 1	20	20		$V_{\text{IN}} = 0\text{V}$, Inverting Input	± nA max
			50	50		$V_{\text{IN}} = 0\text{V}$, Noninverting Input	nA max
Op Amp Input Offset Current	I_{OS}	– 1	70	70		$V_{\text{IN}} = 0\text{V}$	nA max
Op Amp Input Offset Voltage	V_{OS}	– 1	3	3		$V_{\text{IN}} = 0\text{V}$	± mV max
Op Amp Output Voltage Range	V_{R}	– 1	11	11		$V_S = \pm 15\text{V}$, Op-Amp Railed High	V min
			– 1	– 1		$V_S = \pm 15\text{V}$, Op-Amp Railed Low	V max
Max Clock Frequency	f_{CLOCK}	– 1	4	4		$V_{\text{IN}} = 0.01, 9.4\text{V}$	MHz min
Clock Threshold Voltage	V_{CT}	– 1			2.0	Referred to Pin 12	V max
					0.8	Referred to Pin 12	V min
Clock Input Current	I_{C}	– 1	20	20		Pin 10 = 0V dc	μA max
Low Level Output Voltage	V_{OL}	– 1	0.8	0.8		$I_{\text{OUT}} = 15\text{mA}$	V max
			0.4	0.4		$I_{\text{OUT}} = 10\text{mA}$	V max
					0.4	$I_{\text{OUT}} = 8.0\text{mA}$	V max
Leakage Current	I_{L}	– 1	10	10		$V_{\text{OUT}} = 36\text{V}$	μA max
Delay Time Positive Clock Edge to Output Pulse	t_{D}	– 1	150	150		$f_{\text{CLOCK}} = 200\text{kHz}$ Pin 9 to Pin 1	ns min
			250	250		$f_{\text{CLOCK}} = 200\text{kHz}$ Pin 9 to Pin 1	ns max
Output Pulse Width	t_{PW}	– 1	1	1		$C_{\text{OS}} = 300\text{pF}$	μs min
			2	2		$C_{\text{OS}} = 300\text{pF}$	μs max
Reference Voltage	V_{REF}	– 1	5.05	5.05		$I_{\text{REF}} = 0\text{mA}$	V max
			4.95	4.95		$I_{\text{REF}} = 0\text{mA}$	V min
Reference Voltage Temperature Coefficient	TCV_{REF}	– 1	100		100	$I_{\text{REF}} = 0\text{mA}$	± ppm/°C max
Quiescent Current	$+ I_{\text{SS}}$	– 1	15	15		$V_S = \pm 15\text{V}$, $V_{\text{IN}} = 0.1\text{V}$	mA max
	$- I_{\text{SS}}$	– 1	15	15		$V_S = \pm 15\text{V}$, $V_{\text{IN}} = 0.1\text{V}$	– mA max

NOTES

¹ $V_S = \pm 15\text{V}$, unless otherwise specified. $0.1\mu\text{F}$ decoupling capacitors from $+V_S$ to ground and $-V_S$ to ground.

²Nonlinearity is defined as the deviation from a straight line from zero to full scale, expressed as a fraction of full scale.

³Offset is guaranteed adjustable to zero using a $10\text{k}\Omega$ potentiometer on Pins 2 and 3 with the wiper connected to $+V_S$ through a $250\text{k}\Omega$ resistor.

Table 1.

1.1 Scope.

This specification covers the detail requirement for a 12-bit multiplying, good, voltage output, digital-to-analog converter with readback and selectable modes.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD664TD-UNI/883B
-2	AD664TD-BIP/883B
-3	AD664TE/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Type	Package	Description
D	D-28	28-Pin Ceramic DIP
E	E-44A	44-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{LL} to DGND	0 to +7 V
V_{CC} to DGND	0 to +18 V
V_{EE} to DGND	-18 V to 0 V
Soldering	+300°C, 10 sec
Power Dissipation	1000 mW
AGND to DGND	-1 V to +1 V
Reference Input	-11 V to +11 V
V_{CC} to V_{EE}	0 to +36 V
Digital Inputs	-0.3 V to +7 V
Analog Outputs	Indefinite Shorts to V_{CC} , V_{LL} , V_{EE} and GND

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= 25°C/W for D-28
θ_{JA}	= 60°C/W for D-28
θ_{JC}	= 42°C/W for E-44A
θ_{JA}	= 125°C/W for E-44A

AD664 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Resolution	RES	-1, 2, 3	12	12	12		Bits
Relative Accuracy	RA	-1, 2, 3	1/2	1/2	3/4		± LSB max
Differential Nonlinearity	DNL	-1, 2, 3	3/4	3/4	1	Major Carry Errors	± LSB max
Gain Error	A _E	-1, 2, 3	5	5		All Bits On	± LSB max
Gain Tempco	TCA _E	-1, 2, 3	10		10	All Bits On	± ppm/°C max
Unipolar Offset Error	V _{OS}	-1, 3	1	1		All Bits Off	± LSB max
Unipolar Offset Tempco	TC V _{OS}	-1, 3	2		2	All Bits Off	ppm/°C
Bipolar Zero Error ²	B _{PZE}	-2, 3	2	2		MSB On, All Others Off	± LSB max
Bipolar Zero Tempco	TC _{PZE}	-2, 3	10		10	MSB On, All Others Off	ppm/°C max
Reference Input Resistance	R _{IN}	-1, 2, 3	1.3–2.6	1.3			kΩ min
				2.6			kΩ max
Ref Voltage Range ³	V _{REF}	-1, 2, 3	V _{EE} + 2, V _{CC} - 2				Volts
Voltage Output, UNI ⁴	V _{OU}	-1, 3	0, V _{CC} - 2				Volts
Voltage Output, BIP ⁴	V _{OB}	-2, 3	V _{CC} - 2, V _{EE} + 2				Volts
Output Current	I _{OUT}	-1, 2, 3	5				mA min
I Short Circuit	I _{SC}	-1, 2, 3	40				mA max
Output Voltage Settling Time	t _{SL}	-1, 2, 3	10				μs max
Power Supply Rejection Ratio	PSRR	-1, 2, 3	5	5		All Bits On	ppm/%
Power Supply Current	I _{LL}	-1, 2, 3	1	5		V _{CC} = +16.5 V, V _{EE} = -16.5 V	mA max
	I _{CC}	-1, 2, 3	15	15		I _{CC} : All Bits On	
	I _{EE}	-1, 2, 3	19	19		I _{CC} : All Bits Off	
Gain Matching Error ⁵	mA _E	-1, 2, 3	4	4			± LSBs max
Bipolar Zero Matching Error ⁶	mB _{PZE}	-2, 3	2	2			± LSBs max
Offset Matching Error ⁷	mV _{OS}	-1, 3	1	1			± LSBs max
Digital In High Voltage	V _{IH}	-1, 2, 3	2.0	2.0			Volts max
Digital In Low Voltage	V _{IL}	-1, 2, 3	0.8	0.8	0.8		Volts min
Digital In High Current	I _{IH}	-1, 2, 3				V _{IN} = V _{LL} :	
			10	10	10	$\overline{\text{CS}}/\text{DS0}/\text{DS1}/\text{RST}/\text{RD}/\text{LS}$	± μA max
			10	10	10	$\overline{\text{MS}}/\text{TR}^8$	± μA max
			10	10	10	$\overline{\text{QS0}}/\text{QS1}/\text{QS2}^8$	- μA min
			120	120	120		+ μA max
Digital In Low Current	I _{IL}	-1, 2, 3				V _{IN} = DGND:	
			10	10	10	$\overline{\text{CS}}/\text{DS0}/\text{DS1}/\text{RST}/\text{RD}/\text{LS}$	± μA max
			150	150	150	$\overline{\text{MS}}/\text{TR}^8$	- μA max
			0	0	0		μA max
			10	10	10	$\overline{\text{QS0}}/\text{QS1}/\text{QS2}^8$	± μA max
Digital Out Low Voltage	V _{OL}	-1, 2, 3	0.4	0.4	0.4		+ Volts max
Digital Out High Voltage	V _{OH}	-1, 2, 3	2.4	2.4	2.4		+ Volts min
Power Supply Gain Sensitivity	PSGS	-1, 2, 3		5		11.4 V ≤ V _{CC} ≤ 16.5 V	± ppm/%
				5		-16.5 V ≤ V _{EE} ≤ -11.4 V	± ppm/%
				5		4.5 V ≤ V _{LL} ≤ 5.5 V	± ppm/%

Table 1. (Continued on next page)

NOTES

¹ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $50\ \Omega$ resistor Pin 6 to Pin 7, A0, A1, A2, A3, $\overline{CS} = \text{Logic "0"}$, $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, unipolar configuration.

²Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.

³A minimum power supply of $\pm 12.0\text{ V}$ is required for a 10 V reference voltage.

⁴A minimum power supply of $\pm 12.0\text{ V}$ is required for 0 to $+10\text{ V}$ and $\pm 10\text{ V}$ operation. A minimum power supply of $\pm 11.4\text{ V}$ is required for -5 V to $+5\text{ V}$ operation.

⁵Gain error matching is the largest difference in gain error between any two DACs in one package.

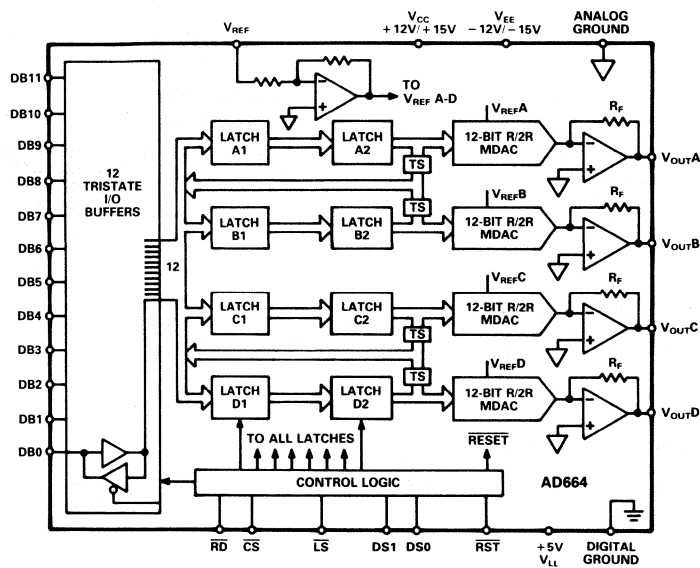
⁶Bipolar zero matching is the largest difference in bipolar zero error between any two DACs in one package.

⁷Offset error matching is the largest difference in offset error between any two DACs in one package.

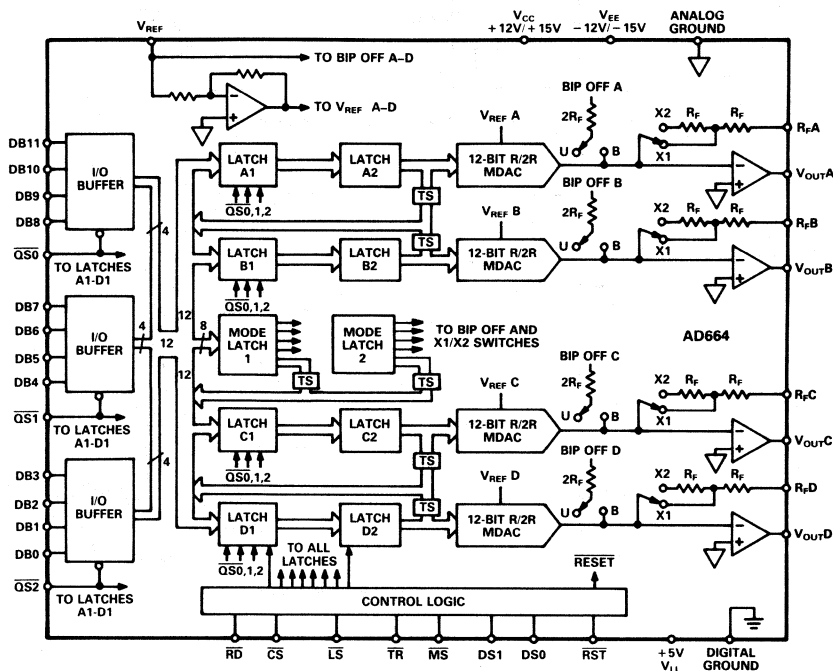
⁸44-pin versions only.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



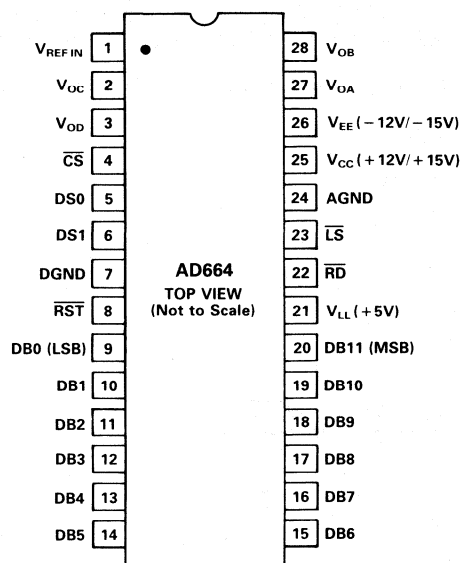
28-Pin Block Diagram



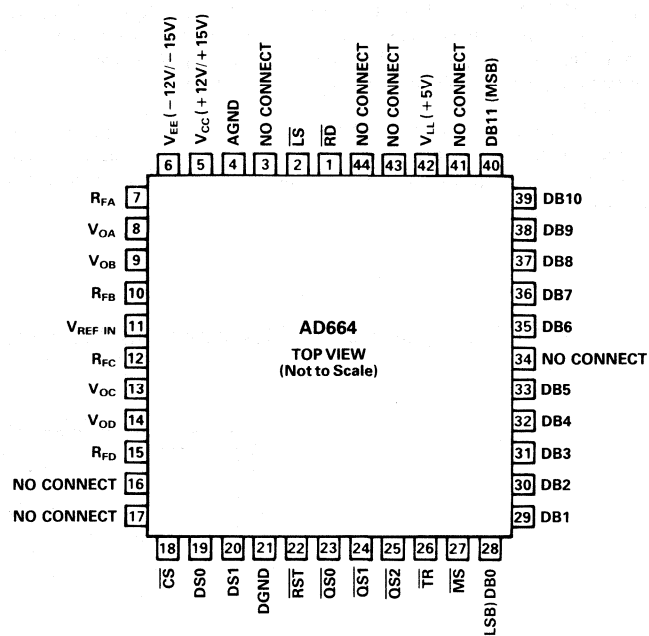
44-Pin Block Diagram

AD664

D Package (DIP)



E Package (LCC)

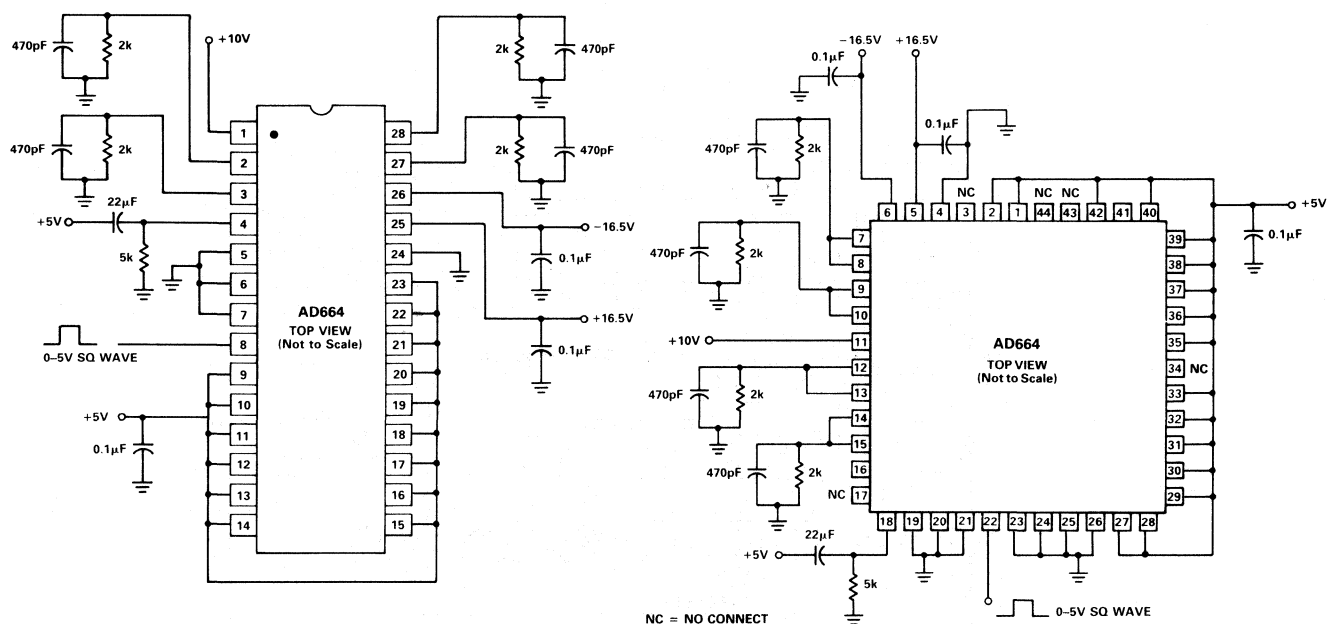


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Digital Timing Specifications

Parameter	Symbol	Min	Limit Typ	Max	Units
Data Input Mode (Figure 1)					
$\overline{\text{CS}}$ Pulse Width	t_W	80			ns
Data Setup	t_{DS}	0			ns
Data Hold	t_{DH}	100			ns
Address Setup	t_{AS}	0			ns
Address Hold	t_{AH}	30			ns
$\overline{\text{LS}}$ Setup	t_{LS}	0			ns
$\overline{\text{LS}}$ Hold	t_{LH}	30			ns
Data Input Mode (Figure 3)					
Data Setup	t_{DS}	0			ns
Data Hold	t_{DH}	0			ns
$\overline{\text{LS}}$ Width	t_{LW}	80			ns
$\overline{\text{LS}}$ Setup	t_{LS}	0			ns
$\overline{\text{CS}}$ Hold	t_{CH}	50			ns
Address Setup	t_{AS}	0			ns
Address Hold	t_{AH}	30			ns
Mode Select (Figure 5)					
$\overline{\text{LS}}$ Setup	t_{LS}	20			ns
Address Setup	t_{AS}	0			ns
Data Setup	t_{DS}	0			ns
$\overline{\text{LS}}$ Width	t_{LW}	80			ns
$\overline{\text{CS}}$ Hold	t_{CH}	260			ns
Data Hold	t_{DH}	0			ns
$\overline{\text{MS}}$ Hold	t_{MH}	0			ns
Mode Select (Figure 7)					
Mode Select	t_{MS}	20			ns
$\overline{\text{MS}}$ Hold	t_{MH}	0			ns
$\overline{\text{LS}}$ Setup	t_{LS}	0			ns
Data Setup	t_{DS}	0			ns
$\overline{\text{CS}}$ Width	t_W	80			ns
$\overline{\text{LS}}$ Hold	t_{LH}	85			ns
Data Hold	t_{DH}	100			ns
Readback Mode (Figure 8, 10)					
Address Setup	t_{AS}	20			ns
Address Hold	t_{AH}	30			ns
$\overline{\text{RD}}$ Setup	t_{RS}	20			ns
$\overline{\text{RD}}$ Hold	t_{RD}	30			ns
$\overline{\text{MS}}$ Setup	t_{MS}	20			ns
$\overline{\text{MS}}$ Hold	t_{MH}	30			ns
Data Access	t_{DV}			240	ns
Data Release	t_{DF}			75	ns
Asynchronous Reset (Figure 11)					
Reset Width	t_W	90			ns

Timing specifications are relative to $\overline{\text{CS}}$. $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $V_{REF} = +10\text{ V}$, $T_A = +25^\circ\text{C}$. Specifications are guaranteed but not tested. Refer to Figures 1–11

Table 2.

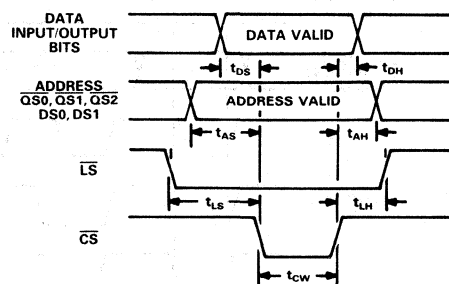


Figure 1. Preload First Rank of a DAC

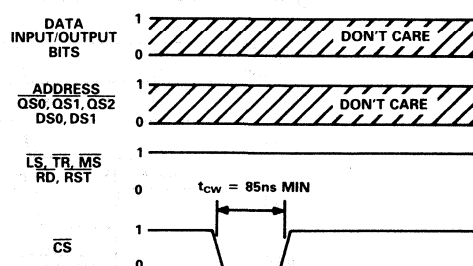


Figure 2. Update Second Rank of a DAC

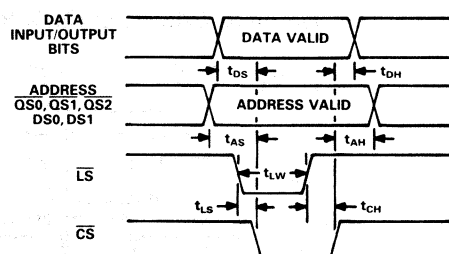


Figure 3. Update Output of a Single DAC

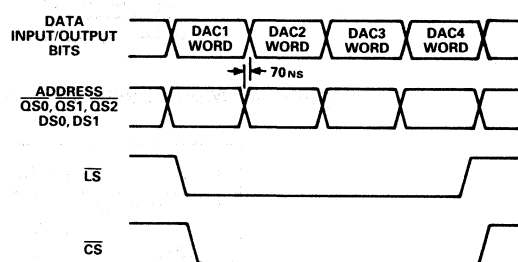


Figure 4. Update All DAC Outputs

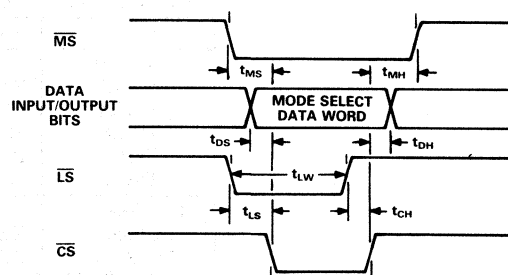


Figure 5. Load and Update Mode of One DAC

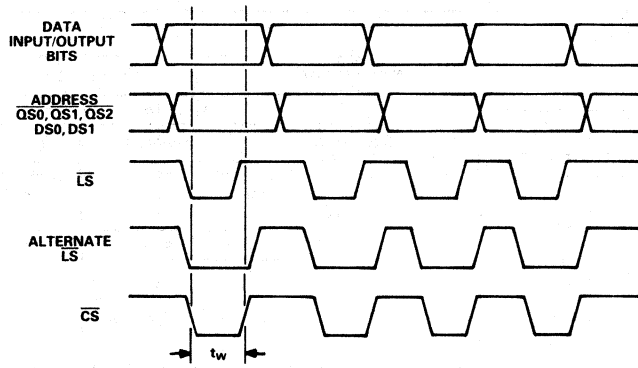


Figure 6. Load and Update Multiple DACs

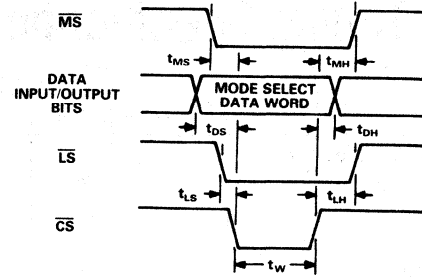


Figure 7. Preload Mode Select Register

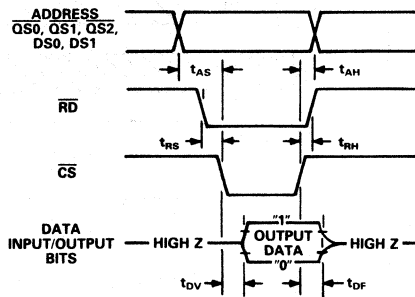


Figure 8. DAC Input Code Readback

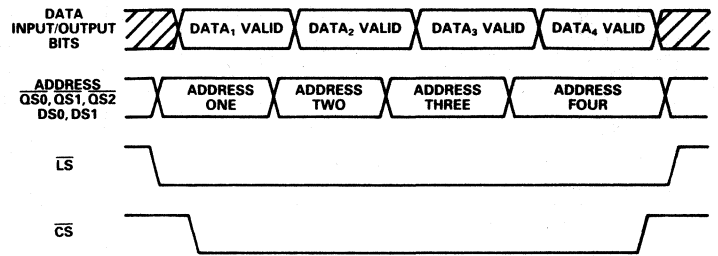


Figure 9. Preload First Rank Registers

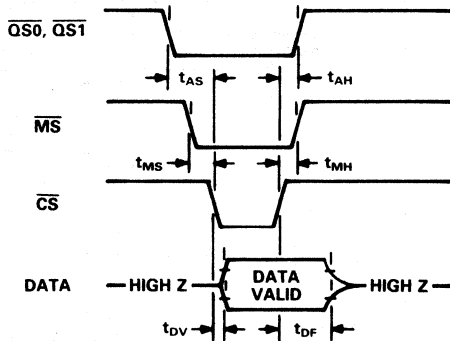


Figure 10. Mode Select Readback

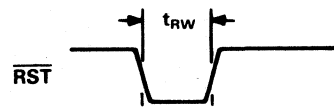


Figure 11. Asynchronous Reset Operation

Function	DS1, DS0	LS	MS	TR	QS0, I, 2 ¹	RD	CS	RST
Load 1st Rank								
DACA	00	0	1	1	Select Quad	1	1→0	1
DACB	01	0	1	1	Select Quad	1	1→0	1
DACC	10	0	1	1	Select Quad	1	1→0	1
DACD	11	0	1	1	Select Quad	1	1→0	1
Load 2nd Rank	XX	1	1	1	XXX	1	1→0	1
Read 2nd Rank	Select D/A	X	1	1	Select Quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
Transparent ¹								
All DACs	XX	1	1	0	000	1	1→0	1
DACA	00	0	1	0	000	1	1→0	1
DACB	01	0	1	0	000	1	1→0	1
DACC	10	0	1	0	000	1	1→0	1
DACD	11	0	1	0	000	1	1→0	1
Mode Select ^{1,2}								
1st Rank	XX	0	0	1	00X	1	1→0	1
2nd Rank	XX	1	0	1	XXX	1	1→0	1
Readback Mode ¹	XX	X	0	1	00X	0	1→0	1

NOTES

X = Don't care.

¹For 44-pin versions only.

²For MS, TR, LS = 0, a MS 1st write occurs.

Table 3. AD664 Truth Table

1.1 Scope.

This specification covers the detail requirements for a complete 12-bit digital-to-analog converter with microprocessor interface, buried Zener reference and output amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	AD667S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28A	28-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Power Ground	0 to +18V
V_{EE} to Power Ground	0 to –18V
Digital Inputs (Pins 11-15, 17-28) to Power Ground	–1.0V to +7.0V
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Ref Out, V_{OUT} (Pins 6, 9)	Indefinite Short to Power Ground Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= 25°C/W for D-28
θ_{JA}	= 60°C/W for D-28
θ_{JC}	= 42°C/W for E-28A
θ_{JA}	= 125°C/W for E-28A

AD667 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1/2	1/2	3/4	All Bits with Positive Errors On. All Bits with Negative Errors On	± LSB max
Differential Nonlinearity	DNL	– 1	3/4	3/4	1	Major Carry Errors	± LSB max
Gain Error ²	A _E	– 1	0.20	0.20		All Bits On	± % FSR max
Gain Temperature Coefficient	TCA _E	– 1	30		30	All Bits On	± ppm/°C max
Unipolar Offset Error	V _{OS}	– 1	2	2		All Bits Off	± LSB max
Temperature Coefficient Unipolar Offset	TCV _{OS}	– 1	3		3	All Bits Off	± ppm/°C max
Bipolar Zero Error ²	B _{PZE}	– 1	0.10	0.10		MSB On, All Other Bits Off Bipolar Mode	± % FSR max
B/P Zero Temperature Coefficient	TCB _{PZE}	– 1	10		10	MSB On, All Other Bits Off Bipolar Mode	± ppm/°C max
Input Resistance	R _{IN}	– 1	15				kΩ min
			25				kΩ max
Reference Output Voltage ³	V _{REF}	– 1	9.9	9.9	9.9	Bipolar Mode, V _S = ± 11.4 0.1mA External Load	+ V min
			10.10	10.10	10.10		+ V max
Output Current	I _{OUT}	– 1	5				± mA min
Output Short-Circuit Current	I _{SC}	– 1	40				+ mA max
Latch Functionality	A _{EA}	– 1	1	1	1	See Notes 4 & 5	± LSB max
Latch Functionality	V _{OSA}	– 1	1	1	1	See Note 4	± LSB max
Power Supply Rejection Ratio	PSRR	– 1	10	10		All Bits On + 11.4V ≤ V _{CC} ≤ + 16.5V	ppm of FSR/% max
			10	10		All Bits On – 11.4V ≤ V _{EE} ≤ – 16.5V	
Power Supply Current	I _{CC}	– 1	12	12		V _{CC} = + 16.5V, V _{EE} = – 16.5V I _{CC} : All Bits On I _{EE} : All Bits On	+ mA max
	I _{EE}	– 1	25	25			– mA max
Digital Input High Voltage	V _{IH}	– 1	2.0	2.0	2.0		+ V min
			5.5				+ V max
Digital Input Low Voltage	V _{IL}	– 1	0.8	0.8	0.7		+ V max
Digital Input High Current	I _{IH}	– 1	10	10		V _{IH} = 5.5V	+ μA max
Digital Input Low Current	I _{IL}	– 1	5	5		V _{IL} = 0.0V	+ μA max
Data Setup Time ⁶	t _{DC}	– 1	50				ns min
Data Hold Time ⁶	t _{DH}	– 1	0				ns min
CS Pulse Width ⁶	t _{CP}	– 1	100				ns min
Address Valid End of CS ⁶	t _{AC}	– 1	100				ns min
Output Voltage Settling Time ⁶	t _{SL}	– 1	4			R _{FB} = 10k R _L = 2k 500pF	μs max
			3			R _{FB} = 5k See Figure 1	

NOTES

¹V_{CC} = + 15V, V_{EE} = – 15V, 50Ω resistor Pin 6 to Pin 7, A₀, A₁, A₂, A₃, CS = LOGIC “0”, V_{IH} = 2.0V, V_{IL} = 0.8V, Unipolar configuration unless otherwise specified.

Unipolar Configuration – Pins 1 and 2 to Pin 9, Pin 4 to Pin 5.

Bipolar Configuration – Pin 1 to Pin 9, 50Ω resistor Pin 4 to Pin 6.

²Adjustable to 0.

³In subgroup 1, the reference output is loaded with 0.5mA nominal reference current, 1.0mA bipolar offset current and 0.1mA additional current.

In subgroups 2 and 3, only the 0.5mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

⁴All bits low, A₀, A₁, A₂, A₃ LOGIC “0”; A₀, A₁, A₂, A₃ initialized to LOGIC “1”, each 4-Bit register set to LOGIC “1”, and A₀, A₁, A₂ set sequentially to LOGIC “0” and back to LOGIC “1” to latch data into first rank.

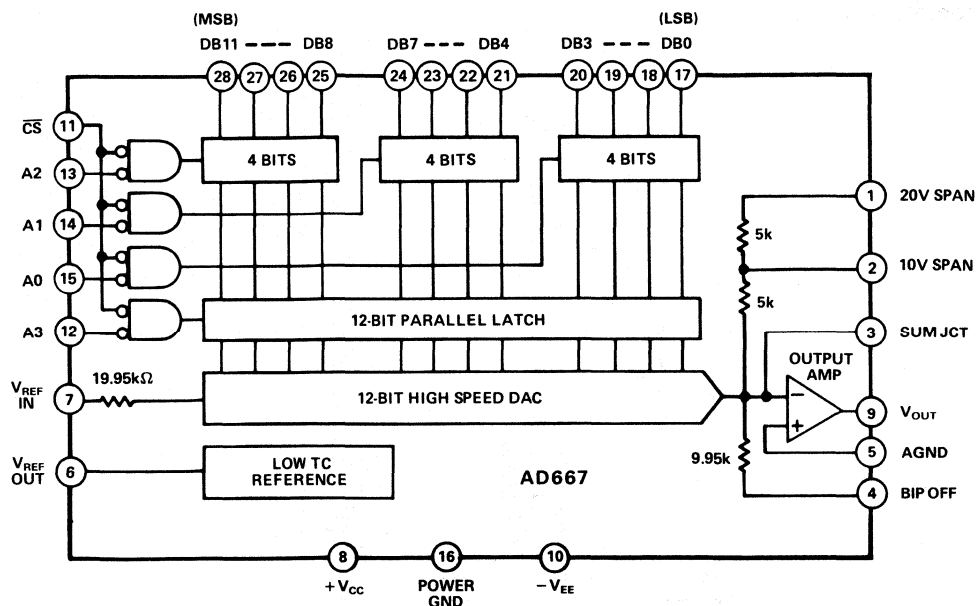
⁵A₃ set to LOGIC “0” and back to LOGIC “1” to latch full-scale output into second rank.

⁶See Figure 1 and Table 2.

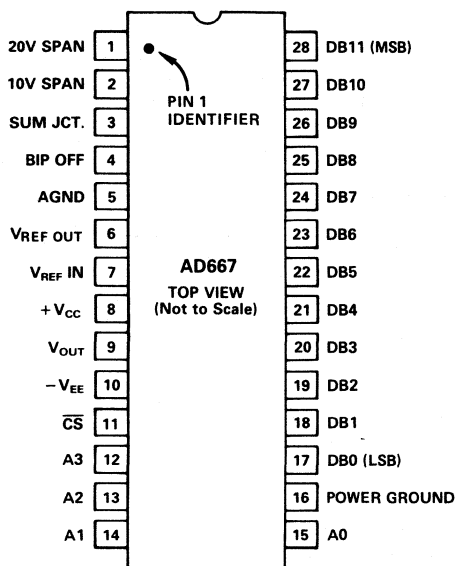
Table 1.

REV. C

3.2.1 Functional Block Diagram and Terminal Assignments.

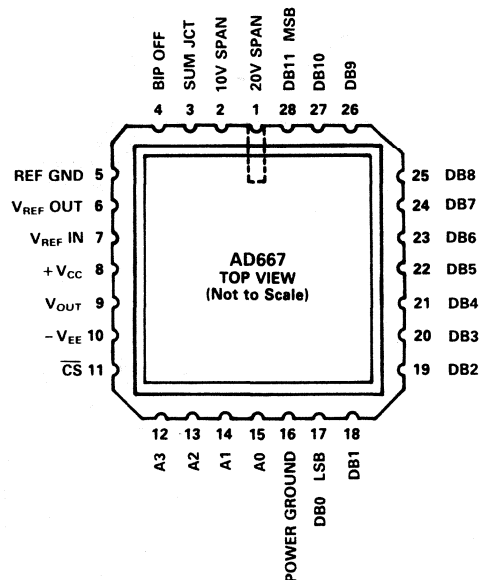


D Package (DIP)



*NOTE DIP PACKAGE PIN NUMBERS AND LCC CONTACT NUMBERS SERVE THE SAME FUNCTION.

E Package (LCC)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

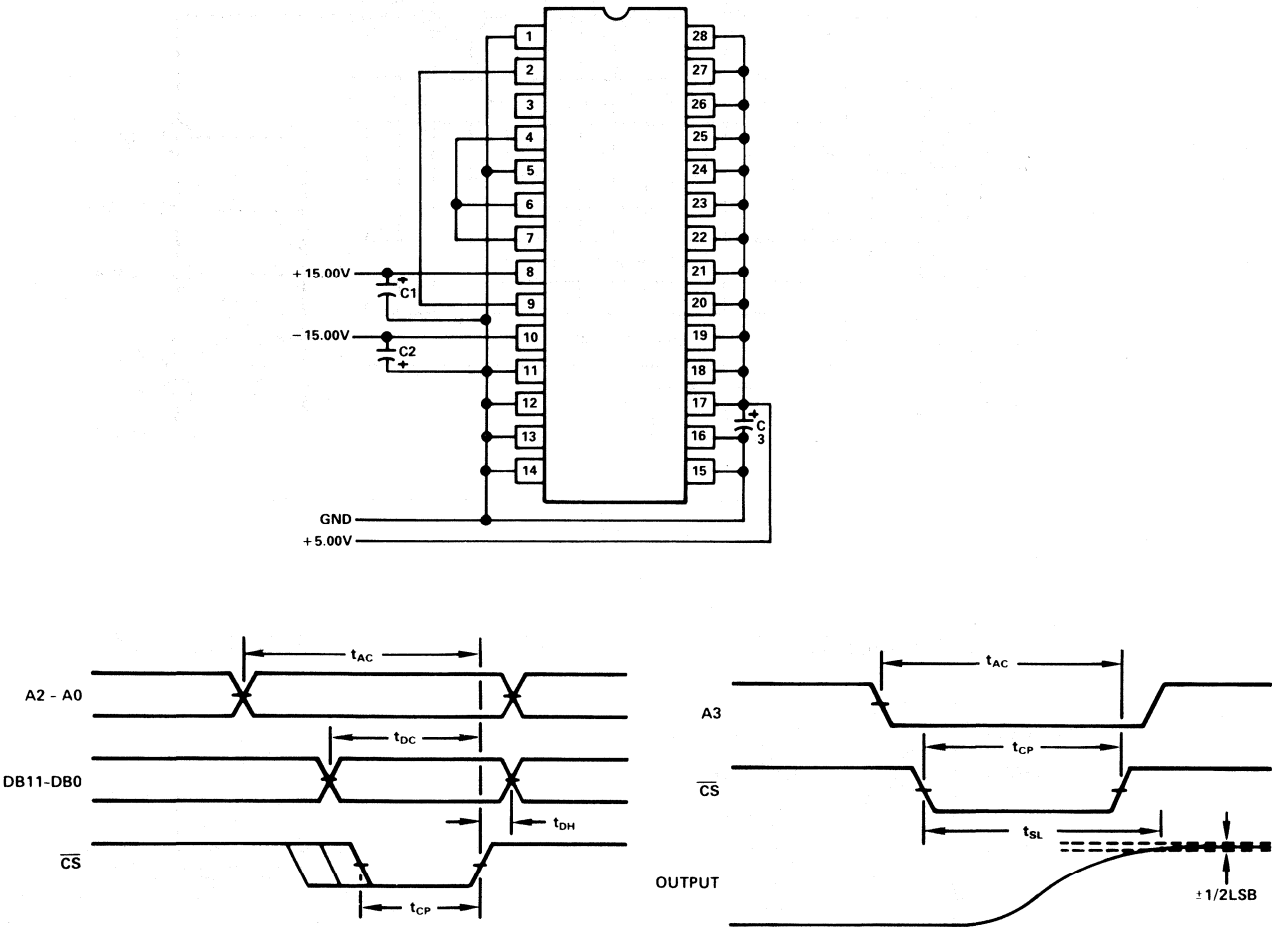


Figure 1.

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table 2. AD667 Truth Table

1.1 Scope.

This specification covers the detail requirements for a complete single supply 8-bit resolution A/D converter with an instrumentation input amplifier, and complete microprocessor interface.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD670S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-20	20-Pin DIP
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Ground	0V to +7.5V
Digital Inputs (Pins 11-15)	–0.5V to $V_{CC} + 0.5V$
Digital Outputs (Pins 1-9)	Momentary Short to V_{CD} or Ground
Analog Inputs (Pins 16-19)	–30V to +30V
Power Dissipation	450mW
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering to Specs)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 85^\circ\text{C/W}$

AD670 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Relative Accuracy ²	RA	– 1	1/2	1/2	1				+ LSB max
Differential Nonlinearity ³	DNL	– 1	8	8	8				+ Bits max
Gain Error ²	A _E	– 1	1.5	1.5	2.5				± LSB max
Unipolar Offset Error	O _E	– 1	1	1	2			2.55V Input Range	± LSB max
Bipolar Zero Error	B _{POE}	– 1	1	1	2			± 1.28V FS	± LSB max
Input Resistance	R _{IN}	– 1	8 12	8 12	8 12			2.55V Input Range 2.55V Input Range	kΩ min kΩ max
Input Bias Current	I _B	– 1	750	750	750			255mV Input Range	+ nA max
Input Offset Current	I _{OS}	– 1	200	200	200				+ nA max
Absolute Input Signal Range ⁴	V _{ABS}	– 1	0.34	0.34	0.15			255mV Input Range	– V min
			V _{CC} – 3.3	V _{CC} – 3.3	V _{CC} – 3.5			255mV Input Range	+ V max
			3.4	3.4	1.5			2.55V Input Range	– V min
			V _{CC}	V _{CC}	V _{CC}			2.55V Input Range	+ V max
Common-Mode Rejection ⁵	CMR	– 1	1	1 ⁶	2 ⁷			255mV	± LSB max
Three-State Leakage Current	I _{OZ}	– 1	40	40	40				± μA max
Power Supply Rejection Ratio	PSRR	– 1	0.015	0.015	0.015			2.55V FS V _{CC} = +4.75V to +5.5V	± %FS/% max
Power Supply Current	I _{CC}	– 1	45	45	45				+ mA max
Digital Input High Voltage	V _{IH}	– 1	2.0	2.0	2.0				+ V min
Digital Input Low	V _{IL}	– 1	0.8	0.8	0.7				+ V max
Digital Input High Current	I _{IH}	– 1	100	100	100				+ μA max
Digital Input Low Current	I _{IL}	– 1	100	100	100				– μA min
Digital Output Low Voltage	V _{OL}	– 1	0.4	0.4	0.4			I _{OL} = –1.6mA	+ V max
Digital Output High Voltage	V _{OH}	– 1	2.4	2.4	2.4			I _{OH} = 0.5mA	+ V min
Conversion Time	TC	– 1	10			10	13		μs max
Write/Start Pulse Width	t _W	– 1	300			300	300	See Note 6	ns min
Input Data Setup Time	t _{DS}	– 1	200						ns min
Input Data Hold Time	t _{DH}	– 1	10						ns min
Read/Write Setup Before Control	t _{RWC}	– 1	0						ns min
Status Delay	t _{DC}	– 1	700						ns max
Delay From Status to Data Read	t _{SD}	– 1	250						ns max
Bus Access Time	t _{TD}	– 1	250			250			ns max
Data Hold Time	t _{DH}	– 1	25						ns max
Output Float Delay	t _{DT}	– 1	150			150			ns max
Read Time	t _r	– 1	250						ns min

NOTES

¹T_A = +25°C, V_S = +5V.

²Tested on both 2.56V full scale and ± 1.28V full scale.

³Minimum resolution for which there are no missing codes.

⁴Input signal range is with respect to Power Ground (Pin 10).

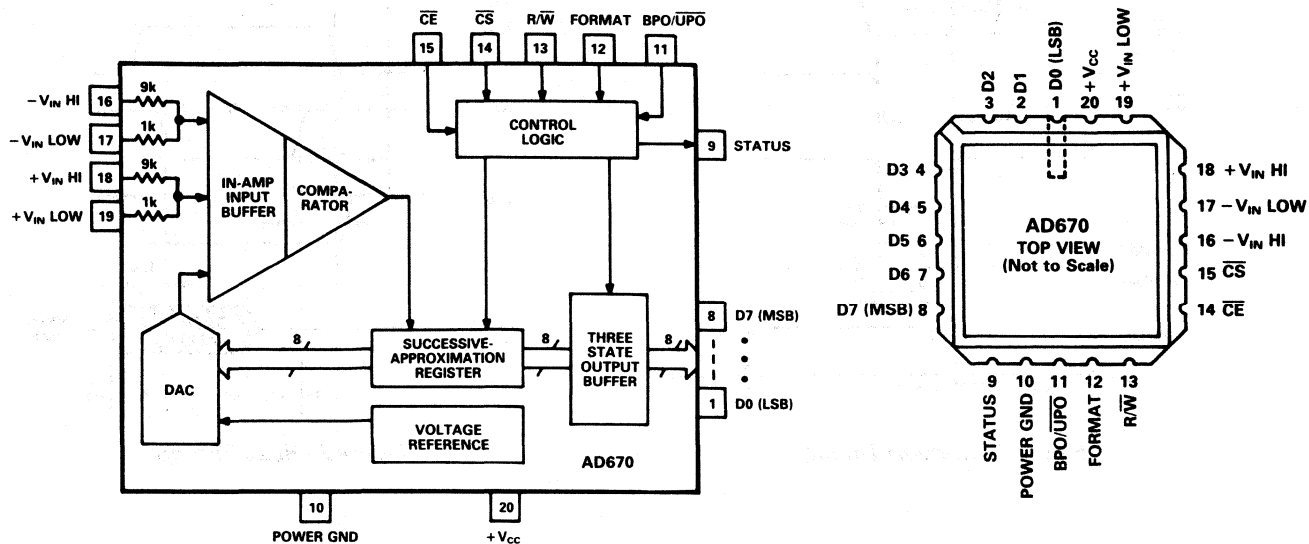
⁵Digital output code will not change by more than 1LSB with full scale applied to the differential inputs over the input signal range.

Timing per Figures 1, 2 or 3.

⁶V_{CM} = 0 to –0.34V; V_{CM} = 0 to V_{CC} – 3.6V.

⁷V_{CM} = 0 to –0.15V; V_{CM} = 0 to V_{CC} – 3.8V.

3.2.1 Functional Block Diagrams and Terminal Assignments.

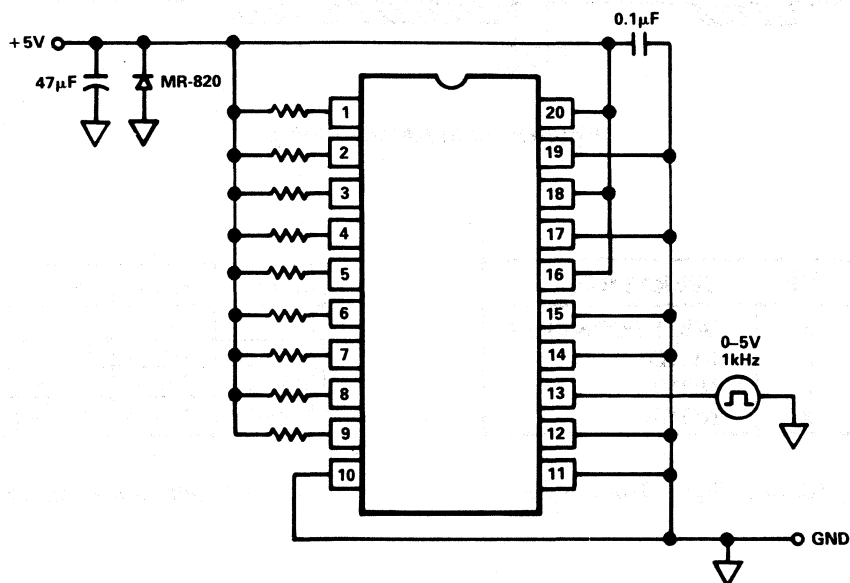


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS ARE 3k Ω , 1%, 1/4 WATT.

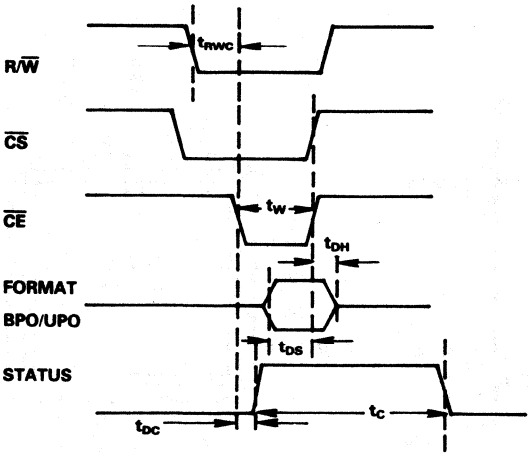


Figure 1. Convert Timing

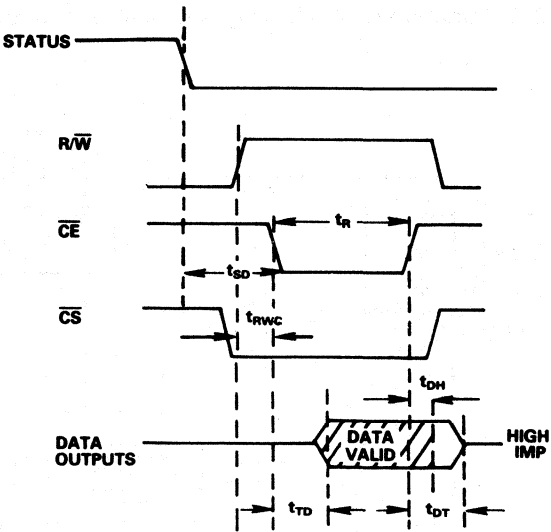


Figure 2. Read Timing

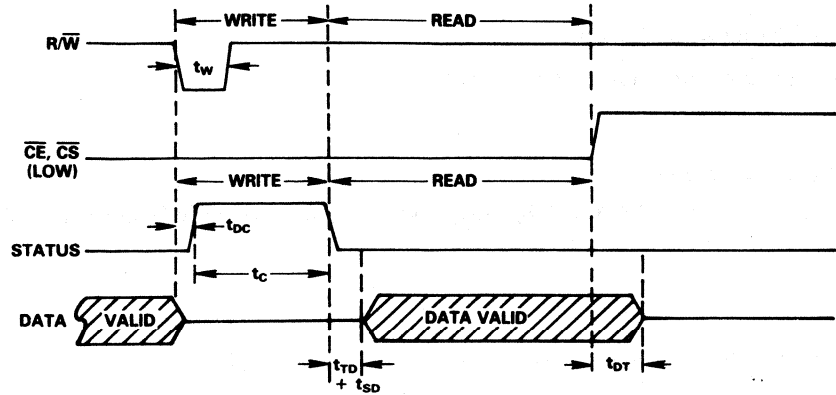


Figure 3. Stand-Alone Timing

R/W	CS	CE	OPERATION
0	0	0	WRITE/CONVERT
1	0	0	READ
X	X	1	NONE
X	1	X	NONE

Table 2. AD670 Control Signal Truth Table

Mode	Range	Min	Max	Unit
Unipolar	LOW	0	255	mV
Unipolar	HIGH	0	2.55	V
Bipolar	LOW	-128	127	mV
Bipolar	HIGH	-1.28	1.27	V

Table 3. Differential Input Signal Range

1.1 Scope.

This specification covers the detail requirements for a 12-bit resolution A/D converter with complete microprocessor interface and a high performance buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
- 1	AD674ASD/883B
- 2	AD674ATD/883B
- 3	AD674AUD/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Digital Common	+ 16.5V
V_{EE} to Digital Common	- 16.5V
V_{LOGIC} to Digital Common	+ 7V
Analog Common to Digital Common	$\pm 1V$
Control Inputs (CE, $\overline{CS}$, A_O , $12/\overline{8}$, $R/\overline{C}$) to Digital Common	- 0.5V to $V_{LOGIC} + 0.5V$
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common	$\pm 16.5V$
$20V_{IN}$ to Analog Common	$\pm 24V$
REF OUT	Indefinite Short to Common Momentary Short to V_{CC}
Power Dissipation	833mW
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$ for D-28
 $\theta_{JA} = 60^\circ\text{C/W}$ for D-28

AD674A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Power Dissipation	P _D	– 1, 2, 3	720	720			Tristated Outputs	mW max
Input Resistance	R _{IN}	– 1, 2, 3	3	3			10V Span	kΩ min
			7	7				kΩ max
			6	6			20V Span	kΩ min
			14	14				kΩ max
Internal Reference Output Voltage	V _{REF}	– 1, 2, 3	+ 9.9 + 10.1	+ 9.9 + 10.1			Bipolar 20V Span 2.0mA External Load	V min V max
Logic Input High Voltage ² CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O	V _{IH}	– 1, 2, 3	2.0	2.0	2.0			+ V min
Logic Input Low Voltage ² CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O	V _{IL}	– 1, 2, 3	0.8	0.8	0.8			+ V max
Logic Input Current CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A _O	I _{LIN}	– 1, 2, 3	100	100	100		V _{IH} = 5.0V V _{IL} = 0.0V	± μA max
Logic Output High Voltage DB11–DB0	V _{OH}	– 1, 2, 3	2.4	2.4	2.4		I _{SOURCE} = 500μA	+ V min
Logic Output Low Voltage DB11–DB0, STS	V _{OL}	– 1, 2, 3	0.4	0.4	0.4		I _{SINK} = 1.6mA	+ V max
Three-State Output Leakage DB11–DB0	I _{OLT}	– 1, 2, 3	20	20	20		Outputs Tristated V _{IH} = 5.0V	± μA max
Power Supply Current	I _L	– 1, 2, 3	40	40	40		Outputs Tristated	mA max
	I _{CC}	– 1, 2, 3	5	5	5			
	I _{EE}	– 1, 2, 3	29	29	29			
Integral Nonlinearity	INL	– 1	1	1	1		Major Transitions Unipolar 10V Span and Bipolar 20V Span	± LSB max
		– 2, 3	1/2	1	1	1/2		
Differential Nonlinearity ³	DNL	– 1	11	11	11		All Codes Tested Unipolar 10V Span and Bipolar 20V Span	Bits min
		– 2, 3	12	11	12	12		
Power Supply Rejection ⁴	PSR	– 1	2	2			See Note 5 Unipolar – 10V Span See Note 6 See Note 7	± LSB max
		– 2, 3	1	2				
	PSR	– 1, 2, 3	1/2	1/2		1		
	PSR	– 1	2	2				
		– 2, 3	1	2		1		
Unipolar Offset Error	V _{OSE}	– 1, 2, 3	2	2			10V Span	± LSB max
Unipolar Offset Drift	TC _{VOS}	– 1			2		10V Span	± LSB max
		– 2, 3			1			
Bipolar Offset Error	B _{POE}	– 1	10	10			20V Span	± LSB max
		– 2, 3	4	4				
Bipolar Offset Drift	TCB _{POE}	– 1			4		20V Span	± LSB max
		– 2			2			
		– 3			1			
Full-Scale Calibration Error	A _B	– 1, 2, 3	0.25	0.25			Bipolar 20V Span	± % of FSR max
	A _U	– 1, 2, 3	0.25				Unipolar 10V Span	± % of FSR max
Full-Scale Calibration Drift	TCA _E	– 1			50		Bipolar 20V Span	ppm/°C
		– 2			25			
		– 3			12.5			

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REV. A

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Test Condition ¹	Units
Full-Control Mode ¹								
STS Delay from CE	t _{DSC}	– 1, 2, 3	200			200	Timing Per Figure 1	ns max
CE Pulse Width	t _{HEC}	– 1, 2, 3	50			50	Timing Per Figure 1	ns min
Access Timing (from CE) ⁸	t _{DD}	– 1, 2, 3	150			150	Timing Per Figure 2	ns max
Output Float Delay ⁹	t _{HL}	– 1, 2, 3	150			150	Timing Per Figure 2	ns max
Data Valid After CE Low	t _{HD}	– 1, 2, 3	25			25	Timing Per Figure 2	ns min
Stand-Alone Mode ¹								
Low R/C Pulse Width	t _{HRL}	– 1, 2, 3	50			50	Timing Per Figure 3	ns min
High R/C Pulse Width	t _{HRH}	– 1, 2, 3	150			150	Timing Per Figure 3	ns min
STS Delay from R/C	t _{DS}	– 1, 2, 3	200			200	Timing Per Figure 3	ns max
Data Access Time ⁸	t _{DDR}	– 1, 2, 3	150			150	Timing Per Figure 3	ns max
Data Valid After R/C Low	t _{HDR}	– 1, 2, 3	25			25	Timing Per Figure 3	ns min
Conversion Time	t _C	– 1, 2, 3	15			15	To 12 Bits	μs max
			10			10	To 8 Bit	

NOTES

¹V_{CC} = +15V, V_{EE} = –15V, V_{LOGIC} = +5V, 12/8 connected to V_{LOGIC}, A_O and CS at logic “0,” CE at logic “1.”

10V Unipolar – 50Ω resistor Pin 8 to Pin 10, 50Ω resistor Pin 12 to ground. Analog input connected to Pin 13.

20V Bipolar – 50Ω resistor Pin 8 to Pin 12, 50Ω resistor Pin 8 to Pin 10. Analog input connected to Pin 14.

See Figures 1, 2 and 3 for timing information.

²V_{IH} = 2.0V min and V_{IL} = 0.8V max, guaranteed design limits –55°C to +125°C.

³Minimum resolution for which no missing codes are guaranteed.

⁴Change in the full-scale unipolar 10V span as power supply voltage is varied from min to max specified value.

⁵Test Conditions for PSRR:

13.5V ≤ V_{CC} ≤ 16.5V, V_{LOGIC} = 5V, V_{EE} = –15V

11.4V ≤ V_{CC} ≤ 12.6V, V_{LOGIC} = 5V, V_{EE} = –12V

⁶4.5V ≤ V_{LOGIC} ≤ 5.5V, V_{CC} = 15V, V_{EE} = –15V

⁷–16.5 ≤ V_{EE} ≤ –13.5V, V_{LOGIC} = 5V, V_{CC} = 15V

–12.6V ≤ V_{EE} ≤ –11.4V, V_{LOGIC} = 5V, V_{CC} = 12V

⁸See Figure 4.

⁹See Figure 5.

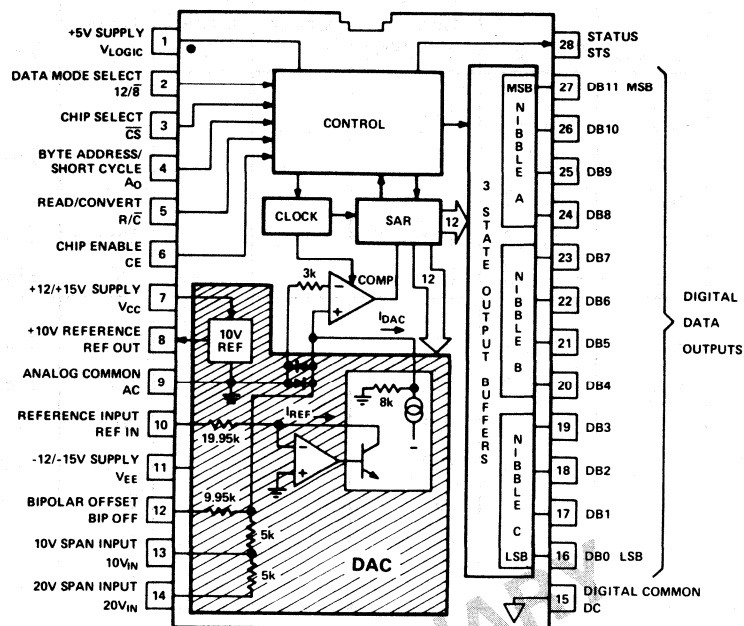
Table 1.

CE	CS	R/C	12/8/	A _O	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4LSBs and 4 Trailing Zeros

Table 2. Truth Table

AD674A

3.2.1 Functional Block Diagram and Terminal Assignments.

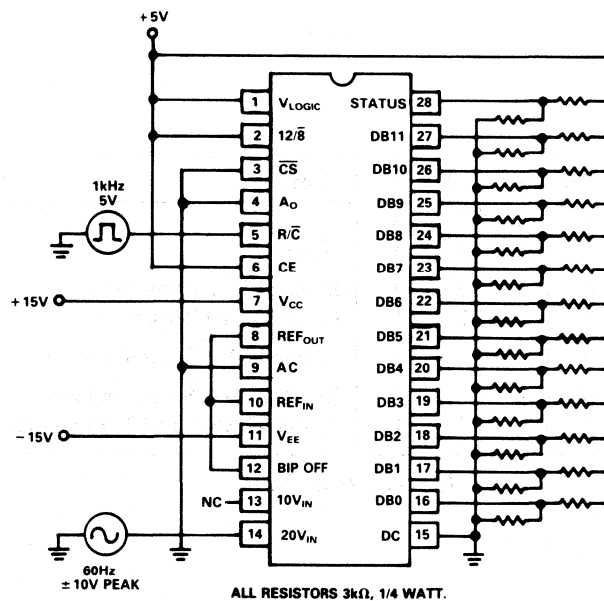


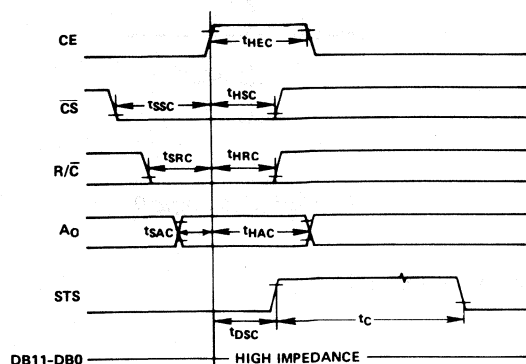
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

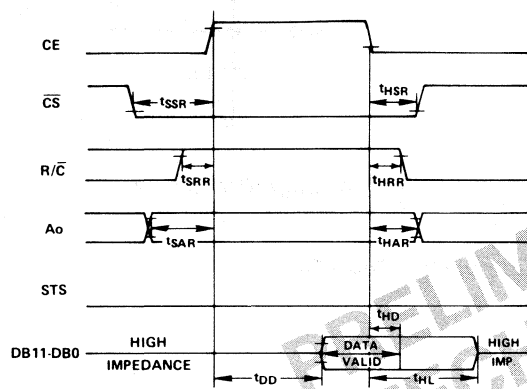
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Symbol	Parameter	Min	Max	Units
t_{DSC}	STS Delay from CE		200	ns
t_{HEC}	CE Pulse Width	50		ns
t_{SSC}	CS to CE Setup	50		ns
t_{HSC}	CS Low During CE High	50		ns
t_{SRC}	R/C to CE Setup	50		ns
t_{HRC}	R/C Low During CE High	50		ns
t_{SAC}	A ₀ to CE Setup	0		ns
t_{HAC}	A ₀ Valid During CE High	50		ns
t_C	Conversion Time			
	8-Bit Cycle	6	10	μs
	12-Bit Cycle	9	15	μs

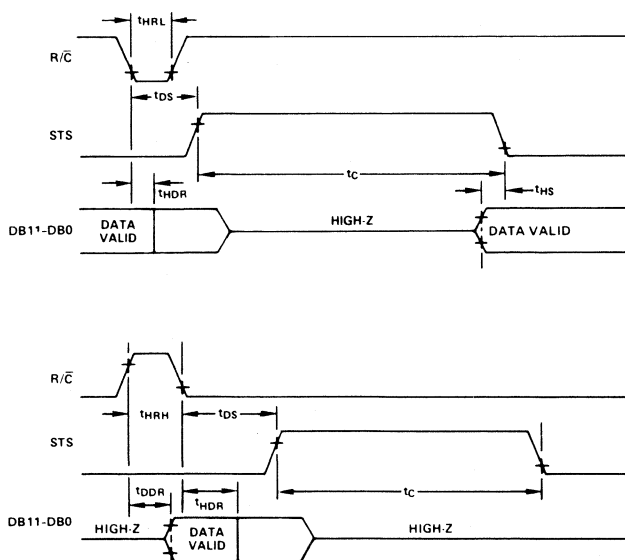
Figure 1. Convert Start Timing



Symbol	Parameter	Min	Max	Units
t_{DD}^1	Access Time (from CE)		150	ns
t_{HD}^2	Data Valid after CE Low	25		ns
t_{HL}^2	Output Float Delay		150	ns
t_{SSR}	CS to CE Setup	50		ns
t_{SRR}	R/C to CE Setup	0		ns
t_{SAR}	A ₀ to CE Setup	50		ns
t_{HSR}	CS Valid After CE Low	0		ns
t_{HRR}	R/C High After CE Low	0		ns
t_{HAR}	A ₀ Valid After CE low	50		ns

¹ t_{DD} is measured with the load circuit of Figure 4 and defined as the time required for an output to cross 0.4V or 2.4V.
² t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 5.

Figure 2. Read Timing



Symbol	Parameter	Min	Max	Units
t_{HRL}	Low R/C Pulse Width	50		ns
t_{DS}	STS Delay from R/C		200	ns
t_{HDR}	Data Valid After R/C Low	25		ns
t_{HS}	STS Delay After Data Valid	30	600	ns
t_{HRH}	High R/C Pulse Width	150		ns
t_{DDR}	Data Access Time		150	ns

Figure 3. Stand-Alone Mode Timing



Figure 4. Load Circuit for Access Timing Test



Figure 5. Load Circuit for Output Float Delay Test

PRELIMINARY
TECHNICAL
DATA

1.1 Scope.

This specification covers the detail requirements for a high precision, 8.192 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD689SQ/883B
-2	AD689TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{IN} to Ground	+36V
GND to GND Sense	$\pm 200\text{mV}$
Power Dissipation	500mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

AD689 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	– 1, 2	5	5				+ mA max
Output Voltage Error	V _{OUT}	– 1	16	16				± mV max
		– 2	4	16		4		
Gain Adjustment	V _{ADJ}	– 1, 2	+ 655 – 245	+ 655 – 245				mV min
Line Regulation	VR _{LINE}	– 1, 2	250	250	250		10.8V ≤ V _{IN} ≤ 36V	± μV/V max
Load Regulation, Sourcing	VR _{LOAD}	– 1, 2	100	100	100		I _L = 0mA to 8.192mA	± μV/mA max
Load Regulation, Sinking	I _{OUT}	– 1, 2	100	100	100		I _L = – 8.192mA to 0mA	± μV/mA max
Output Voltage Temperature Coefficient	DV _{OUT} /dT	– 1 – 2	20 10		20 10			± ppm/°C max
Output Short-Circuit Current	I _{SC}	– 1, 2	50	50			To Ground, to V _{IN}	+ mA max

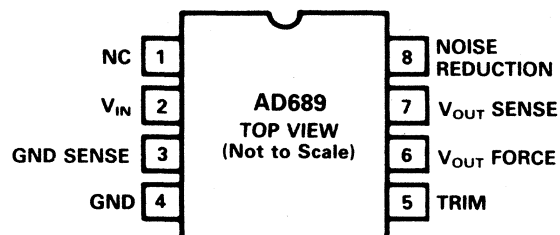
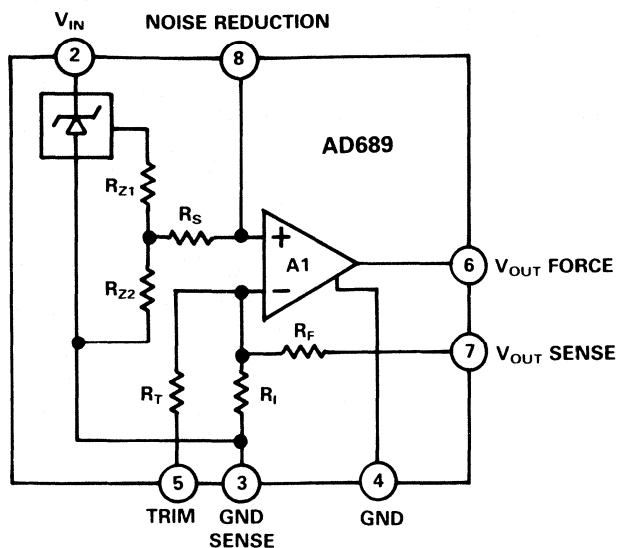
NOTE

¹V_{IN} = +12V, no load unless otherwise indicated.

Table 1.

PRELIMINARY
TECHNICAL
DATA

3.2.1 Functional Block Diagram and Terminal Assignments.

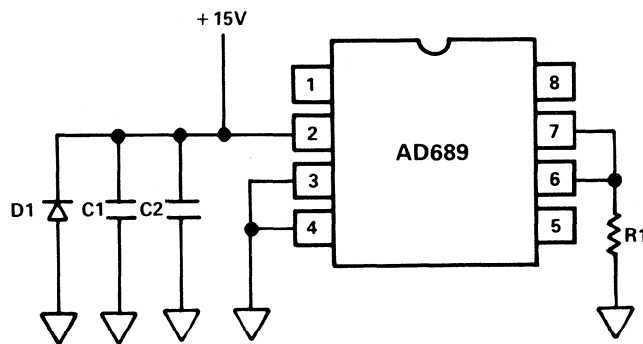


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE: D1 = MR-820
C1 = 0.1 μ F
C2 = 47 μ F
R1 = 787 Ω 1/4 WATT AT 25°C

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1.1 Scope.

This specification covers the detail requirements for a precision, low input current, low offset voltage, monolithic bipolar amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD705T/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

Q Q-8 8-Pin Cerdip Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	650 mW
Input Voltage	$\pm V_S$
Differential Input Voltage ²	$\pm 0.7\text{ V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60 sec)	$+300^\circ\text{C}$

NOTES

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8	75°C	$6.7\text{ mW}/^\circ\text{C}$

²The Input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds $\pm 0.7\text{ V}$, external series protection resistors should be added to limit the input current to less than 25 mA.

1.5 Thermal Characteristics.

Thermal Resistance: $\theta_{JC} = 22^\circ\text{C}/\text{W}$ for Q-8
 $\theta_{JA} = 110^\circ\text{C}/\text{W}$ for Q-8

AD705 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	–1	25	90	60	25		±μV
Input Offset Voltage Drift	TCV _{OS}	–1	0.6		0.6			±μV/°C
Power Supply Rejection Ratio	PSRR	–1	114	114	108		±2 V ≤ V _S ≤ ±18 V ±2.5 V ≤ V _S ≤ ±18 V	±dB
Input Bias Current ³	I _B	–1	100 150	150 200	250 450	100 150	Either Input, V _{CM} = 0 V Either Input, V _{CM} = ±13.5 V	±pA
Input Offset Current	I _{OS}	–1	100 150	150 200	250 450	100 150	V _{CM} = 0 V V _{CM} = ±13.5 V	±pA
Unity Gain Crossover Frequency	F _U	–1	0.4					MHz
Slew Rate	I _{SR}	–1	0.1					V/μs
Common Mode Rejection Ratio	CMRR	–1	114	114	108		V _{CM} = ±13.5 V	dB
Open Loop Gain	A _{OL}	–1	400 300	400 300	300 200		V _O = ±12 V, R _L = 10 kΩ V _O = ±10 V, R _L = 2 kΩ	V/mV
Output Voltage Swing	V _{OUT}	–1	±13	±13	±13		R _L = 10 kΩ	V
Power Supply Quiescent Current	I _Q	–1	600	600	800			μA
Input Noise Voltage	e _N	–1	1				0.1 to 10 Hz, p-p max	μV

NOTES

¹V_S = ±15 V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

³Bias current specifications guaranteed maximum at either input.

Table 1.

TOP VIEW

AD705

Pin 1: OFFSET NULL

Pin 2: -IN

Pin 3: +IN

Pin 4: V-

Pin 5: OVER COMP

Pin 6: OUTPUT

Pin 7: V+

Pin 8: OFFSET NULL



This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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1.1 Scope.

This specification covers the detail requirements for a linear bipolar monolithic low drift, low offset voltage operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD707S(X)/883B
–2	AD707T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip
H	H-08A	8-Pin TO-99 Metal Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm V_S$
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	
AD707T, AD707S	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Cerdip (Q)	75°C	$6.7\text{mW}/^\circ\text{C}$
TO-99 (H)	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$ for H-08A
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$ for H-08A
 $\theta_{JC} = 22^\circ\text{C}/\text{W}$ for Q-8A
 $\theta_{JA} = 110^\circ\text{C}/\text{W}$ for Q-8A

AD707 – SPECIFICATIONS

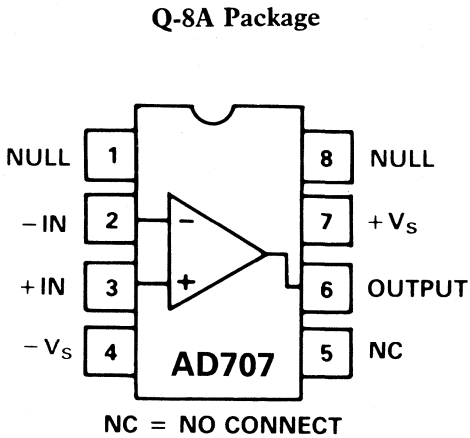
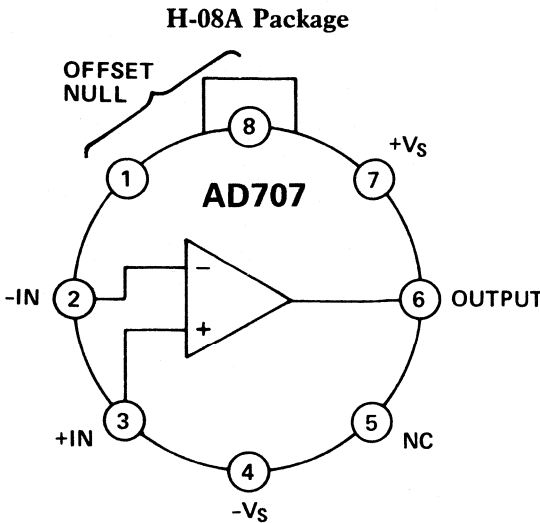
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A_{VS}	- 1	5000	5000	5000		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV min
			5000	5000			$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	
		- 2	8000	8000	8000		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	
			8000	8000			$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	
Output Voltage Swing	V_{OP}	- 1, 2	13.5	13.5			$R_L \geq 10k\Omega$	$\pm V$ min
			12.5	12.5	12.0		$R_L = 2k\Omega$	
			12.0	12.0			$R_L = 1k\Omega$	
Input Offset Voltage	V_{IO}	- 1	25	75	45	25		$\pm \mu V$ max
		- 2	15		25	15		
Input Offset Drift	$\Delta V_{IO}/\Delta T$	- 1	0.3		0.3			$\pm \mu V/^\circ C$ max
		- 2	0.1		0.1			
Input Offset Current	I_{IO}	- 1	1.5	1.5	2.0			$\pm nA$ max
		- 2	1.0	1.0	1.5			
Input Bias Current	I_{IB}	- 1	1.5	1.5	3.0			$\pm nA$ max
		- 2	1.0	1.0	2.0			
Input Offset Current Drift	dI_{IB}/dT	- 1	35					$\pm pA/^\circ C$ max
		- 2	25					
Input Bias Current Drift	dI_{IB}/dT	- 1	35					$\pm pA/^\circ C$ max
		- 2	25					
Input Resistance Differential	R_{DIFF}	- 1	45					M Ω min
		- 2	60					
Common-Mode Rejection Ratio	CMRR	- 1, 2	130	130	130		$V_{CM} = \pm CMVR$	dB min
Common-Mode Voltage Range	CMVR	- 1, 2	13	13	13			$\pm V$ min
Input Noise Voltage	e_n	- 1/2	0.6/0.35				0.1Hz to 10Hz	μV pk-pk max
Input Noise Voltage Density	e_n	- 1/2	14/13				$f_o = 10Hz$	nV/ $\sqrt{Hz}$ max
			12/11				$f_o = 100Hz$	
			11/11				$f_o = 1kHz$	
Input Current Noise	I_{NPP}	- 1, 2	30				0.1Hz to 10Hz	pA pk-pk max
Power Supply Current	I_Q	- 1, 2	3	3				mA max
Power Consumption	P_D	- 1, 2	90	90			No Load	mW max
Power Supply Rejection Ratio	PSRR	- 1	115	115	115		$\pm 3 \leq V_S \leq \pm 18$	dB min
		- 2	120	120	120			

NOTE

¹ $T_A = +25^\circ C$, $V_S = \pm 15$, unless otherwise noted.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

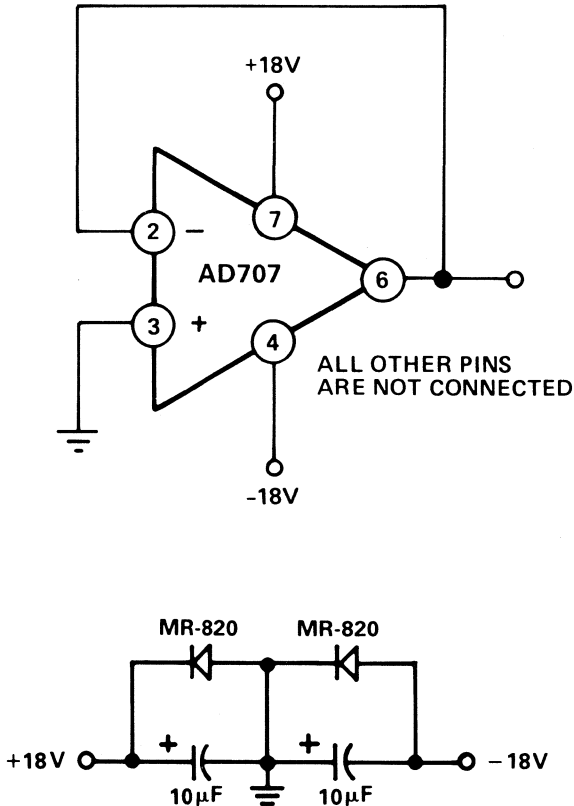


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a linear bipolar monolithic dual low drift, low offset voltage operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD708S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	 $\pm 22\text{ V}$
Internal Power Dissipation ¹	 500 mW
Differential Input Voltage	 $\pm V_S$
Input Voltage	 $\pm V_S$
Output Short Circuit Duration	 Indefinite
Storage Temperature Range	 -65°C to $+150^\circ\text{C}$
Operating Temperature Range	
AD708S	 -55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	 $+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT	DERATE ABOVE MAXIMUM
Package Type	Temperature for Rating	Ambient Temperature
Cerdip (Q)	75°C	6.7 mW/°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$ for Q-8
 $\theta_{JA} = 110^\circ\text{C/W}$ for Q-8

AD708 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A_{VS}	–1	4000	4000	4000		$R_L \geq 2 \text{ k}\Omega$, $V_{OUT} = \pm 10 \text{ V}$	V/mV min
Output Voltage Swing	V_{OP}	–1	13.5	13.5			$R_L = \geq 10 \text{ k}\Omega$	$\pm \text{V min}$
			12.5	12.5	12.0		$R_L = 2 \text{ k}\Omega$	$\pm \text{V min}$
			12.0	12.0			$R_L = 1 \text{ k}\Omega$	$\pm \text{V min}$
Input Offset Voltage	V_{IO}	–1	30		50	30		$\pm \mu\text{V max}$
Input Offset Drift	$\Delta V_{IO}/\Delta T$	–1	0.3			0.3		$\pm \mu\text{V}/^\circ\text{C max}$
Input Offset Voltage Match ²	V_{OSM}	–1	30		50	30		$\pm \mu\text{V max}$
Input Offset Voltage Drift Match ²	TCV_{OSM}	–1	0.3			0.3		$\pm \mu\text{V}/^\circ\text{C max}$
Input Offset Current	I_{IO}	–1	1.0	1.0	1.5			$\pm \text{nA max}$
Input Bias Current	I_{IB}	–1	1.0	1.0	4.0			$\pm \text{nA max}$
Input Offset Current Drift	dI_{IB}/dT	–1	25					$\pm \text{pA}/^\circ\text{C max}$
Input Bias Current Drift	dI_{IB}/dT	–1	30					$\pm \text{pA}/^\circ\text{C max}$
Input Bias Current Match ²	I_{IBM}	–1	1.0	1.0	2.0			$\pm \text{nA max}$
Common-Mode Rejection Ratio	CMRR	–1	130		130	130	$V_{CM} = \pm 13 \text{ V}$	dB min
Power Supply Rejection Ratio	PSRR	–1	120		120	120	$\pm 3 \leq V_S \leq \pm 18$	dB min
Common-Mode Rejection Ratio Match ²	CMRR _M	–1	130		130	130	$V_{CM} = \pm 13 \text{ V}$	dB min
Power Supply Rejection Ratio Match ²	PSRR _M	–1	120		120	120	$\pm 3 \text{ V} \leq V_S \leq 18 \text{ V}$	dB min
Input Noise Voltage	e_n	–1	0.35				0.1 Hz to 10 Hz	$\mu\text{V pk-pk max}$
Input Noise Voltage Density	e_n	–1	12				$f_O = 10 \text{ Hz}$	$\text{nV}/\sqrt{\text{Hz max}}$
			11				$f_O = 100 \text{ Hz}$	
			11				$f_O = 1 \text{ kHz}$	
Input Current Noise	I_{NPP}	–1	35				0.1 Hz to 10 Hz	pA pk-pk max
Power Supply Current	I_Q	–1	5.5	5.5				mA max
Power Consumption	P_D	–1	165	165			No Load	mW max
Channel Separation	CS	–1	140					dB min

NOTES

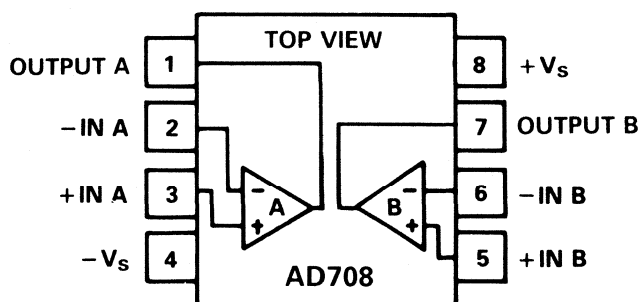
¹ $T_A = +25^\circ\text{C}$, $V_S = \pm 15 \text{ V}$, unless otherwise noted.

²Matching is defined as the difference between parameters of the two amplifiers.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Plastic (N)
and Cerdip (Q)
Package

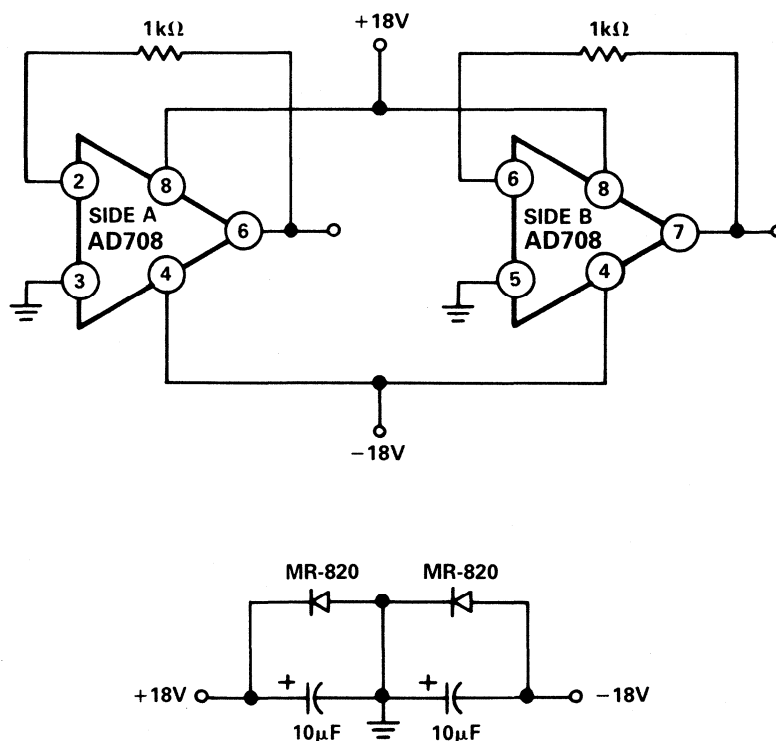


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD711S(X)/883B
- 2	AD711T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip Package
H	H-08B	8-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Input Voltage	$\pm 18\text{V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8A	75°C	6.7mW/°C
H-08B	80°C	7.1mW/°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C/W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C/W}$ for Q-8A
θ_{JC}	$= 65^\circ\text{C/W}$ for H-08B
θ_{JA}	$= 150^\circ\text{C/W}$ for H-08B

AD711 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	-1 -2	1.0 0.5	1.0 0.5	2.0 1.0		± mV max
Input Offset Voltage Drift	TCV _{OS}	-1 -2	20 10		20 10		± μV/°C max
Power Supply Rejection Ratio	PSRR	-1 -2	76 80	76 80	76 80		dB min
Input Bias Current ³	I _B	-1, 2 -1, 2	50 100	50 100		Either Input, V _{CM} = 0 Either Input, V _{CM} = +10V	± pA max
Input Offset Current ³	I _{OS}	-1, 2	25	25		V _{CM} = 0	± pA max
Gain Bandwidth Product	GBW	-1 -2	3.0 3.4				MHz min
Slew Rate	t _{SR}	-1 -2	16 18	16 18		Unity Gain Unity Gain	V/μs min
Common-Mode Voltage Range	CMVR	-1, 2	-V _S + 4V +V _S - 2V				V
Common-Mode Rejection Ratio	CMRR	-1 -2 -1 -2	76 80 70 76	76 80 70 76	76 80 70 74	V _{CM} = ±10V V _{CM} = ±10V V _{CM} = ±11V V _{CM} = ±11V	dB min dB min
Open Loop Gain	A _{OL}	-1 -2	150 200	150 200	100 100	V _O = ±10V, R _L ≥ 2kΩ V _O = ±10V, R _L ≥ 2kΩ	V/mV min
Output Voltage Swing	V _{OUT}	-1, 2	+13/-12.5	+13/-12.5	±12	R _L ≥ 2kΩ	± V min
Power Supply Current	I _Q	-1 -2	3.4 3.0	3.4 3.0			mA max

NOTES

¹T_A = +25°C, V_S = ±15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

Nulling will induce an additional ±3μV/°C.

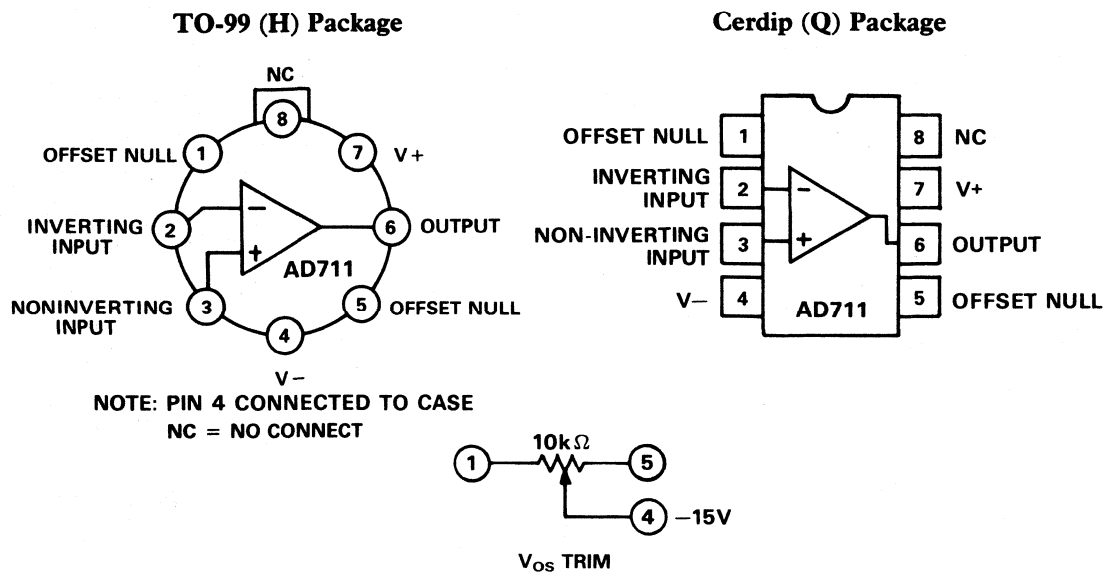
³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

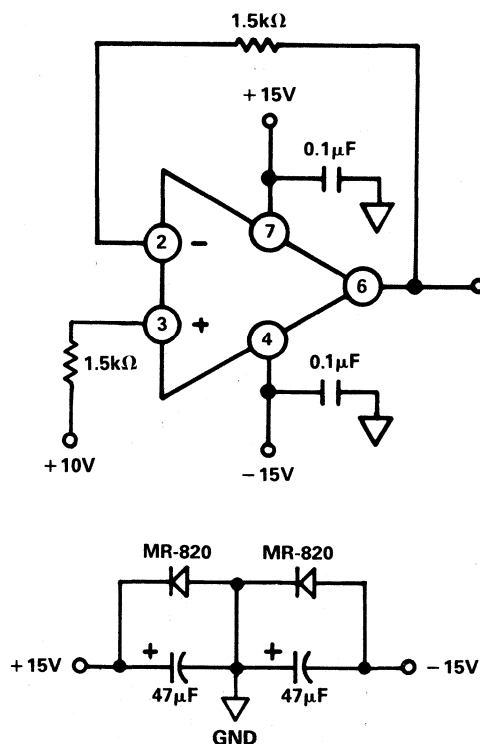


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD712S(X)/883B
- 2	AD712T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip Package
H	H-08B	8-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Input Voltage	$\pm 18\text{V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8A	75°C	$6.7\text{mW}/^\circ\text{C}$
H-08B	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8A
θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08B
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08B

AD712 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	-1 -2	1.0 0.7	1.0 0.7	2.0 1.5		± mV max
Input Offset Voltage Drift	TCV _{OS}	-1 -2	20 10		20 10		± μV/°C max
Power Supply Rejection Ratio	PSRR	-1 -2	76 80	76 80	76 80		dB min
Input Bias Current ³	I _B	-1, 2 -1, 2	75 100	75 100		Either Input, V _{CM} = 0 Either Input, V _{CM} = +10V	± pA max
Input Offset Current ³	I _{OS}	-1, 2	25	25		V _{CM} = 0	± pA max
Gain Bandwidth Product	GBW	-1 -2	3.0 3.4				MHz min
Slew Rate	t _{SR}	-1 -2	16 18	16 18		Unity Gain Unity Gain	V/μs min
Common-Mode Voltage Range	CMVR	-1, 2	-V _S + 4V +V _S - 2V				V
Common-Mode Rejection Ratio	CMRR	-1 -2 -1 -2	76 80 70 76	76 80 70 76	76 80 70 74	V _{CM} = ±10V V _{CM} = ±10V V _{CM} = ±11V V _{CM} = ±11V	dB min dB min
Open Loop Gain	A _{OL}	-1 -2	150 200	150 200	100 100	V _O = ±10V, R _L ≥ 2kΩ V _O = ±10V, R _L ≥ 2kΩ	V/mV min
Output Voltage Swing	V _{OUT}	-1, 2	+13/-12.5	+13/-12.5	±12	R _L ≥ 2kΩ	± V min
Power Supply Current	I _Q	-1 -2	6.8 6.0	6.8 6.0			mA max
Input Offset Voltage Match ⁴	V _{OSM}	-1 -2	1.0 0.7	1.0 0.7	2.0 1.5		± mV max
Input Offset Voltage Drift Match ⁴	TCV _{OSM}	-1 -2	20 10		20 10		± μV/°C max
Input Bias Current Match ⁴	I _{BM}	-1, 2	25	25			± pA max

NOTES

¹T_A = +25°C, V_S = ±15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C. Nulling will induce an additional ±3μV/°C.

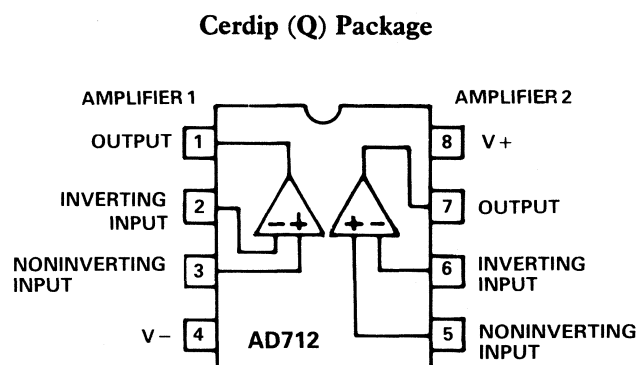
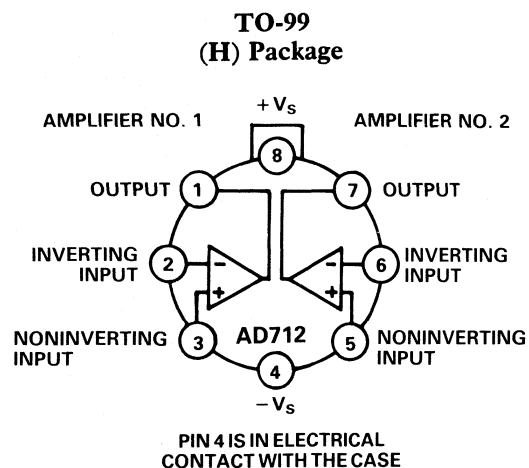
³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C. For temperatures above +25°C, the current doubles every 10°C.

⁴Matching is defined as the difference between parameters of the two amplifiers.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

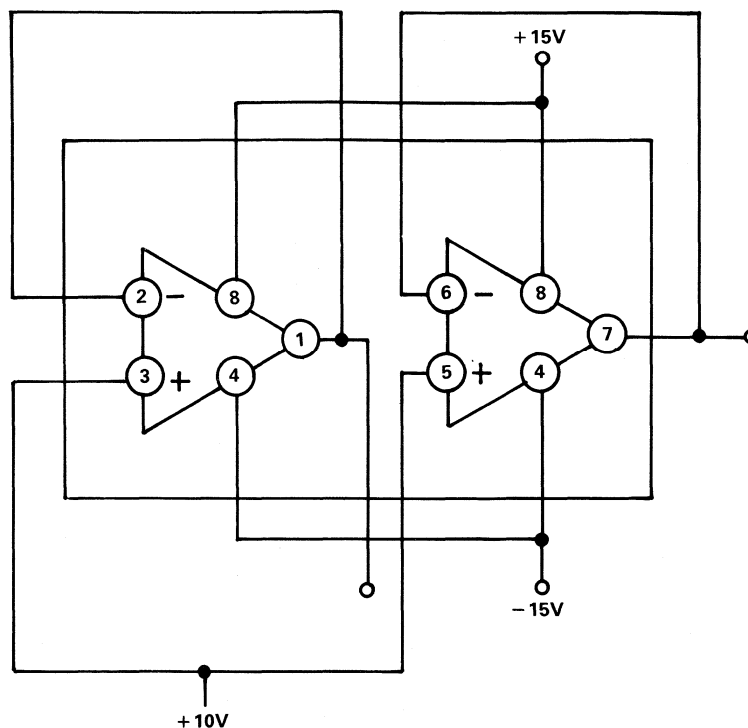


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirement for a precision monolithic laser-trimmed quad BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD713S(Q)/883B
-2	AD713T(Q)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

Q Q-14 14-Pin Cerdip Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation	500 mW
Input Voltage	$\pm 18\text{ V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$ for Q-14
 $\theta_{JA} = 110^\circ\text{C/W}$ for Q-14

AD713 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	-1 -2	1.5 0.5	1.5 0.5	2.0 1.0		±mV max
Input Offset Voltage Drift	TCV _{OS}	-2	15				±µV/°C
Power Supply Rejection Ratio	PSRR	-1 -2	78 84	78 84	76 84		dB min
Input Bias Current ³	I _B	-1 -2	150 75	150 75		Either Input, V _{CM} = 0	±pA max
		-1 -2	200 120	200 120		Either Input, V _{CM} = +10 V	
Input Offset Current ³	I _{OS}	-1 -2	75 35	75 35		V _{CM} = 0	±pA max
Gain Bandwidth Product	GBW	-1 -2	3.0 3.4				MHz min
Slew Rate	t _{SR}	-1 -2	16 18	16 18		Unity Gain Inverter	V/µs min
Common-Mode Voltage Range	CMVR	-1, 2	-V _S +4V +V _S -2V				V
Common-Mode Rejection Ratio	CMRR	-1 -2	78 84	78 84	76 82	V _{CM} = ±10 V V _{CM} = ±10 V	dB min
		-1 -2	72 78	72 78	70 74	V _{CM} = ±11 V V _{CM} = ±11 V	
Open Loop Gain	A _{OL}	-1	150	150	100	V _O = ±10 V, R _L ≥ 2 kΩ	V/mV min
		-2	200	200	100	V _O = ±10 V, R _L ≥ 2 kΩ	
Output Voltage Swing	V _{OUT}	-1, 2	+13/-12.5	+13/-12.5	±12	R _L ≥ 2kΩ	V min
Power Supply Current	I _Q	-1 -2	13.5 12.0	13.5 12.0			mA max
Input Offset Voltage Match ⁴	V _{OSM}	-1 -2	1.8 0.8	1.8 0.8	2.3 1.3		±mV max
Input Offset Voltage Drift Match ⁴	TCV _{OSM}	-2	25				±µV/°C max
Input Bias Current Match ⁴	I _{BM}	-1	100	100			±pA max
		-2	35	35			

NOTES

¹T_A = +25°C, V_S = ±15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

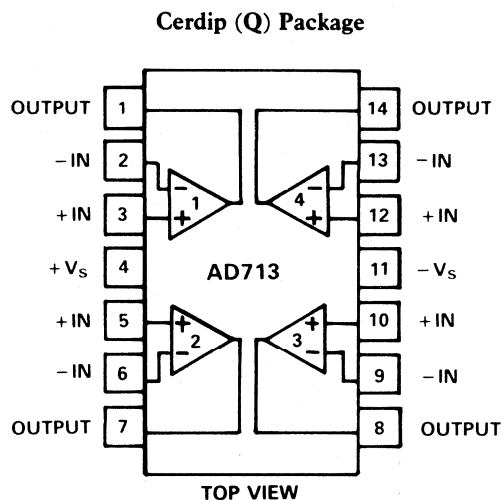
³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C.

For temperatures above +25°C, the current doubles every 10°C.

⁴Matching is defined as the difference between parameters of the two amplifiers.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

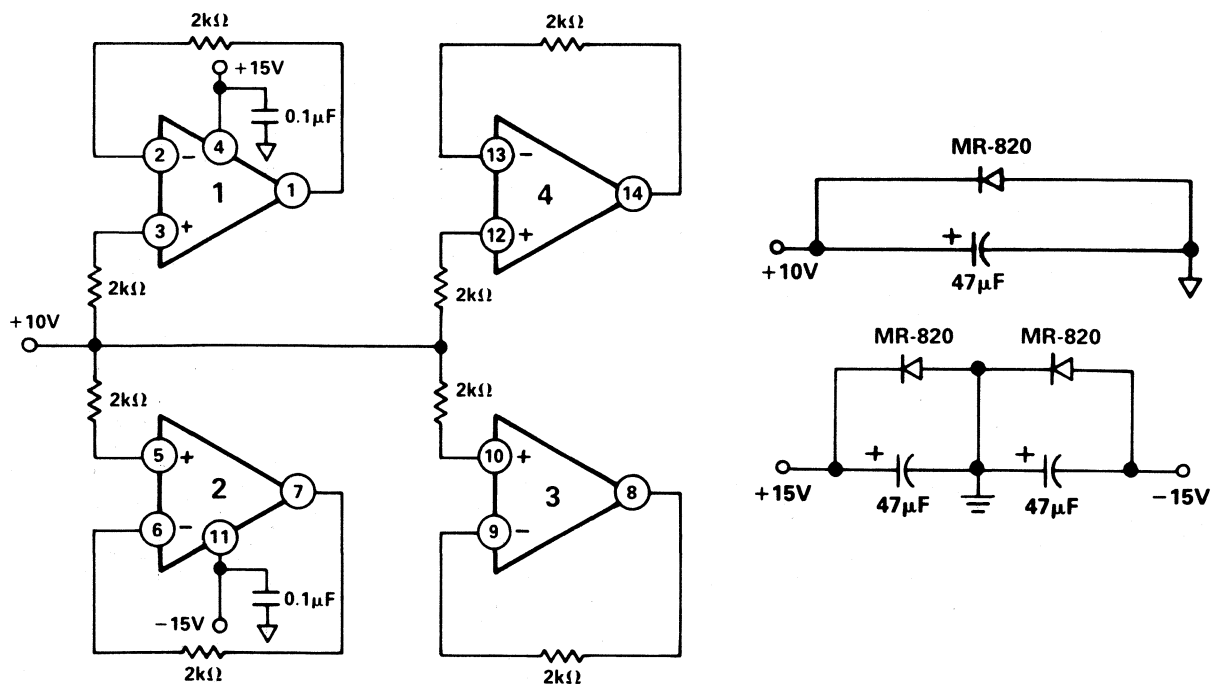


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a general purpose bipolar operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD741SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-08A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise stated)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	$\pm 15\text{V}$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

NOTES

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 65^\circ\text{C}/\text{W}$
 $\theta_{JA} = 150^\circ\text{C}/\text{W}$

AD741 – SPECIFICATIONS

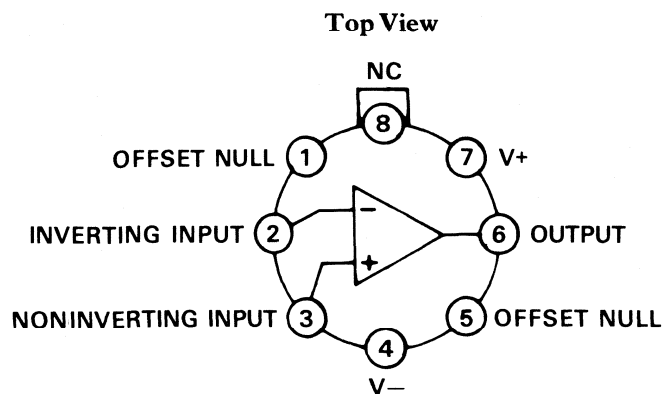
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{VS}	– 1	50	50	25		V _{OUT} = ± 10V R _L = 2kΩ	V/mVmin
Slew Rate	SR	– 1	0.4					± V/μs min
Output Voltage Swing	V _{OUT}	– 1	10	10			R _L = 2kΩ min	± V min
Input Offset Voltage	V _{IO}	– 1	2.0	2.0	4.0			± mV min
Input Offset Voltage Drift		– 1	15		15			μV/°C
Input Offset Current	I _{IO}	– 1	10	10	25			± nA max
Input Bias Current	I _{IB}	– 1	75	75	250			± nA max
Output Short Circuit Current	I _{SC}	– 1	25					mA
Differential Input Voltage	V _{DIFF}	– 1	25					± V max
Common-Mode Voltage Range	CMVR	– 1	12					± V min
Common-Mode Rejection Ratio	CMRR	– 1	90	90	90		V _{IN} = ± 10V	dB
Power Supply Current	I _O	– 1	2.8	2.8				mA max
Rejection Ratio	PSRR	– 1	100	100	100			± μV/V max

NOTE

¹T_A = +25°C, V_S = ± 15V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

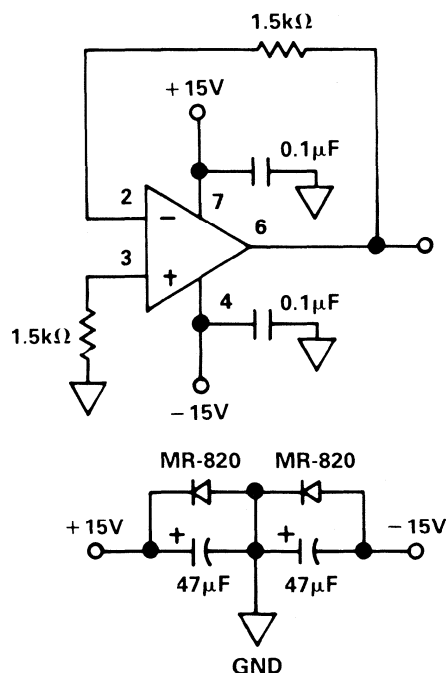


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD744S(X)/883B
– 2	AD744T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8	8-Pin Cerdip Package
H	H-08B	8-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Input Voltage	$\pm 18\text{V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8	75°C	$6.7\text{mW}/^\circ\text{C}$
H-08B	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8
θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08B
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08B

AD744 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	– 1 – 2	1.0 0.5	1.0 0.5	2.0 1.0		± mV max
Input Offset Voltage Drift	TCV _{OS}	– 1 – 2	20 10		20 10		± μV/°C max
Power Supply Rejection Ratio	PSRR	– 1 – 2	82 88	82 88	82 88		dB min
Input Bias Current ³	I _B	– 1, 2 – 1 – 2	100 150 150	100 150 150		Either Input, V _{CM} = 0 Either Input, V _{CM} = + 10V Either Input, V _{CM} = + 10V	± pA max
Input Offset Current ³	I _{OS}	– 1, 2	50	50		V _{CM} = 0	± pA max
Gain Bandwidth Product	GBW	– 1 – 2	8 9				MHz min
Slew Rate	t _{SR}	– 1 – 2	45 50	45 50		Gain = – 1 Gain = – 1	V/μs min
Common-Mode Rejection Ratio	CMRR	– 1	78	78	76	V _{CM} = ± 10V	dB min
		– 2	82	82	80	V _{CM} = ± 10V	
		– 1	72	72	70	V _{CM} = ± 11V	dB min
		– 2	78	78	74	V _{CM} = ± 11V	
Open Loop Gain	A _{OL}	– 1 – 2	200 250	200 250	100 100	V _O = ± 10V, R _L ≥ 2kΩ V _O = ± 10V, R _L ≥ 2kΩ	V/mV min
Output Voltage Swing	V _{OUT}	– 1, 2	+ 13/– 12.5	+ 13/– 12.5	± 12	R _L ≥ 2kΩ	± V min
Power Supply Current	I _Q	– 1 – 2	5.0 4.0	5.0 4.0			mA max

NOTES

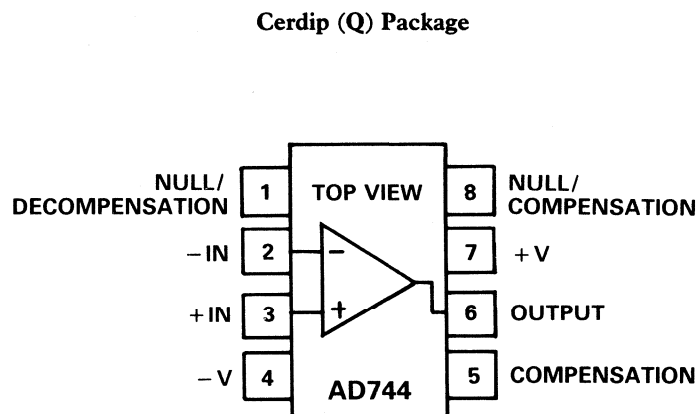
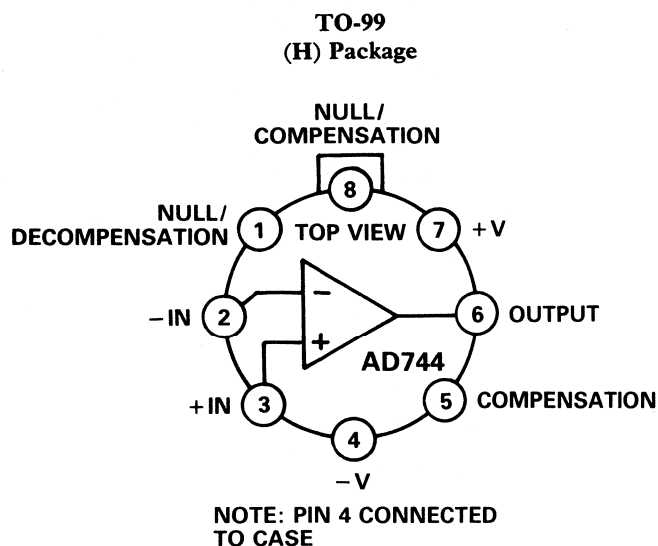
¹T_A = + 25°C, V_S = ± 15V unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = + 25°C. Nulling will induce an additional ± 3μV/°C/mV.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = + 25°C. For temperatures above + 25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

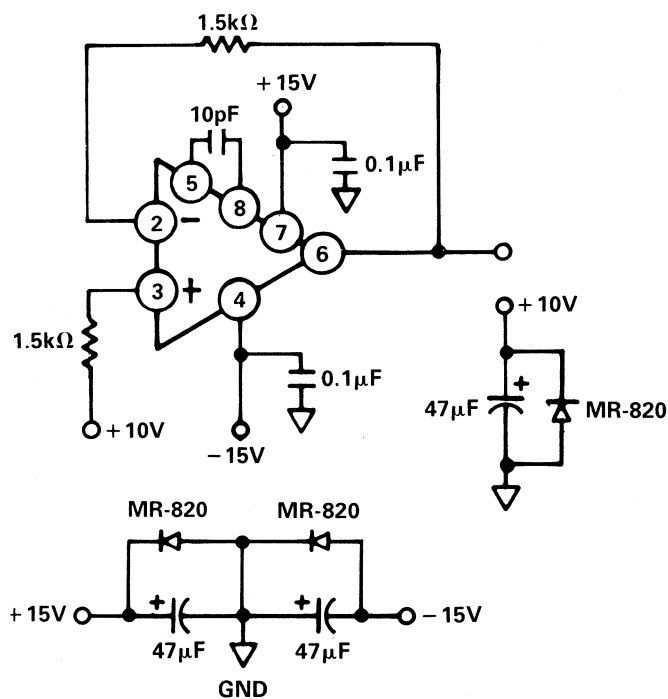


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Precision 500 ns Settling Dual BiFET Op Amp

AD746

1.1 Scope.

This specification covers the detail requirements for a precision, monolithic, laser-trimmed BiFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD746S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

Q	Q-8	8-Pin Cerdip Package
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1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	500 mW
Input Voltage	$\pm 18\text{ V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8	75°C	$6.7\text{ mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C}/\text{W}$ for Q-8
 $\theta_{JA} = 110^\circ\text{C}/\text{W}$ for Q-8

AD746 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	–1	1.0	1.0	2.0		±mV max
Input Offset Voltage Drift	TCV _{OS}	–1	20		20		±μV/°C max
Power Supply Rejection Ratio	PSRR	–1	80	80	80		dB min
Input Bias Current ³	I _B	–1	250	250		Either Input, V _{CM} = 0	±pA max
		–1	350	350		Either Input, V _{CM} = +10 V	
Input Offset Current ³	I _{OS}	–1	125	125		V _{CM} = 0	±pA max
Gain Bandwidth Product	GBW	–1	8				MHz min
Slew Rate	t _{SR}	–1	45	45		A _{VCL} = –1	V/μs min
Common Mode Rejection Ratio	CMRR	–1	78	78	76	V _{CM} = ±10 V	dB min
		–1	72	72	70	V _{CM} = ±11 V	dB min
Open Loop Gain	A _{OL}	–1	150	150	65	V _O = ±10 V, R _L ≥ 2 kΩ	V/mV min
Output Voltage Swing	V _{OUT}	–1	+13/–12.5	+13/–12.5	±12	R _L ≥ 2 kΩ	±V min
Power Supply Current	I _Q	–1	10	10			mA max

NOTES

¹T_A = +25°C and V_S = ±15 V, unless otherwise noted.

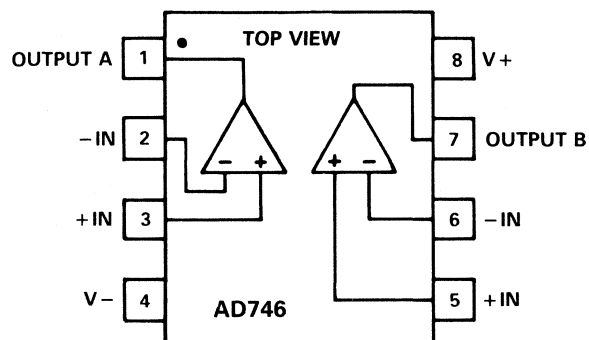
²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C. Nulling will induce an additional +3 μV/°C/mV.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = 25°C. For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Cerdip (Q) Package

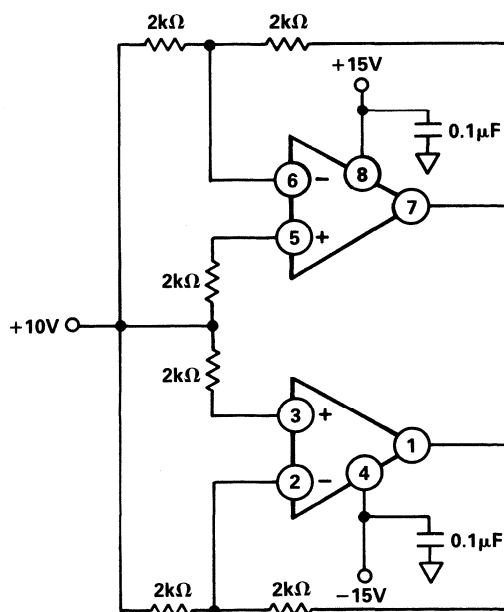


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Microprocessor-Compatible 12-Bit D/A Converter

AD767

1.1 Scope.

This specification covers the detail requirements for a complete 12-bit digital-to-analog converter with microprocessor interface, buried Zener reference and output amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
—1	AD767SD/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Power Ground	0V to +18V
V_{EE} to Power Ground	0V to -18V
Digital Inputs (Pins 11, 13-24) to Power Ground	-1.0V to +7.0V
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Ref Out, V_{OUT} (Pins 6, 9)	Indefinite Short to Power Ground Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
$\theta_{JA} = 80^\circ\text{C/W}$

AD767 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1	1	1	All Bits With Positive Errors On. All Bits with Negative Errors On	± LSB max
Differential Nonlinearity	DNL	– 1	1	1	1	Major Carry Errors	± LSB max
Gain Error ²	A _E	– 1	0.20	0.20		All Bits On	± % FSR max
Gain Temperature Coefficient	TCA _E	– 1	30		30	All Bits On	± ppm/°C max
Unipolar Offset Error	V _{OS}	– 1	2	2		All Bits Off	± LSB max
Temperature Coefficient Unipolar Offset	TCV _{OS}	– 1	3		3	All Bits Off	± ppm/°C max
Bipolar Zero Error ²	B _{PZE}	– 1	0.10	0.10		MSB On, All Other Bits Off Bipolar Mode	± % FSR max
B/P Zero Temperature Coefficient	TCB _{PZE}	– 1	10		10	MSB On, All Other Bits Off Bipolar Mode	± ppm/°C max
Input Resistance	R _{IN}	– 1	15				kΩ min
			25				kΩ max
Reference Output Voltage	V _{REF}	– 1	9.9	9.9	9.9	Unipolar Mode 1.1mA External Load	+ V min
			10.10	10.10	10.10		+ V max
Output Current	I _{OUT}	– 1	5				± mA min
Output Short-Circuit Current	I _{SC}	– 1	40				+ mA max
Power Supply Rejection Ratio	PSRR	– 1	10	10		All Bits On + 11.4V ≤ V _{CC} ≤ + 16.5V	± ppm of FSR/% max
			10	10		All Bits On – 11.4V ≤ V _{EE} ≤ – 16.5V	
Power Supply Current	I _{CC}	– 1	13	13		V _{CC} = + 16.5V, V _{EE} = – 16.5V I _{CC} : All Bits On	+ mA max
	I _{EE}	– 1	23	23		I _{EE} : All Bits Off	– mA max
Digital Input High Voltage	V _{IH}	– 1	2.0	2.0	2.0		+ V min
			5.5				+ V max
Digital Input Low Voltage	V _{IL}	– 1	0.8	0.8	0.7		+ V max
Digital Input High Current	I _{IH}	– 1	10	10		V _{IH} = 5.5V	+ μA max
Digital Input Low Current	I _{IL}	– 1	5	5		V _{IL} = 0.0V	+ μA max
Data Setup Time ³	t _{DC}	– 1	90				ns min
Data Hold Time ³	t _{DH}	– 1	20				ns min
CS Pulse Width ³	t _{CP}	– 1	90				ns min
Output Voltage Settling Time ³	t _{SL}	– 1	4			R _{FB} = 10k R _L = 2k 500pF	μs max
			3			R _{FB} = 5k	

NOTES

¹V_{CC} = + 15V, V_{EE} = – 15V, 50Ω resistor Pin 6 to Pin 7, CS = LOGIC “0”, V_{IH} = 2.0V, V_{IL} = 0.8V, Unipolar configuration unless otherwise specified.

Unipolar Configuration – Pins 1 and 2 to Pin 9, Pin 4 to Pin 5.

Bipolar Configuration – Pin 1 to Pin 9, 50Ω resistor Pin 4 to Pin 6.

²Adjustable to 0V.

³See Figure 1.

Table 1.

REV. B

AD767

Timing Specifications.

$V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$.

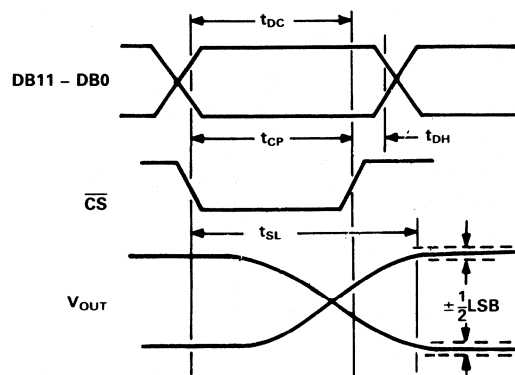


Figure 1.



High Speed, Precision Comparator with Latch Circuit

AD790

1.1 Scope.

This specification covers the detail requirements for a high speed, low power, precision comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD790SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Logic Supply Voltage	$+7\text{ V}$
Internal Power Dissipation	500 mW
Differential Input Voltage	$\pm 16.5\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 60 sec)	$+300^\circ\text{C}$

Note

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The voltage at any pin should never exceed supply voltages.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C/W}$
θ_{JA}	$= 100^\circ\text{C/W}$

AD790 – SPECIFICATIONS

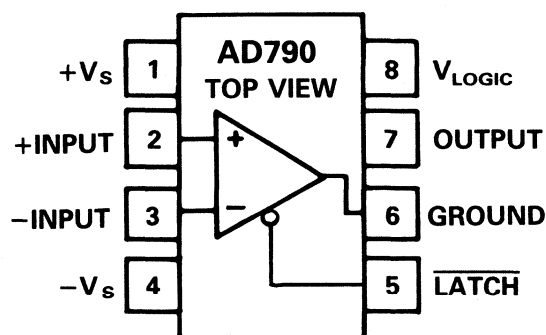
Test	Symbol	Device	Design Limit @ 25°C	Sub Group 1	Sub Group 2, 3	V _S	Test Condition ¹	Units
Response Time	t _{PD}	–1	45			±15 V		ns max
Response Time	t _{PD}	–1	50			+5 V		ns max
Input Offset Voltage	V _{OS}	–1	1.0	1.0	1.5	±15 V		mV max
Input Offset Voltage	V _{OS}	–1	1.5	1.5	2.0	+5 V		mV max
Hysteresis	V _H	–1	0.65	0.65	0.65	±15 V		mV max
Hysteresis	V _H	–1	1.0	1.0	1.0	+5 V		mV max
Input Bias Current	I _B	–1	5	5	7	±15 V		μA max
Input Bias Current	I _B	–1	5	5	8	+5 V		μA max
Input Offset Current	I _{OS}	–1	0.25	0.25	0.40	±15 V		μA max
Input Offset Current	I _{OS}	–1	0.25	0.25	0.40	+5 V		μA max
Power Supply Rejection Ratio	PSRR	–1	80	80	76	±15 V	V _S ±20%	dB min
Power Supply Rejection Ratio	PSRR	–1	80	80	76	+5 V	V _S ±20%	dB min
Common Mode Rejection Ratio	CMRR	–1	80	80	76	±15 V	–10 V < V _{CM} < 10 V	dB min
Power Dissipation	P _{DISS}	–1	242	242		±15 V		mW max
Power Dissipation	P _{DISS}	–1	60	60		+5 V		mW max
Output High Voltage	V _{OH}	–1	4.3	4.3	4.3	±15 V	6.4 mA Source	V min
Output High Voltage	V _{OH}	–1	4.3	4.3	4.3	+5 V	6.4 mA Source	V min
Output Low Voltage	V _{OL}	–1	0.5	0.5	0.5	±15 V	6.4 mA Sink	V max
Output Low Voltage	V _{OL}	–1	0.5	0.5	0.5	+5 V	6.4 mA Sink	V max
Differential Input Voltage	V _{DIFF}	–1	±15			±15 V		V max
Differential Input Voltage	V _{DIFF}	–1	+5			+5 V		V max
Common Mode Input Voltage	V _{CM}	–1	+13			±15 V		V max
	V _{CM}	–1	–15			±15 V		V min
Common Mode Input Voltage	V _{CM}	–1	+3			+5 V		V max
	V _{CM}	–1	0			+5 V		V min
Quiescent Current +V _S –V _S +V _{LOGIC}	I _Q	–1				±15 V		
	I _Q	–1	10	10		±15 V		mA max
	I _Q	–1	5	5		±15 V		mA max
	I _Q	–1	3.3	3.3		+5 V		mA max
Quiescent Current in Single Supply Mode	I _Q	–1	12	12		+5 V		mA max

NOTE

¹V_{LOGIC} = +5 V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

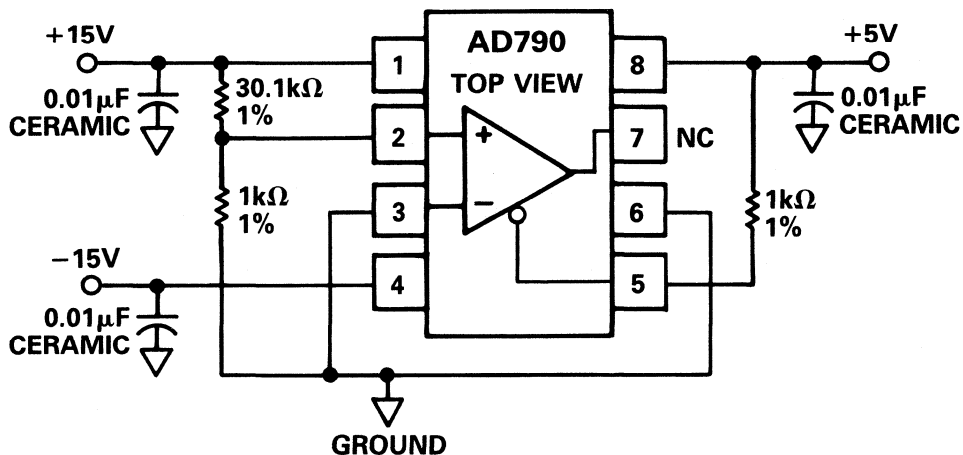


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (50).

4.2.1 Life Test/Burn-In Circuit.

Steady-state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic, four-quadrant multiplier, whose transfer function is

$$W = \frac{XY}{1 V^2} \times 4 mA$$

where:

$$X = (X_1 - X_2)$$

$$Y = (Y_1 - Y_2)$$

W = Value of output current source; see Figure. 3.2.1.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD843S(Q)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	 $\pm 9 V$
Internal Power Dissipation	 500 mW
Input Voltages (X_1, X_2, Y_1, Y_2)	 $\pm V_S$
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$
Storage Temperature Range	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	 $+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

AD834 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Total Error ² vs. Supplies ³	TE	-1 -1	2 0.3	2	3	0.3	-1 V ≤ X, Y ≤ +1 V ±V _S = ±4 V to ±6 V	±% FS ±%FS/V
Linearity ⁴	LE	-1	1	1				±%FS
Bandwidth	BW	-1	500					MHz
Feedthrough, X	FRR _X	-1	0.3	0.3			X = ±1 V; Y = nulled	±% FS
Feedthrough, Y	FRR _Y	-1	0.2	0.2			X = nulled, Y = ±1 V	±% FS
Input Offset Voltage vs. Supplies	V _{IO}	-1 -1	3 300	3	4	300	X and Y inputs ±4 V to ±6 V	±mV ±μV/V
Input Clipping Level	V _{CL}	-1	1.1				Differential	±V
Nonlinearity, X	NL _X	-1	0.5			0.5	Y = 1 V; X = ±1 V	±%FS
Nonlinearity, Y	NL _Y	-1	0.3			0.3	X = 1 V; Y = ±1 V	±% FS
Output Offset Current	I _O	-1	60	60	60		Differential; X = Y = 0	±μA
Scaling Current Error	SI	-1	0.04	0.04			From nominal of 4 mA; differential	±mA
Supply Current	+I _S -I _S	-1 -1	14 35	14 35	14 35			mA mA
Power Supply Operating Range	V _S	-1	4.0 9.0					±V min to max
Zero Signal Current	ZSC (or ZSI)	-1	8.5				Each Output	mA

NOTES

¹±V_S = ±5 V, T_A = 25°C unless otherwise specified.

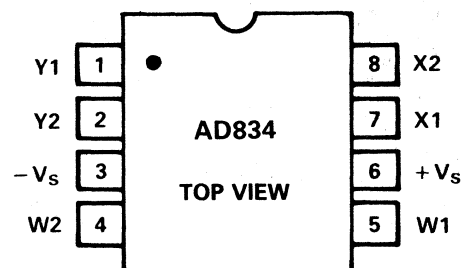
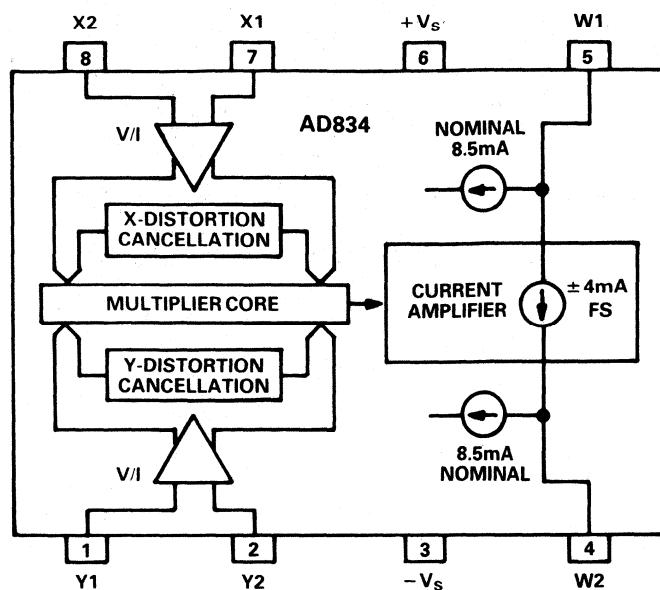
²Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full-scale output.

³Both supplies taken simultaneously; sinusoidal input at f ≤ 10kHz.

⁴Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

Table 1.

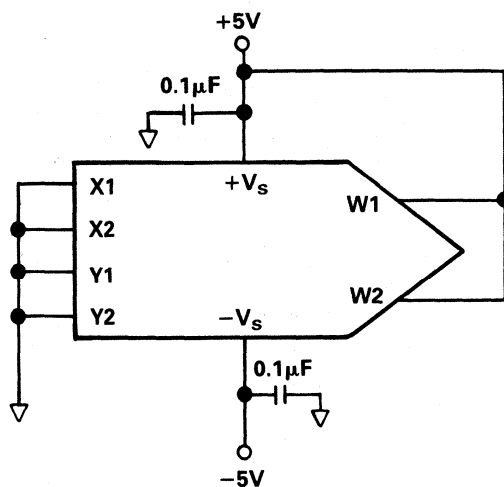
3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.



1.1 Scope.

This specification covers the detail requirements for a high speed, fast settling monolithic, operational amplifier which is stable at closed-loop gains of 10 or greater.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD840SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-14.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.3 W
Input Common-Mode Voltage, Max Safe	$\pm V_S$
Differential Input Voltage	$\pm 6\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so that T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$. Junction temperatures greater than 150°C may cause significant degradation of performance. Therefore, use of a heat sink is recommended if the device is used in high temperature or high output current applications.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 35^\circ\text{C/W}$
θ_{JA}	$= 110^\circ\text{C/W}$

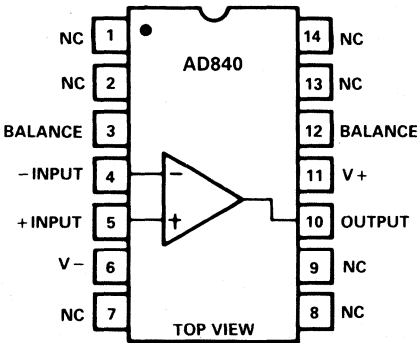
AD840 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage	V _{OS}	–1	1	1	2		±mV max
Input Bias Current	I _B	–1	8	8	12	V _{IN} = 0 V	±µA max
Input Offset Current	I _{OS}	–1	0.4	0.4	0.6		±µA max
Common-Mode Voltage Range	CMVR	–1	10	10	10		±V min
Common-Mode Rejection Ratio	CMRR	–1	90	90	85	V _{CM} = ±10 V	dB min
Open-Loop Gain	A _{OL}	–1	100	100	50	V _{OUT} = ±10 V, R _{LOAD} = 1 kΩ	V/mV min
		–1	75	75	50	V _{OUT} = ±10 V, R _{LOAD} = 500 Ω	V/µV min
Output Voltage Swing	V _{OUT}	–1	10	10	10	R _L = 500 Ω	±V min
Output Current	I _{OUT}	–1	50			V _{OUT} = ±10 V	±mA min
Slew Rate	SR	–1	350				V/µs min
Power Supply Rejection	PSRR	–1	90	90	80	V _S = ±5 V to ±18 V	dB min
Power Supply Current	I _Q	–1	12	12	16	V _{OUT} = 0	mA max

NOTE
¹V_S = ±15 V, unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

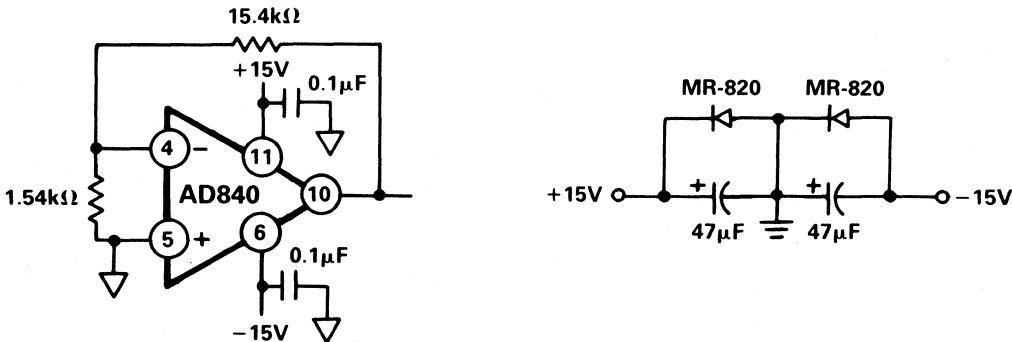


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-in Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high speed, fast settling monolithic, operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD841S(X)/883B

1.2.3 Case Outline

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-14	14-Pin Cerdip Package
H	H-12A	12-Pin TO-8 Metal Can Package
E	E-20A	20-Contact LCC Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted).

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.3 W
Input Common-Mode Voltage, Max Safe	$\pm V_S$
Differential Input Voltage	$\pm 6\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so that T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$. Junction temperatures greater than $+150^\circ\text{C}$ may cause significant degradation of performance. Therefore, use of a heat sink is recommended if the device is used in high temperature or high output current applications.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 35^\circ\text{C/W}$ for Q-14
θ_{JA}	$= 110^\circ\text{C/W}$ for Q-14
θ_{JC}	$= 30^\circ\text{C/W}$ for H-12A
θ_{JA}	$= 100^\circ\text{C/W}$ for H-12A
θ_{JC}	$= 25^\circ\text{C/W}$ for E-20A
θ_{JA}	$= 150^\circ\text{C/W}$ for E-20A

AD841 – SPECIFICATIONS

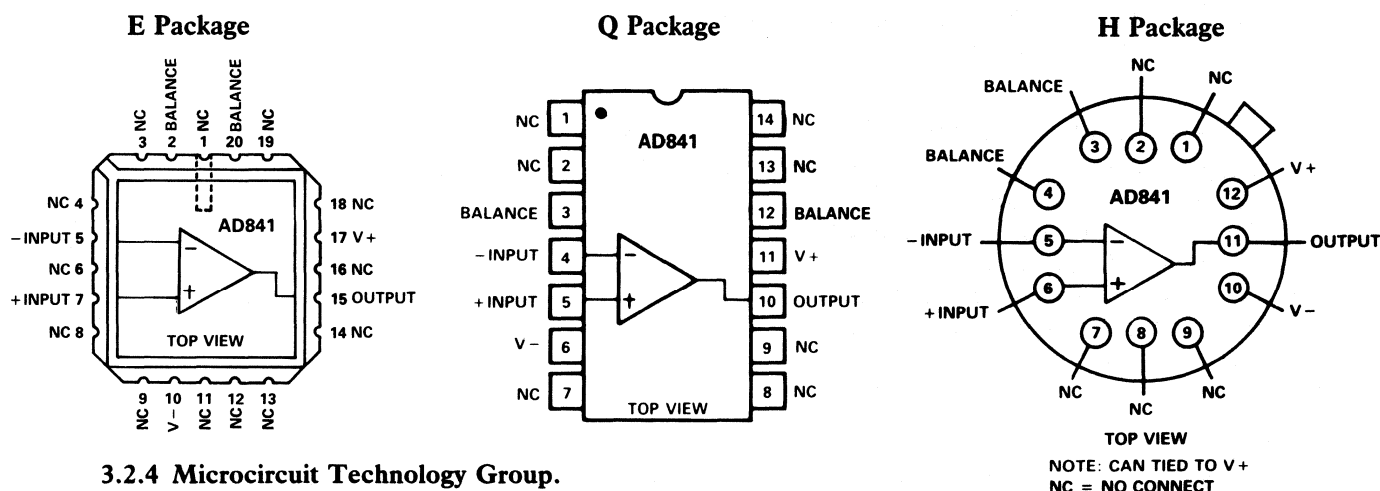
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Conditions ¹	Units
Input Offset Voltage	V_{OS}	-1	2	2	5.5		$\pm$ mV max
Input Bias Current	I_B	-1	8	8	12	$V_{IN} = 0$ V	$\pm$ μ A max
Input Offset Current	I_{OS}	-1	0.4	0.4	0.6		$\pm$ μ A max
Common-Mode Voltage Range	CMVR	-1	10	10	10		$\pm$ V min
Common-Mode Rejection Ratio	CMRR	-1	86	86	80	$V_{CM} = \pm 10$ V	dB min
Open Loop Gain	A_{OL}	-1	25	25	12	$V_{OUT} = \pm 10$ V, $R_{LOAD} = 500 \Omega$	V/mV min
Output Voltage Swing	V_{OUT}	-1	10	10	10	$R_{LOAD} = 500 \Omega$	$\pm$ V min
Output Current	I_{OUT}	-1	50	50		$V_{OUT} = \pm 10$ V	$\pm$ mA min
Slew Rate	SR	-1	200				V/ μ s min
Power Supply Rejection	PSRR	-1	86	86	80	$V_S = \pm 5$ V to ± 18 V	dB min
Power Supply Current	I_Q	-1	12	12	16	$V_{OUT} = 0$	mA max

NOTE

¹ $V_S = \pm 15$ V, unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

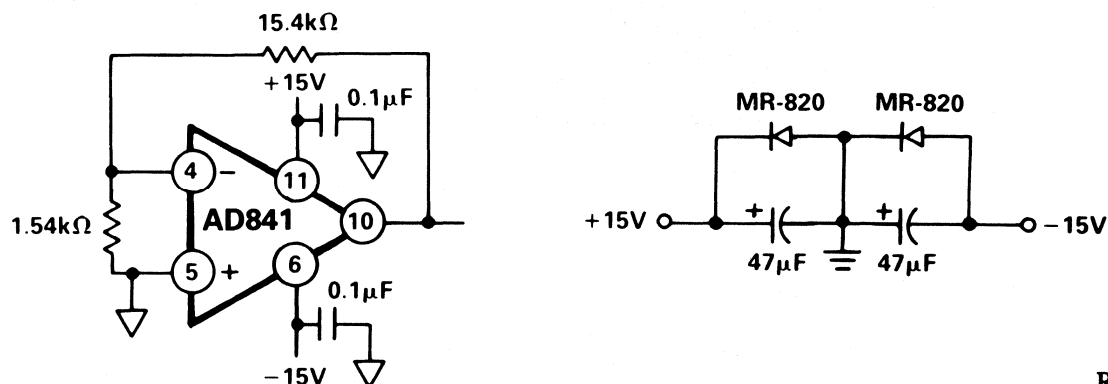


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



REV. A

1.1 Scope.

This specification covers the detail requirements for a high speed, fast settling monolithic, operational amplifier which is stable at closed loop gains of two or greater.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD842S(X)/883B

1.2.3 Case Outline

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-14	14-Pin Cerdip Package
H	H-12A	12-Pin TO-8 Metal Can Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.4 W
Input Common-Mode Voltage, Max Safe	$\pm V_S$
Differential Input Voltage	$\pm 6\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so that T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$. Junction temperatures greater than $+150^\circ\text{C}$ may cause significant degradation of performance. Therefore, use of a heat sink is recommended if the device is used in high temperature or high output current applications.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 30^\circ\text{C/W}$ for Q-14
θ_{JA}	$= 110^\circ\text{C/W}$ for Q-14
θ_{JC}	$= 30^\circ\text{C/W}$ for H-12A
θ_{JA}	$= 100^\circ\text{C/W}$ for H-12A

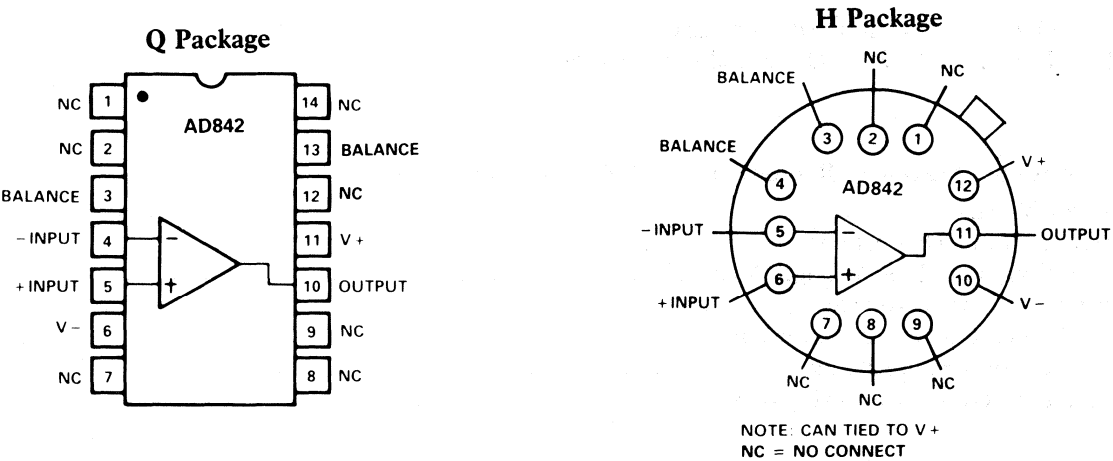
AD842 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Conditions ¹	Units
Input Offset Voltage	V _{OS}	–1	1.5	1.5	3.5		±mV max
Input Bias Current	I _B	–1	8	8	12	V _{IN} = 0 V	±µA max
Input Offset Current	I _{OS}	–1	0.4	0.4	0.6		±µA max
Common-Mode Voltage Range	CMVR	–1	10	10	10		±V min
Common-Mode Rejection Ratio	CMRR	–1	86	86	80	V _{CM} = ±10 V	dB min
Open Loop Gain	A _{OL}	–1	40	40	20	V _{OUT} = ±10 V, R _{LOAD} = 500 Ω	V/mV min
Output Voltage Swing	V _{OUT}	–1	10	10	10	R _{LOAD} = 500 Ω	±V min
Output Current	I _{OUT}	–1	100			V _{OUT} = ±10 V	±mA min
Slew Rate	SR	–1	300				V/µs min
Power Supply Rejection	PSRR	–1	86	86	80	V _S = ±5 V to ±18 V	dB min
Power Supply Current	I _Q	–1	14	14	19	V _{OUT} = 0	mA max

NOTE
¹V_S = ±15 V, unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

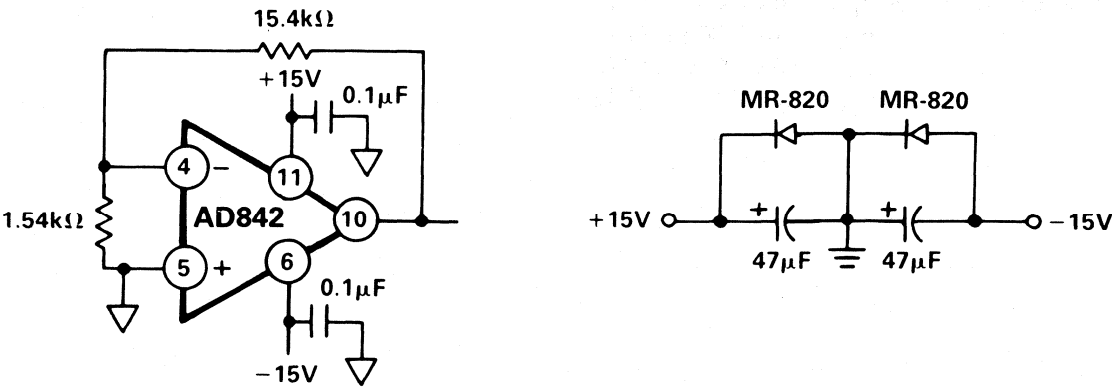


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-in Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, monolithic, laser-trimmed CBFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD843S(Q)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8	8-Pin Cerdip Package
H	H-12A	12-Pin Metal Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.35 W
Input Voltage	$\pm 18\text{ V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so the T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 22^\circ\text{C/W}$ for Q-8
θ_{JA}	$= 110^\circ\text{C/W}$ for Q-8
θ_{JC}	$= 65^\circ\text{C/W}$ for H-12A
θ_{JA}	$= 80^\circ\text{C/W}$ for H-12A

AD843 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	–1	15	15	10		V _{OUT} = ±10 V, R _L = 500 Ω	V/mV min
Slew Rate	t _{SR}	–1	160	160			Gain = –1	V/μs min
Output Voltage Swing	V _{OUT}	–1	±10	±10			R _L ≥ 500 Ω	±V min
Input Offset Voltage ²	V _{OS}	–1	2	2	4.5			±mV max
Input Offset Drift	TC V _{OS}	–1	12					±μV/°C max
Input Bias Current ³	I _B	–1	2.5	2.5				±nA max
Input Offset Current ³	I _{OS}	–1	1	1				±nA max
Common Mode Rejection Ratio	CMRR	–1	60	60	60			dB min
Common Mode Voltage Range	CMVR	–1	10	10	10			±V min
Power Supply Current	I _Q	–1	13	13	16			mA max
Power Supply Rejection Ratio	PSRR	–1	65	65	62		V _S = ±5 V to ±18 V	dB min

NOTES

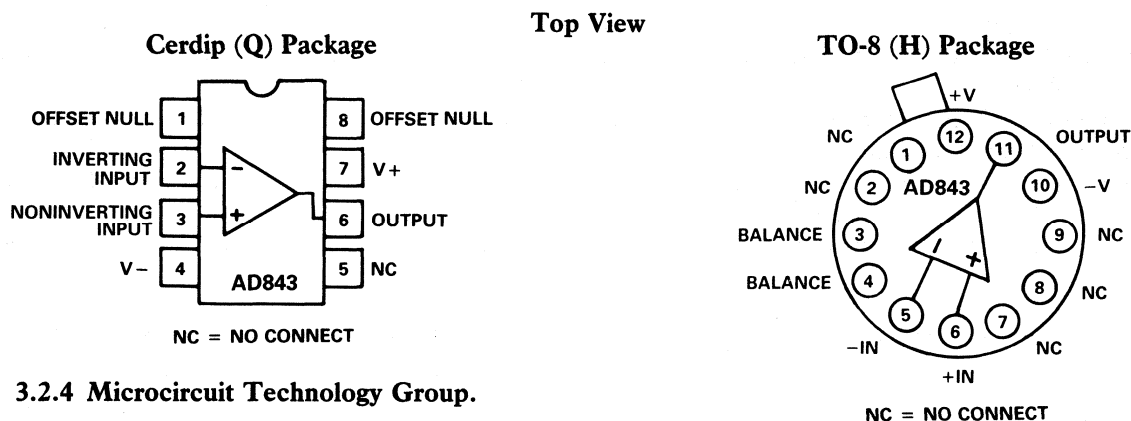
¹T_A = +25°C and V_S = ±15 V, unless otherwise noted.

²Input offset voltage specifications are guaranteed with V_{OS} unnullled at T_A = +25°C.

³Bias current specifications guaranteed after 5 minutes of operation at T_A = +25°C. For temperatures above +25°C, the current doubles every 10°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

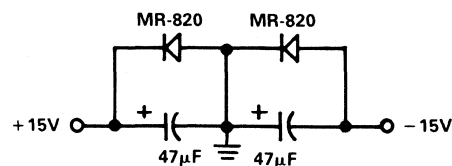
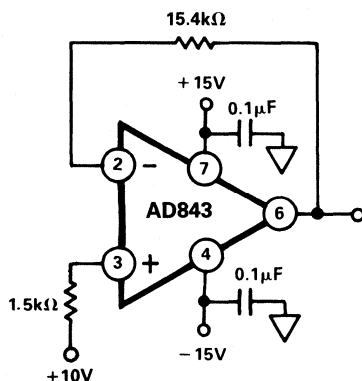


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, monolithic, laser-trimmed current-feedback high speed amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD844S(Q)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation	1.0 W
Common Mode Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$\pm 6\text{ V}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

AD844 SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V_{OS}	-1	300	300	500		$\pm \mu V$ max
Input Offset Voltage Drift	TCV_{OS}	-1	5				$\pm \mu V/^{\circ}C$ max
Power Supply Rejection Ratio	PSRR	-1	20	20	20	5 V–18 V ³	$\mu V/V$ max
Common-Mode Rejection Ratio	CMRR	-1	35	35	35	$V_{CM} = \pm 10 V$	$\mu V/V$ max
Input Bias Current ⁴	I_B	-1 -1	450 400	450 400	2500 1300	Inverting Noninverting	$\pm nA$ max
Input Bias Current Drift	TCI_B	-1 -1	30 15			Inverting Noninverting	$nA/^{\circ}C$ max
Input Bias Current vs. Supply	I_{BPSR}	-1 -1	250 150	250 150	300 200	Inverting 5 V–18 V ³ Noninverting 5 V–18 V ³	nA/V max
Input Bias Current vs. Common Mode	I_{BCMR}	-1 -1	160 150	160 150	200 200	Inverting $V_{CM} = \pm 10 V$ Noninverting $V_{CM} = \pm 10 V$	nA/V max
Differential Input Resistance	R_{IN}	-1 -1	65 7			Inverting Noninverting	Ω max $M\Omega$ min
Common-Mode Voltage Range	CMVR	-1	10				$\pm V$ min
Open Loop Transresistance	TZ	-1	2.2	2.2	1.3	$V_O = \pm 10 V$ $R_L = 500 \Omega$	$M\Omega$ min
Output Voltage Swing	V_{OUT}	-1	10	10		$R_L = 500 \Omega$	$\pm V$ min
Quiescent Current	I_Q	-1	7.5	7.5	9.5		mA max

NOTES

¹ $T_A = +25^{\circ}C$ and $V_S = \pm 15 V$, unless otherwise noted.

²Input offset voltage specifications are guaranteed after 5 minutes at $T_A = +25^{\circ}C$.

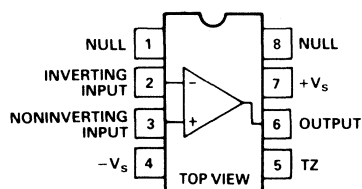
³Test conditions: $+V_S = 15 V$, $-V_S = 5 V$ to $18 V$ and $+V_S = 5 V$ to $18 V$, $-V_S = -15 V$.

⁴Bias current specifications are guaranteed maximum after 5 minutes at $T_A = +25^{\circ}C$.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Q Package (Cerdip)

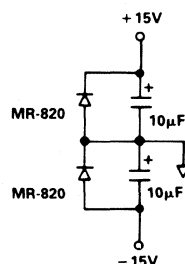
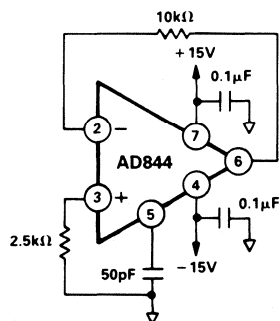


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-in Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



REV. A

1.1 Scope.

This specification covers the detail requirements for a precision monolithic laser-trimmed CBFET amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD845S(Q)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.1 W
Input Voltage	$\pm 18\text{ V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so the t_j does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-8
 $\theta_{JA} = 110^\circ\text{C/W}$ for Q-8

AD845 – SPECIFICATIONS

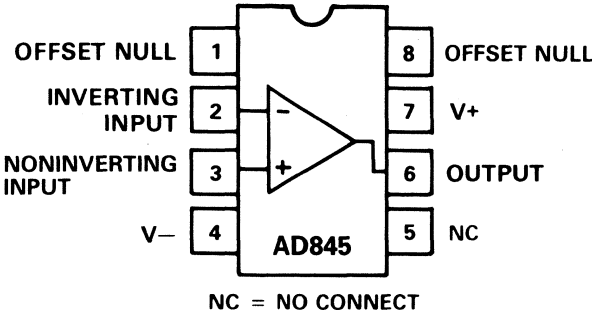
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Conditions ¹	Units
Gain Open Loop	A_{OL}	-1	200	200			$V_{OUT} = \pm 10\text{ V}, R_L \geq 2\text{ k}\Omega$	V/mV min
		-1	100	100	50		$V_{OUT} = \pm 10\text{ V}, R_L = 500\text{ }\Omega$	V/mV min
Slew Rate	t_{SR}	-1	94	94			Gain = -1	V/ μ s min
Output Voltage Swing	V_{OUT}	-1	12.5	12.5	12		$R_L \geq 500\text{ }\Omega$	$\pm$ V min
Input Offset Voltage ²	V_{OS}	-1	1	1	2			$\pm$ mV max
Input Offset Drift	TC V_{OS}	-1	10		10			$\pm$ μ V/ $^{\circ}$ C max
Input Bias Current ³	I_B	-1	2	2	500			$\pm$ nA max
Input Offset Current ³	I_{OS}	-1	0.3	0.3	20			$\pm$ nA max
Common-Mode Rejection Ratio	CMRR	-1	86	86				dB min
Common-Mode Voltage Range	CMVR	-1	10	10	10			$\pm$ V min
Power Supply Current	I_Q	-1	12	12	12			mA max
Power Supply Rejection Ratio	PSRR	-1	88	88			$V_S = \pm 5\text{ V to } \pm 15\text{ V}$	dB min

NOTES

¹ $T_A = +25^{\circ}\text{C}$, $V_S = \pm 15\text{ V}$ unless otherwise noted.
²Input offset voltage specifications are guaranteed with V_{OS} unnullled at $T_A = +25^{\circ}\text{C}$.
³Bias current specifications guaranteed after 5 minutes of operation at $T_A = +25^{\circ}\text{C}$. For temperatures above $+25^{\circ}\text{C}$, the current doubles every 10°C .

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

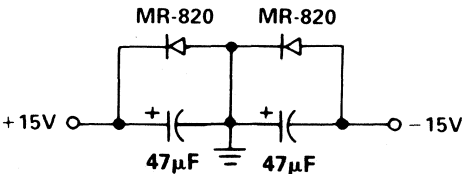
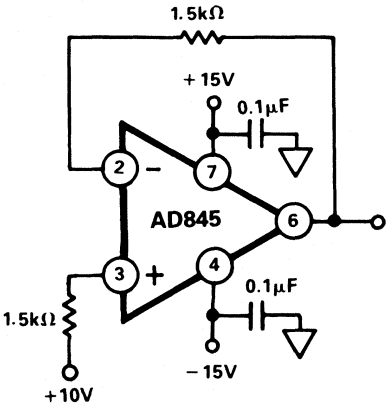


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a precision, monolithic laser-trimmed high speed amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD846S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip Package
H	H-8A	8-Pin TO-99 Metal Can Package

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation Q/H	1.5W/1.0W
Input Voltage	$\pm 18\text{V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$\pm 6\text{V}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 35^\circ\text{C/W}$ for Q-8A
θ_{JA}	$= 100^\circ\text{C/W}$ for Q-8A
θ_{JC}	$= 35^\circ\text{C/W}$ for H-8A
θ_{JA}	$= 150^\circ\text{C/W}$ for H-8A

AD846 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Input Offset Voltage ²	V _{OS}	– 1	200	200	350		± μV max
Input Offset Voltage Drift	TCV _{OS}	– 1	5.5				± μV/°C max
Power Supply Rejection Ratio	PSRR	– 1	110	110	104	5V–18V ³	dB min
Common-Mode Rejection Ratio	CMRR	– 1	110	110	104	V _{CM} = ± 10V	dB min
Input Bias Current ⁴	I _B	– 1 – 1	450 15	450 15	1500 20	Inverting Noninverting	± nA max ± μA max
Input Bias Current Drift	TCI _B	– 1 – 1	20 80			Inverting Noninverting	nA/°C max
Input Bias Current vs. Supply	I _{BPSR}	– 1 – 1	15 15	15 15	25 20	Inverting 5V–18V ³ Noninverting 5V–18V ³	nA/V max
Input Bias Current vs. Common Mode	I _{BCMR}	– 1 – 1	10 15	10 15	20 20	Inverting V _{CM} = ± 10V Noninverting V _{CM} = ± 10V	nA/V max
Open-Loop Transresistance	TZ	– 1	100	100	50	V _O = ± 10V R _L = 500Ω	MΩ min
Output Voltage Swing	V _{OUT}	– 1	10	10		R _L = 500Ω	± V min
Quiescent Current	I _Q	– 1	6.0	6.0	7		mA max

NOTES

¹T_A = +25°C and V_S = ± 15V, unless otherwise noted.

²Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

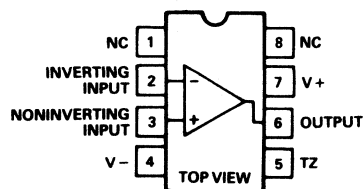
³Test conditions: +V_S = 15V, –V_S = 5V to 18V and +V_S = 5V to 18V, –V_S = –15V.

⁴Bias current specifications are guaranteed maximum after 5 minutes at T_A = +25°C.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Q Package (Cerdip)

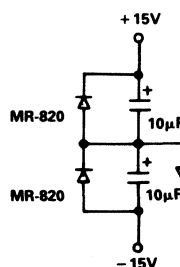
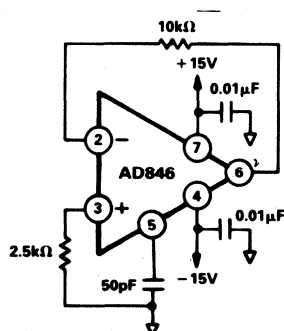


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high speed, low power, unity-gain stable operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD847SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.1 W
Input Common-Mode Voltage, Max Safe	$\pm V_S$
Differential Input Voltage	$\pm 6\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so the T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$.

1.5 Thermal Characteristics.

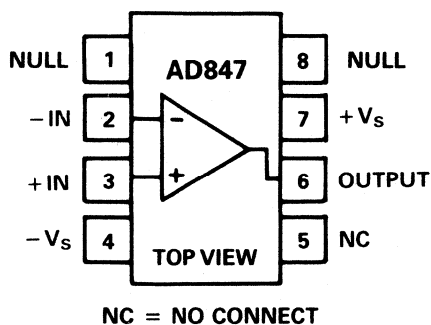
Thermal Resistance $\theta_{JA} = 100^\circ\text{C}/\text{W}$
 $\theta_{JC} = 30^\circ\text{C}/\text{W}$

AD847 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	V _S	Test Condition	Units
Input Offset Voltage	V _{OS}	-1	1	1	4	±5 V		±mV max
Input Bias Current	I _B	-1	5	5	7.5	±5 V, ±15 V	V _{IN} = 0 V	±μA max
Input Offset Current	I _{OS}	-1	0.3	0.3	0.4	±5 V, ±15 V		±μA max
Open Loop Gain	A _{OL}	-1	2	2	1	±5 V	V _{OUT} = ±2.5 V, R _{LOAD} = 500 Ω	V/mV min
		-1	3	3	1.5	±15 V	V _{OUT} = ±10 V, R _{LOAD} = 1 kΩ	V/mV min
Common-Mode Rejection Ratio	CMRR	-1	80	80		±5 V	V _{CM} = ±2.5 V	dB min
		-1	80	80	75	±15 V	V _{CM} = ±12 V	dB min
Output Voltage Swing	V _{OUT}	-1	3	3		±5 V	R _{LOAD} = 500 Ω	±V min
		-1	2.5	2.5		±5 V	R _{LOAD} = 150 Ω	±V min
		-1	12	12		±15 V	R _{LOAD} = 1 kΩ	±V min
		-1	10	10		±15 V	R _{LOAD} = 500 Ω	±V min
Slew Rate	SR	-1	225			±15 V		V/μs min
Power Supply Rejection	PSRR	-1	75	75	72		V _S = ±5 V to ±15 V	dB min
Power Supply Current	I _Q	-1	5.7	5.7	7.8	±5 V	V _{OUT} = 0	mA max
		-1	6.3	6.3	8.4	±15 V	V _{OUT} = 0	mA max

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

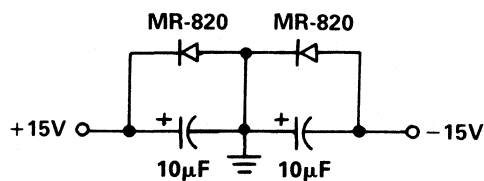
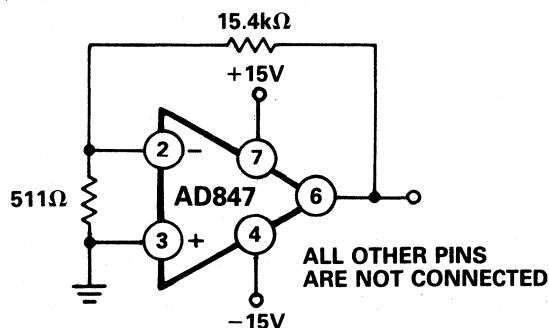


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-in Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high speed, low power, operational amplifier that is stable at closed loop gains of 5 or greater.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD848SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.1 W
Input Common-Mode Voltage, Max Safe	$\pm V_S$
Differential Input Voltage	$\pm 6\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so the T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$.

1.5 Thermal Characteristics.

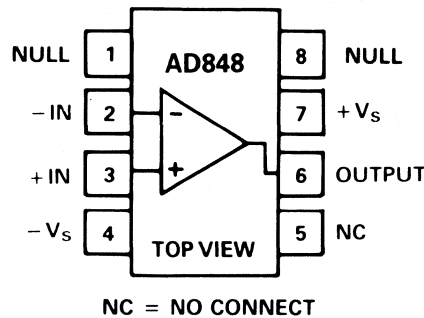
Thermal Resistance θ_{JA}	$= 110^\circ\text{C/W}$
θ_{JC}	$= 30^\circ\text{C/W}$

AD848 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	V _S	Test Condition	Units
Input Offset Voltage	V _{OS}	-1 -1	1 2.3	1 2.3	2 3.5	±5 V ±15 V		±mV max ±mV max
Input Bias Current	I _B	-1	5	5	7.5	±5 V, ±15 V	V _{IN} = 0 V	±µA max
Input Offset Current	I _{OS}	-1	0.3	0.3	0.4	±5 V, ±15 V		±µA max
Open Loop Gain	A _{OL}	-1 -1	9 12	9 12	5 6	±5 V ±15 V	V _{OUT} = ±2.5 V, R _{LOAD} = 500 Ω V _{OUT} = ±10 V, R _{LOAD} = 1 kΩ	V/mV min V/mV min
Common-Mode Rejection Ratio	CMRR	-1 -1	92 92	92 92		±5 V ±15 V	V _{CM} = ±2.5 V V _{CM} = ±12 V	dB min dB min
Output Voltage Swing	V _{OUT}	-1 -1 -1 -1	3 2.5 12 10	3 2.5 12 10		±5 V ±5 V ±15 V ±15 V	R _{LOAD} = 500 Ω R _{LOAD} = 150 Ω R _{LOAD} = 1 kΩ R _{LOAD} = 500 Ω	±V min ±V min ±V min ±V min
Slew Rate	SR	-1	225			±15 V		V/µs min
Power Supply Rejection	PSRR	-1	85	85	80		V _S = ±4.5 V to ±18 V	dB min
Power Supply Current	I _Q	-1 -1	6.0 6.8	6.0 6.8	8.3 9.0	±5 V ±15 V	V _{OUT} = 0 V _{OUT} = 0	mA max mA max

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

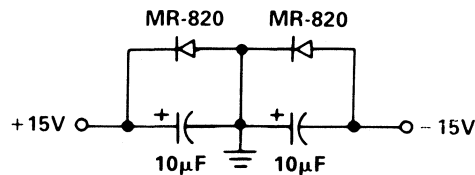
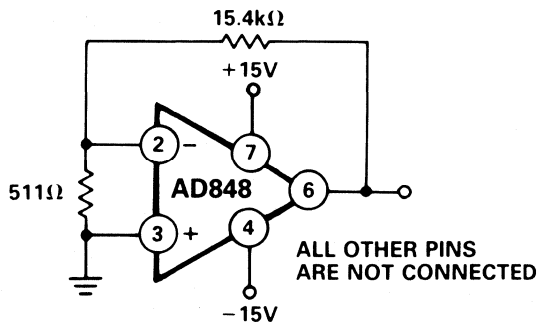


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-in Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high speed, low power operational amplifier that is stable at closed loop gains of 25 or greater.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD849SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	1.1 W
Input Common-Mode Voltage, Max Safe	$\pm V_S$
Differential Input Voltage	$\pm 6\text{ V}$
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$+300^\circ\text{C}$

NOTE

¹Maximum internal power dissipation is specified so the T_J does not exceed $+150^\circ\text{C}$ at an ambient temperature of $+25^\circ\text{C}$.

1.5 Thermal Characteristics.

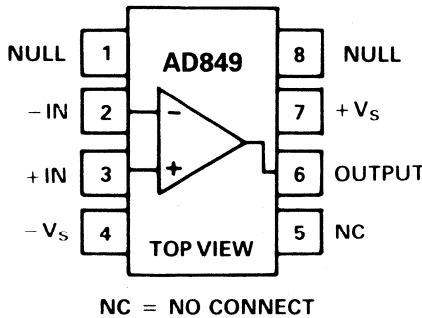
Thermal Resistance θ_{JA}	$= 110^\circ\text{C/W}$
θ_{JC}	$= 30^\circ\text{C/W}$

AD849 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	V _S	Test Condition	Units
Input Offset Voltage	V _{OS}	-1	0.75	0.75	1.0	±5 V, ±15 V		±mV max
Input Bias Current	I _B	-1	5	5	7.5	±5 V, ±15 V	V _{IN} = 0 V	±μA max
Input Offset Current	I _{OS}	-1	0.3	0.3	0.4	±5 V, ±15 V		±μA max
Open Loop Gain	A _{OL}	-1	30	30	15	±5 V	V _{OUT} = ±2.5 V, R _{LOAD} = 500 Ω	V/mV min
		-1	45	45	25	±15 V	V _{OUT} = ±10 V, R _{LOAD} = 1 kΩ	V/mV min
Common-Mode Rejection Ratio	CMRR	-1	100	100		±5 V	V _{CM} = ±2.5 V	dB min
		-1	100	100	96	±15 V	V _{CM} = ±12 V	dB min
Output Voltage Swing	V _{OUT}	-1	3	3		±5 V	R _{LOAD} = 500 Ω	±V min
		-1	2.5	2.5		±5 V	R _{LOAD} = 150 Ω	±V min
		-1	12	12		±15 V	R _{LOAD} = 1 kΩ	±V min
		-1	10	10		±15 V	R _{LOAD} = 500 Ω	±V min
Slew Rate	SR	-1	225			±15 V		V/μs min
Power Supply Rejection	PSRR	-1	98	98	94		V _S = ±4.5 V to ±18 V	dB min
Power Supply Current	I _Q	-1	6.0	6.0	8.3	±5 V	V _{OUT} = 0	mA max
		-1	6.8	6.8	9.0	±15 V	V _{OUT} = 0	mA max

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

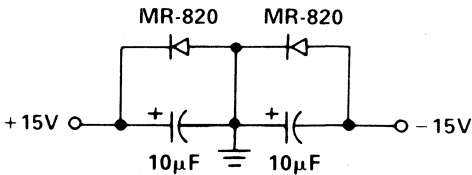
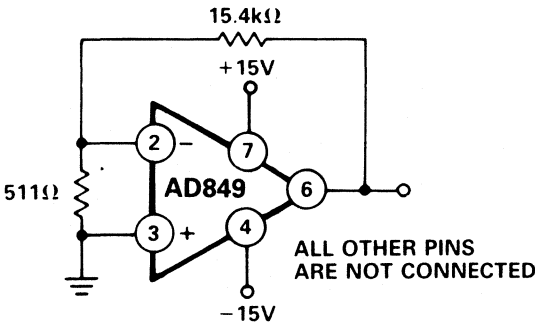


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (85).

4.2.1 Life Test/Burn-in Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a high speed, high slew rate, fast-settling monolithic amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD5539SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-14.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	+ 10V
Internal Power Dissipation ¹	550mW
Differential Input Voltage	0.25V
Common-Mode Range ($T_{\min}$ to $T_{\max}$)	$\pm 2.5\text{V}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT	DERATE ABOVE MAXIMUM
Package Type	Temperature for Rating	Ambient Temperature
Q-14	75°C	$6.7\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 220^\circ\text{C}/\text{W}$
 $\theta_{JA} = 110^\circ\text{C}/\text{W}$

AD5539 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	– 1	48	48	46		V _O = +2.3V, –1.7V R _L = 2kΩ	dB min
Gain Bandwidth Product ²	GBW	– 1	1400				A _{CL} = 26dB	MHz min
Full Power Bandwidth ²	FBW	– 1	82/65/68				A _{CL} = 7/20/2	MHz min
Slew Rate ²	t _{SR}	– 1	600					V/μs min
Settling Time ²	t _{SL}	– 1	12				To 0.1%	ns max
Output Voltage Swing	V _{OUT}	– 1	+2.3, –1.7	+2.3, –1.7			R _L = 150Ω, 470Ω to –V _S	± V min
			+2.5, –2.0	+2.5, –2.0	+2.3, –1.5		R _L = 2kΩ	
Input Offset Voltage ³	V _{OS}	– 1	3	3	5			± mV max
Input Offset Current ⁴	I _{OS}	– 1	1	1	3			± μA max
Input Bias Current ⁴	I _B	– 1	13	13	25		V _{CM} = 0	± μA max
Input Resistance Differential	R _{DIFF}	– 1	100					kΩ min
Common-Mode Rejection Ratio	CMRR	– 1	70	70	60		V _{CM} = 1.7, R _S = 100Ω	dB min
Differential Input Voltage ⁵	V _{DIFF}	– 1	250					± mV max
Common-Mode Voltage Range	CMVR	– 1	2.5					± V min
Input Noise Voltage Density	E _N	– 1	4				f = 1kHz, R _S = 50Ω	nV/√Hz max
Power Supply Current	I _Q	– 1	17	17	18		Initial I _{CC} +	mA max
			14	14	15		Initial I _{CC} –	mA max
Rejection Ratio	PSRR	– 1	1000	1000	2000			± μV/V max

NOTE

¹T_A = +25°C, V_S = ±15V.

²R_L = 150Ω, 470Ω to –V_S.

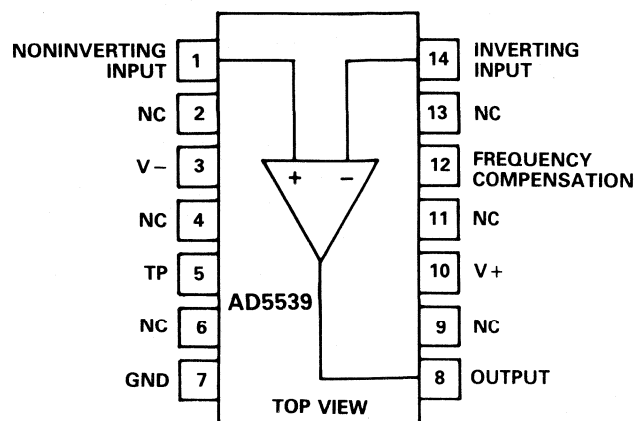
³Input offset voltage specifications are guaranteed after five minutes of operation at T_A = +25°C.

⁴Bias current specifications are guaranteed maximum at either input after five minutes of operation at T_A = +25°C.

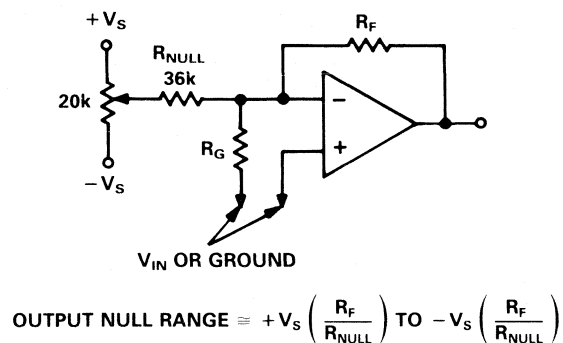
⁵Defined as voltage between inputs, such that neither exceed ±2.5V from ground.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



OFFSET NULL CONFIGURATION

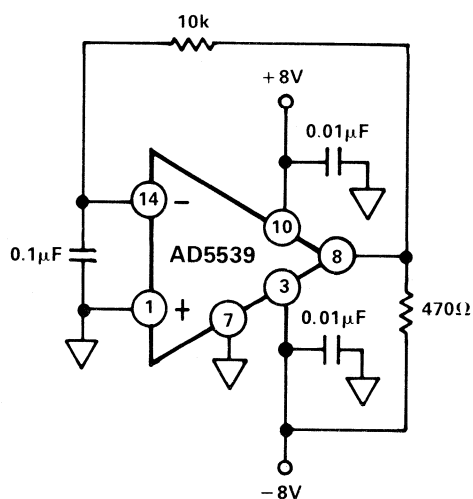


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter which can attenuate an analog signal over the range 0 to -88.5dB in 0.375dB steps.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7111T(X)/883B
-2	AD7111U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline:

(X)	Package	Description
E	E-20A	20-Terminal LCC
Q	Q-16	16-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND		+7V
V_{IN} to AGND		+35V
Digital Input Voltage to DGND		$-0.3\text{V}, V_{DD}$
Output Voltage (Pin 1) to AGND		$-0.3\text{V}, V_{DD}$
V_{RFB} to AGND		$\pm 35\text{V}$
AGND to DGND		0 to V_{DD}
DGND to AGND		0 to V_{DD}
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derate above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)		$+300^\circ\text{C}$

NOTE

Pin numbers refer to DIP package ONLY.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-16 and E-20A

AD7111 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T _{min} to T _{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Error	A _E	-1 -2	0.20 0.15	0.15 0.15	0.2 0.15	0.10		± dB max
0.375dB Steps: Accuracy = ± 0.17dB ²	RA	-1 -2	0-30 0-36	0-30 0-30	0-30 0-36	0-36		dB min
0.75dB Steps: Accuracy = ± 0.35dB ²	RA	-1 -2	0-36 0-42	0-42 0-42	0-36 0-42	0-48		dB min
1.5dB Steps: Accuracy = ± 0.7dB ²	RA	-1 -2	0-42 0-48	0-48 0-48	0-42 0-48	0-54		dB min
3.0dB Steps: Accuracy = ± 1.4dB ²	RA	-1 -2	0-48 0-54	0-60 0-60	0-48 0-54	0-66		dB min
6.0dB Steps: Accuracy = ± 2.7dB ²	RA	-1 -2	0-60 0-60	0-60 0-60	0-60 0-60	0-72		dB min
Nominal 0.375dB Step ³	MR	-1 -2	0-48 0-54	0-48 0-48	0-48 0-54	0-54		dB min
Nominal 0.75dB Step ³	MR	-1 -2	0-60 0-66	0-72 0-72	0-60 0-66			dB min
Nominal 1.5dB Step ³	MR	-1 -2	0-72 0-78	0-85.5 0-85.5	0-72 0-78	0-88.5		dB min
Nominal 3.0dB Step ³	MR	-1, 2	0-88.5	0-88.5	0-88.5			dB min
Nominal 6.0dB Step ³	MR	-1, 2	0-88.5	0-88.5	0-88.5			dB min
DC Supply Rejection	PSR	-1, 2	0.005				ΔV _{DD} = ± 10% Input Data Latch Loaded with 0000 0000	± dB per % max
Propagation Delay	t _{PD}	-1, 2	4.5				R _{OUT1} = 100Ω, C _{OUT1} = 13pF; Time required for the output current to reach 90% of its final value for a Full Scale Change. Measured from $\overline{WR}$ going high, CS = 0V.	μs max
Feedthrough ⁴	FT	-1 -2	68 72				Full scale Change. Measured from $\overline{WR}$ going high, CS = 0V. V _{IN} = 6V rms, 1kHz sinewave. Input Data loaded with 1111 1111.	- dB max
Output Capacitance	C _{OUT}	-1, 2	185					pF max
V _{IN} Input Resistance	R _{IN}	-1 -2 -1 -2	7 9 18 15	7 9 18 15	7 9 18 15			kΩ min kΩ max
R _{FB} Input Resistance	R _{FB}	-1 -2 -1 -2	7.3 9.3 18.8 15.7	7.3 9.3 18.8 15.7	7.3 9.3 18.8 15.7			kΩ min kΩ max
Input High Voltage	V _{IH}	-1, 2	2.4	2.4	2.4			V min
Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V max
Input Leakage Current	I _{IN}	-1, 2	10	1	10		Digital Inputs = V _{DD} or 0V	± μA max
Input Capacitance	C _{IN}	-1, 2	7					pF max
Supply Current	I _{DD}	-1, 2	4 1	1 0.5	4 1		Digital Inputs = V _{IH} or V _{IL} . Digital Inputs = 0V or V _{DD}	mA max mA max
Chip-Select-to-Write Setup Time ⁵	t _{CS}	-1, 2	0					ns min
Chip-Select-to-Write Hold Time ⁵	t _{CH}	-1, 2	0					ns min
Write Pulse Width ⁵	t _{WR}	-1, 2	500					ns min
Data Valid to Write Setup Time ⁵	t _{DS}	-1, 2	250					ns min
Data Valid to Hold Time ⁵	t _{DH}	-1, 2	10					ns min
Refresh Time ⁵	t _{RFSH}	-1, 2	4.5					ns min

NOTES

¹V_{DD} = + 5V; V_{PIN1} = V_{PIN2} = 0V; V_{IN} = - 10V.

²Accuracy is measured using the internal R_{FB} and includes effects of leakage current and gain TC. ⁵Timing per Figure 1.

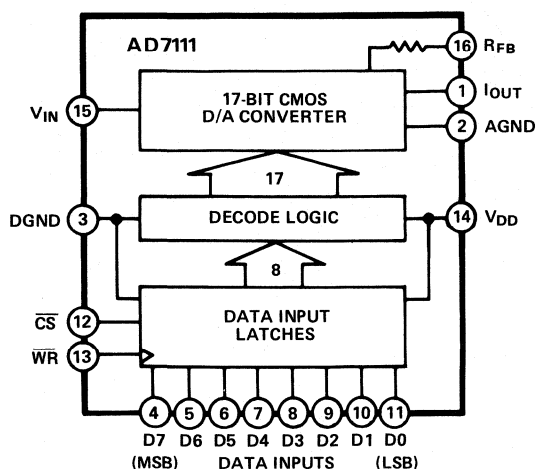
³Monotonic range for specified step.

⁴Feedthrough can be further reduced by connecting the metal lid to ground.

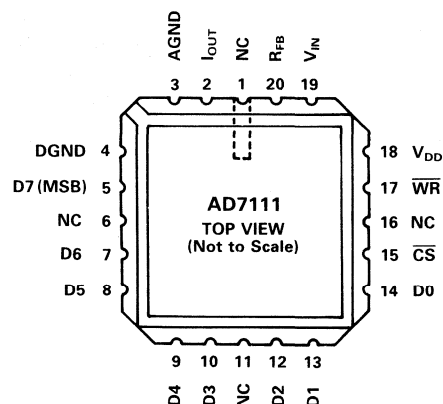
Table 1.

REV. B

3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

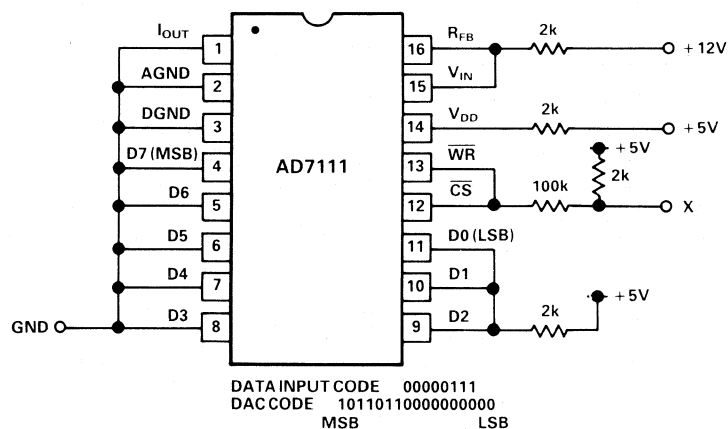


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE
 ON POWER UP APPLY 0V TO POINT X TO
 LOAD THE INPUT DATA INTO THE DAC.



Table 2. Ideal Attenuation in dB vs. Input Code

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter which attenuates an analog input signal over the range 0 to -85.5dB in 1.5dB steps.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7118T(X)/883B
-2	AD7118U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-20A	20-Contact LCC
Q	Q-14	20-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	0V, +17V
V_{IN} to AGND	$\pm 35\text{V}$
Digital Input Voltage to DGND	-0.3V , V_{DD}
Output Voltage (Pin 14) to AGND	-0.3V to V_{DD}
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

NOTE

Pin numbers refer to DIP package ONLY.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

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AD7118 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Relative Accuracy ²	RA	-1	0.5	0.5	0.5		0 to -30dB	± dB max
		-2	0.4	0.5	0.4	0.35		
		-1	0.8	0.75	0.8		-31.5 to -42dB	
		-2	0.7	0.75	0.7	0.5		
Monotonic Range	MR	-1	0-66	0-85.5	0-66		Nominal 1.5dB Steps	- dB
		-2	0-72	0-85.5	0-72			
		-1, 2	0-85.5	0-85.5	0-85.5		Nominal 3.0dB Steps	
DC Supply Rejection	PSR	-1, 2	0.005	0.005	0.005		$\Delta V_{DD} = \pm 10\%$, Input Code = 100000	± dB/% max
Propagation Delay	t_{PD}	-1, 2	0.5				$R_{OUT1} = 100\Omega$, $C_{OUT1} = 13pF$; Time required for the output current to reach 90% of its final value for a Full Scale Change.	µs max
Feedthrough ³	FT	-1	63				$V_{IN} = 6V$ rms, 1kHz sinewave. Input Code = 111111	- dB max
		-2	68					dB max
Input Resistance	R_{IN}	-1, 2	9	9	9			kΩ min
		-1	21	21	21			
		-2	17	17	17			
Input Resistance	R_{FB}	-1, 2	9.45	9.45	9.45			kΩ min
		-1	22	22	22			
		-2	18	18	18			
Digital Input High Voltage	V_{IH}	-1, 2	13.5	13.5	13.5			V min
Digital Input Low Voltage	V_{IL}	-1, 2	1.5	1.5	1.5			V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10		Digital Inputs = V_{DD}	± µA max
Digital Input Capacitance	C_{IN}	-1, 2	7					pF max
Supply Current	I_{DD}	-1, 2	2	1	2		Digital Inputs = 0V or V_{DD}	mA max

NOTES

¹ $V_{PIN1} = V_{PIN14} = 0V$; $V_{IN} = -10V$.

²Accuracy is measured using the internal R_{FB} and includes effects of leakage current and gain TC.

³Feedthrough can be further reduced by connecting metal lid to DGND.

Table 1.

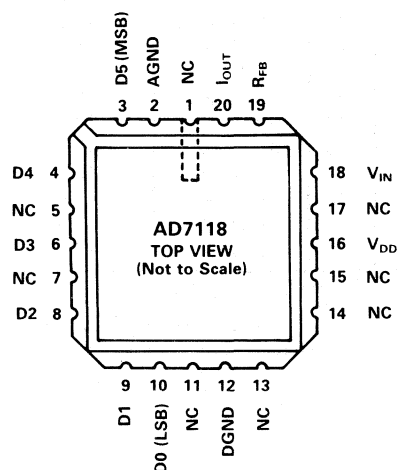
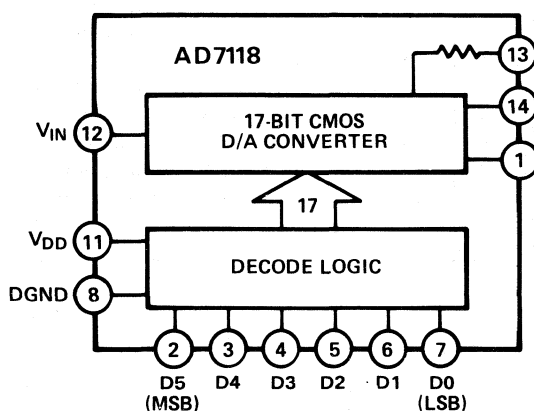
Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Relative Accuracy ²	RA	-1	0.5	0.5	0.5		0 to -30dB	$\pm$ dB max
		-2	0.4	0.5	0.4	0.35	-31.5 to -42dB	
		-1, 2	1.0 0.8	0.75 0.75	1.0 0.8	0.7	-43.5 to -48dB	
Monotonic Range	MR	-1	0-66	0-85.5	0-66		Nominal 1.5dB Steps	- dB
		-2	0-72	0-85.5	0-72		Nominal 3.0dB Steps	
DC Supply Rejection	PSR	-1, 2	0.01	0.01	0.01		$\Delta V_{DD} = \pm 10\%$, Input Code = 100000	$\pm$ dB/% max
Propagation Delay	t_{PD}	-1, 2	2.2				$R_{OUT1} = 100\Omega$, $C_{OUT1} = 13pF$; Time required for the output current to reach 90% of its final value for a Full Scale Change.	μs max
Feedthrough ³	FT	-1	63				$V_{IN} = 6V$ rms, 1kHz sinewave. Input Code = 111111	- dB max
		-2	68					dB max
Input Resistance	R_{IN}	-1, 2	9					k Ω min
		-1 -2	21 17					k Ω max
Input Resistance	R_{FB}	-1, 2	9.45	9.45	9.45			k Ω min
		-1 -2	22 18	22 18	22 18			k Ω max
Digital Input High Voltage	V_{IH}	-1, 2	3.0	3.0	3.0			V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10		Digital Inputs = V_{DD}	$\pm \mu A$ max
Digital Input Capacitance	C_{IN}	-1, 2	7					pF max
Supply Current	I_{DD}	-1, 2	1	0.5	1		Digital Inputs = 0V or V_{DD}	mA max

NOTES

¹ $V_{PIN1} = V_{PIN14} = 0V$; $V_{IN} = -10V$.²Accuracy is measured using the internal R_{FB} and includes effects of leakage current and gain TC.³Feedthrough can be further reduced by connecting metal lid to DGND.

Table 2.

3.2.1 Functional Block Diagram and Terminal Assignments.

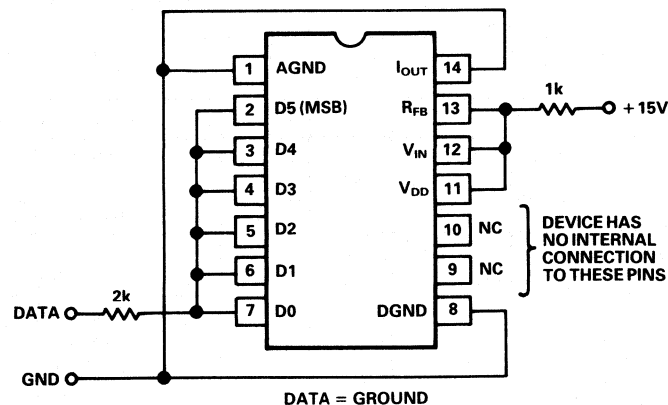


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



N	Digital Input D5 D0	Attenuation dB	VOUT ¹	N	Digital Input	Attenuation	VOUT ¹
0	00 00 00	0.0	10.00	31	01 11 11	46.5	0.0473
1	00 00 01	1.5	8.414	32	10 00 00	48.0	0.0398
2	00 00 10	3.0	7.079	33	10 00 01	49.5	0.0335
3	00 00 11	4.5	5.957	34	10 00 10	51.0	0.0282
4	00 01 00	6.0	5.012	35	10 00 11	52.5	0.0237
5	00 01 01	7.5	4.217	36	10 01 00	54.0	0.0200
6	00 01 10	9.0	3.548	37	10 01 01	55.5	0.0168
7	00 01 11	10.5	2.985	38	10 01 10	57.0	0.0141
8	00 10 00	12.0	2.512	39	10 01 11	58.5	0.0119
9	00 10 01	13.5	2.113	40	10 10 00	60.0	0.0100
10	00 10 10	15.0	1.778	41	10 10 01	61.5	0.00841
11	00 10 11	16.5	1.496	42	10 10 10	63.0	0.00708
12	00 11 00	18.0	1.259	43	10 10 11	64.5	0.00596
13	00 11 01	19.5	1.059	44	10 11 00	66.0	0.00501
14	00 11 10	21.0	0.891	45	10 11 01	67.5	0.00422
15	00 11 11	22.5	0.750	46	10 11 10	69.0	0.00355
16	01 00 00	24.0	0.631	47	10 11 11	70.5	0.00299
17	01 00 01	25.5	0.531	48	11 00 00	72.0	0.00251
18	01 00 10	27.0	0.447	49	11 00 01	73.5	0.00211
19	01 00 11	28.5	0.376	50	11 00 10	75.0	0.00178
20	01 01 00	30.0	0.316	51	11 00 11	76.5	0.00150
21	01 01 01	31.5	0.266	52	11 01 00	78.0	0.00126
22	01 01 10	33.0	0.224	53	11 01 01	79.5	0.00106
23	01 01 11	34.5	0.188	54	11 01 10	81.0	0.000891
24	01 10 00	36.0	0.158	55	11 01 11	82.5	0.000750
25	01 10 01	37.5	0.133	56	11 10 00	84.0	0.000631
26	01 10 10	39.0	0.112	57	11 10 01	85.5	0.000531
27	01 10 11	40.5	0.0944	58	11 10 10	87.0	0.000447
28	01 11 00	42.0	0.0794	59	11 10 11	88.5	0.000376
29	01 11 01	43.5	0.0668	60	11 11 XX ²	∞	
30	01 11 10	45.0	0.0562				

NOTES

¹ VIN = -10V dc

² X = 1 or 0. Output is fully muted for N ≥ 60

³ Monotonic operation is not guaranteed for N = 58, 59

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8-bit, voltage output, digital-to-analog converter with output amplifier and double-buffered interface logic. No external trims are required to achieve full specified performance for the part.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number ¹
– 1	AD7224T(X)/883B
– 2	AD7224U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to AGND	– 0.3V, + 17V
V_{DD} to DGND	– 0.3V, + 17V
V_{SS} to AGND	– 7V, V_{DD}
V_{SS} to DGND	– 7V, V_{DD}
V_{DD} to V_{SS}	– 0.3V, + 24V
AGND to DGND	– 0.3V, + V_{DD}
Digital Input Voltage to DGND	– 0.3V, V_{DD}
V_{REF} to AGND	– 0.3V, V_{DD}
V_{OUT} to AGND	V_{SS} , V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-18 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-18 and E-20A

AD7224 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	- 1, 2	8					Bits
Relative Accuracy	RA	- 1	1	1	1		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$	$\pm$ LSB max
		- 2	1/2	1	1/2	1/2		
Total Unadjusted Error	E_T	- 1	2	2	2		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$	$\pm$ LSB max
		- 2	1	2	1			
Differential Nonlinearity	DNL	- 1, 2	1	1	1		Guaranteed Monotonic to 8-Bits	$\pm$ LSB max
Full-Scale Error	A_E	- 1	3/2	3/2	3/2		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$	$\pm$ LSB max
		- 2	1	3/2	1	1		
Zero Code Error	A_{ZCE}	- 1	30	30	30		$V_{DD} = 16.5V, 11.4V$ and $14V; V_{SS} = -5V; V_{REF} = V_{DD} - 4$	$\pm$ mV max
		- 2	20	30	20	20		
Full-Scale Temp Coefficient	dA_E/dT	- 1, 2	20				$V_{DD} = 14V$ to $16.5V, V_{REF} = +10V$	$\pm$ ppm/ $^{\circ}C$ max
Voltage Output Settling Time ²	t_{SL}	- 1, 2	5				Positive Full-Scale Change	μs max
			7				Negative Full-Scale Change	
Voltage Output Slew Rate	t_{SR}	- 1, 2	2.5					V/ μs min
Minimum Load Resistance	RL_{MIN}	- 1, 2	2				$V_{OUT} = +10V; V_{DD} = +14V$	k Ω min
Reference Voltage Range	V_{REF}	- 1, 2	2 to $(V_{DD} - 4)$					V min to V max
Reference Input Resistance	R_I	- 1, 2	8	8	8		$V_{DD} = 14V$	k Ω min
Reference Input Capacitance	C_I	- 1, 2	100				Occurs When DAC Is Loaded with All 1's	pF min
Digital Input High Voltage	V_{IH}	- 1, 2	2.4	2.4	2.4		$V_{DD} = 11.4V; V_{REF} = V_{DD} - 4$	V min
Digital Input Low Voltage	V_{IL}	- 1, 2	0.8	0.8	0.8		$V_{DD} = 11.4V; V_{REF} = V_{DD} - 4$	V max
Digital Input Leakage Current	I_{IN}	- 1, 2	1	1	1		$V_{IN} = 0V$ or $V_{DD}; V_{DD} = 11.4V$	$\pm$ μA max
Digital Input Capacitance	C_I	- 1, 2	8					pF max
Chip Select/Load DAC Pulse Width	t_{LD}	- 1, 2	200					ns min
Write/Reset Pulse Width	t_{WR}	- 1, 2	200					ns min
Chip Select/Load DAC to Write Setup Time	t_{CS}	- 1, 2	0					ns min
Chip Select/Load DAC to Write HoldTime	t_{CH}	- 1, 2	0					ns min
Data Valid to Write Setup Time	t_{DS}	- 1, 2	100					ns min
Data Valid to Write Hold Time	t_{DH}	- 1, 2	10					ns min
Power Supply Voltage Range	V_{DD}	- 1, 2	11.4				For Specified Performance	+ V min
			16.5					+ V max
	V_S	- 1, 2	4.5				For Specified Performance	- V min
			5.5					- V max
Power Supply Current	I_{DD}	- 1, 2	6	4	6		Output Unloaded: $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 16.5V; V_{SS} = -5.5V; V_{REF} = 12.5V$	mA max
	I_{SS}	- 1, 2	5	3	5			

NOTE: DUAL SUPPLY OPERATION

¹ $V_{DD} = +11.4V$ to $16.5V; V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$ unless otherwise stated.

² $V_{REF} = +10V$; settling time to $\pm 1/2LSB$.

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	R _{ES}	- 1, 2	8					Bits
Total Unadjusted Error	E _T	- 1, 2	2	2	2		V _{DD} = + 14V	± LSB max
Differential Nonlinearity	DNL	- 1, 2	1	1	1		V _{DD} = + 14V; Guaranteed Monotonic to 8-Bits	± LSB max
Voltage Output Settling Time ²	t _{SL}	- 1, 2	5				Positive Full-Scale Change	μs max
			20				Negative Full-Scale Change	
Voltage Output Slew Rate	t _{SR}	- 1, 2	2					V/μs min
Minimum Load Resistance	R _{L-MIN}	- 1, 2	2	2	2		V _{OUT} = + 10V; V _{DD} = + 15V	kΩ min
Reference Input Resistance	R _I	- 1, 2	8				V _{DD} = 14.25V	kΩ min
Reference Input Capacitance	C _I	- 1, 2	100				Occurs When DAC Is Loaded with All 1's	pF max
Digital Input High Voltage	V _{IH}	- 1, 2	2.4	2.4	2.4		V _{DD} = 14.25V	V min
Digital Input Low Voltage	V _{IL}	- 1, 2	0.8	0.8	0.8		V _{DD} = 14.25V	V max
Digital Input Leakage Current	I _{IN}	- 1, 2	1				V _{IN} = 0V or V _{DD} ; V _{DD} = 14.25V	± μA max
Digital Input Capacitance	C _I	- 1, 2	8					pF max
Chip Select/Load DAC Pulse Width	t _{LD}	- 1, 2	200					ns min
Write/Reset Pulse Width	t _{WR}	- 1, 2	200					ns min
Chip Select/Load DAC to Write Setup Time	t _{CS}	- 1, 2	0					ns min
Chip Select/Load DAC to Write Hold Time	t _{CH}	- 1, 2	0					ns min
Data Valid to Write Setup Time	t _{DS}	- 1, 2	100					ns min
Data Valid to Write Hold Time	t _{DH}	- 1, 2	10					ns min
Power Supply Voltage Range	V _{DD}	- 1, 2	14.25				For Specified Performance	+ V min
			15.75					+ V max
Power Supply Current	I _{DD}	- 1, 2	6				Outputs Unloaded; V _{IN} = V _{IL} or V _{IH} V _{DD} = 15.75V	mA max

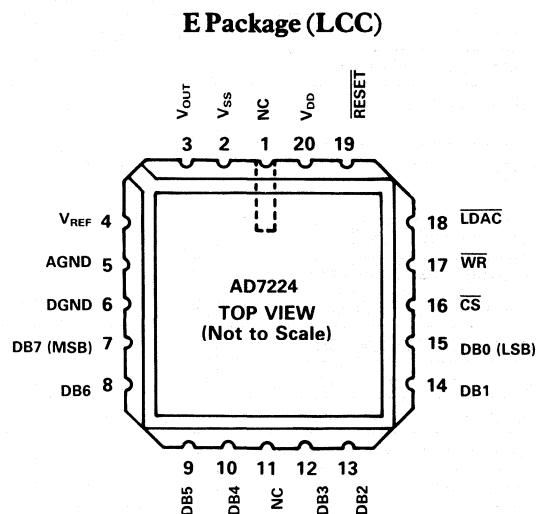
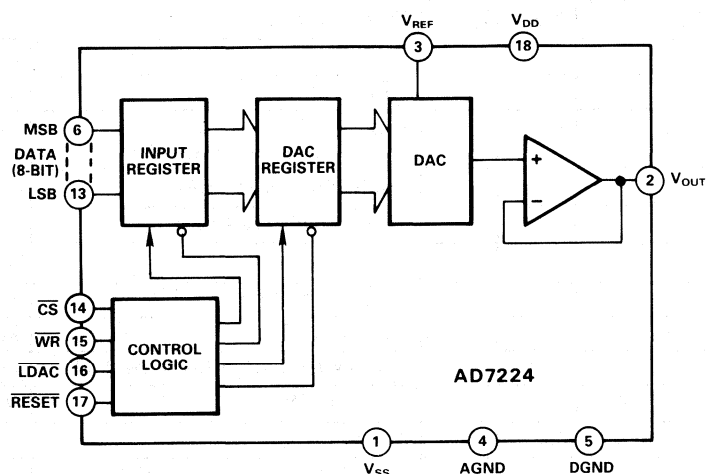
NOTE: SINGLE SUPPLY OPERATION

¹V_{DD} = + 15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} = + 10V unless otherwise stated.²Settling time to ± 1/2LSB.

Table 2.

AD7224

3.2.1 Functional Block Diagram and Terminal Assignments.

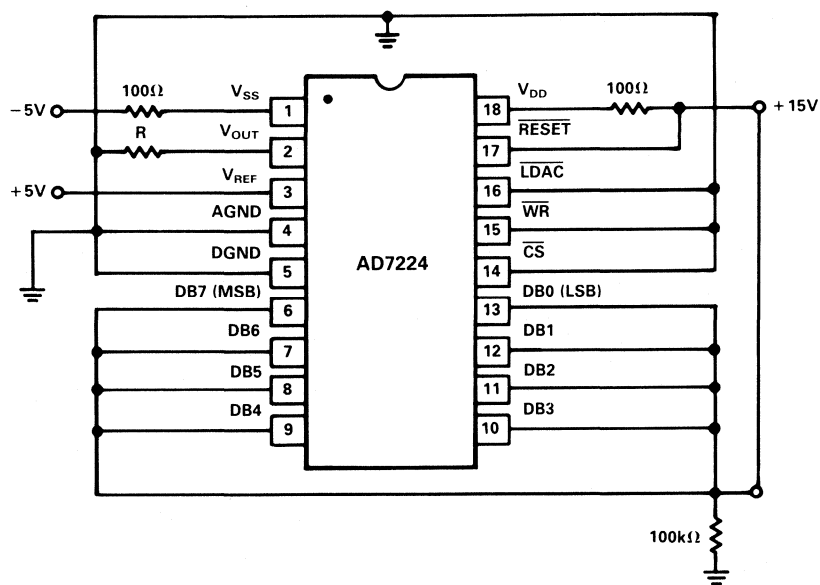


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE:
V_{DD} IS TURNED ON FIRST, THEN V_{SS}
FOLLOWED BY V_{REF}.

RESET	LDAC	WR	CS	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H		L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L		H	DAC Register Latched
L	X	X	X	Both Registers Loaded With All Zeros
	H	H	H	Both Register Latched With All Zeros and Output Remains at Zero
	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care

Table 3. AD7224 Truth Table

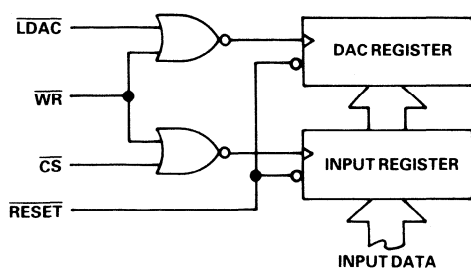
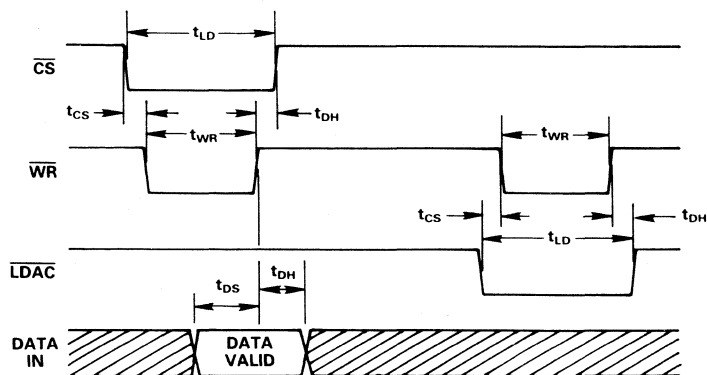


Figure 1. Input Control Logic



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} .
 $t_r = t_f = 20\text{ns}$ OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS

$$\frac{V_{INH} + V_{INL}}{2}$$

Figure 2. Write Cycle Timing Diagram

1.1 Scope.

This specification covers the detail requirements of a monolithic quad, 8-bit, voltage output, digital-to-analog converter with output buffer amplifiers and double-buffered interface logic on-chip. Each D/A converter has a separate reference input terminal.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number ¹
– 1	AD7225T(X)/883B
– 2	AD7225U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to AGND	–0.3V, +17V
V_{DD} to DGND	–0.3V, +17V
V_{DD} to V_{SS}	–0.3V, +24V
AGND to DGND	–0.3V, V_{DD}
Digital Input Voltage to DGND	–0.3V, V_{DD}
V_{REF} to AGND	–0.3V, V_{DD}
V_{OUT} to AGND	V_{SS} , V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	500mW
Derates above $+75^\circ\text{C}$	2mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-24 and E-28A
 $\theta_{JA} = 125^\circ\text{C/W}$ for Q-24 and E-28A

AD7225 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	8					Bits
Total Unadjusted Error	E_T	– 1	2	2	2		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$	$\pm$ LSB max
		– 2	1	2	1	1		
Relative Accuracy	RA	– 1	1	1	1		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$	$\pm$ LSB max
		– 2	0.5	1	0.5	0.5		
Differential Nonlinearity	DNL	– 1, 2	1	1	1		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ Guaranteed Monotonic to 8-Bits	$\pm$ LSB max
Full Scale Error	A_E	– 1	1	1	1		$V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$	$\pm$ LSB max
		– 2	0.5	1	0.5	0.5		
Zero Code Error		– 1	30	25	30		$V_{DD} = 16.5V; 11.4V$ and $14V$	$\pm$ mV max
		– 2	20	25	20	15	$V_{SS} = -5V; V_{REF} = V_{DD} - 4$	
Voltage Output Settling Time	t_{SL}	– 1, 2	5				$V_{REF} = +10V$; Settling Time to $\pm 1/2$ LSB	μ s max
Voltage Output Slew Rate	t_{SR}	– 1, 2	2.5					V/ μ s min
Minimum Load Resistance	$R_{L,MIN}$	– 1, 2	2				$V_{OUT} = +10V; V_{DD} = +14V$	k Ω min
Reference Input Resistance	R_{IN}	– 1, 2	11	11	11		$V_{DD} = 14V$	k Ω min
Reference Input Capacitance	C_{IN}	– 1, 2	100				Occurs when each DAC is loaded with all 1's	pF max
Channel-to-Channel Isolation		– 1, 2	60				$V_{REF} = +10V$ p-p Sinewave (ω 10kHz)	dB min
AC Feedthrough		– 1, 2	70				$V_{REF} = -10V$ p-p Sinewave (ω 10kHz)	– dB max
Digital Input High Voltage	V_{IH}	– 1, 2	2.4	2.4	2.4		$V_{DD} = +14V$	V min
Digital Input Low Voltage	V_{IL}	– 1, 2	0.8	0.8	0.8		$V_{DD} = +14V$ and $11.4V$	V max
Digital Input Leakage Current	I_{IN}	– 1, 2	1	1	1		$V_{IN} = 0V$ or V_{DD} ; $V_{DD} = 16.5V$	$\pm$ μ A max
Digital Input Capacitance	C_{IN}	– 1, 2	8					pF max
Write Pulse Width, t_1	t_{WR}	– 1, 2	150					ns min
Address to Write Setup Time, t_2	t_{AS}	– 1, 2	0					ns min
Address to Write Hold Time, t_3	t_{AH}	– 1, 2	0					ns min
Data Valid to Write Setup Time, t_4	t_{DS}	– 1, 2	90					ns min
Data Valid to Write Hold Time, t_5	t_{DH}	– 1, 2	10					ns min
Load DAC Pulse Width, t_6	$t_{L,DAC}$	– 1, 2	150					ns min
Power Supply Current	I_{DD}	– 1, 2	12	12	12		Outputs Unloaded, $V_{IN} = V_{IL}$ or V_{IH}	mA max
	I_{SS}	– 1, 2	10	10	10		$V_{DD} = 16.5V; V_{SS} = -5.5V; V_{REF} = 12.5V$	

NOTE: DUAL SUPPLY OPERATION

¹ $V_{DD} = +11.4V$ to $16.5V$; $V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$ unless otherwise stated.

Table 1.

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	8					Bits
Total Unadjusted Error	E_T	-1	2	2	2		$V_{DD} = +14V$	$\pm$ LSB max
		-2	1	2	1	1		
Differential Nonlinearity	DNL	-1, 2	1	1	1		$V_{DD} = +14V$ Guaranteed Monotonic to 8-Bits	$\pm$ LSB max
Voltage Output Settling Time Positive Full Scale Change		-1, 2	5				Settling Time to $\pm 1/2$ LSB	μs max
Negative Full Scale Change			7					
Voltage Output Slew Rate	t_{SR}	-1, 2	2.0					V/ μs min
Minimum Load Resistance	R_{LMIN}	-1, 2	2				$V_{OUT} = +10V; V_{DD} = +15V$	k Ω min
Reference Input Resistance	R_{IN}	-1, 2	11				$V_{DD} = 14V$	k Ω min
Reference Input Capacitance	C_{IN}	-1, 2	100				Occurs when each DAC is loaded with all 1's	pF max
Channel-to-Channel Isolation		-1, 2	60				$V_{REF} = +10V$ p-p Sinewave @ 10kHz	dB min
AC Feedthrough		-1, 2	70				$V_{REF} = -10V$ p-p Sinewave @ 10kHz	- dB max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2	1				$V_{IN} = 0V$ or V_{DD} ; $V_{DD} = 16.5V$	$\pm \mu A$ max
Digital Input Capacitance	C_{IN}	-1, 2	8					pF max
Write Pulse Width, t_1	t_{WR}	-1, 2	150					ns min
Address to Write Setup Time, t_2	t_{AS}	-1, 2	0					ns min
Address to Write Hold Time, t_3	t_{AH}	-1, 2	0					ns min
Data Valid to Write Setup Time, t_4	t_{DS}	-1, 2	90					ns min
Data Valid to Write Hold Time, t_5	t_{DH}	-1, 2	10					ns min
Load DAC Pulse Width, t_6	t_{LDAC}	-1, 2	150					ns min
Power Supply Current	I_{DD}	-1, 2	12				Outputs Unloaded, $V_{IN} = V_{IL}$ or V_{IH}	mA max

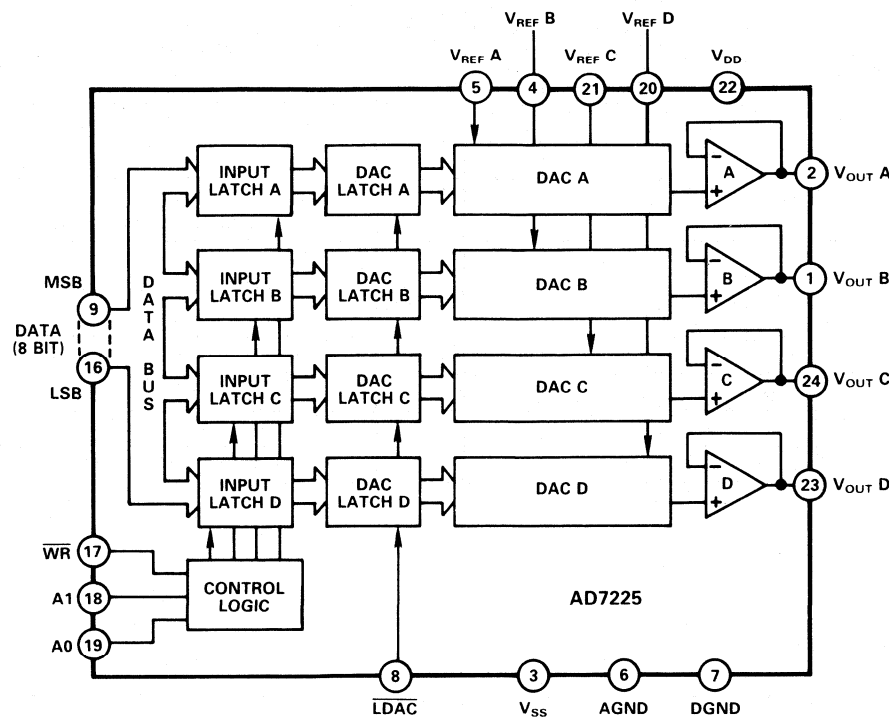
NOTE: SINGLE SUPPLY OPERATION

¹ $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$ unless otherwise stated.

Table 2.

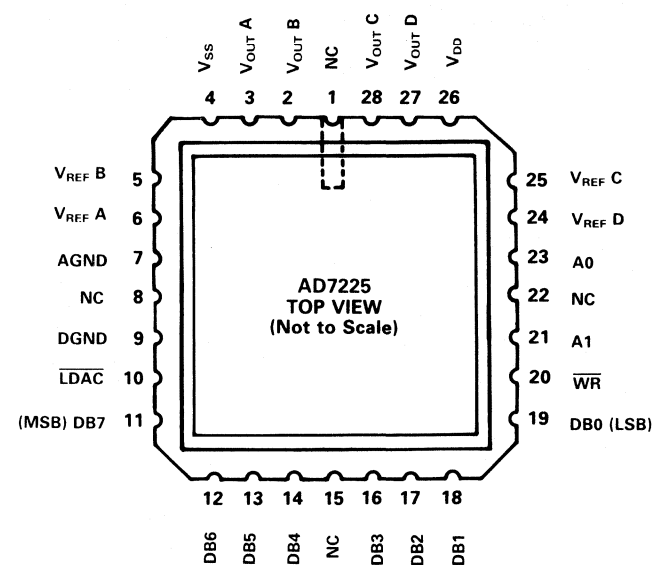
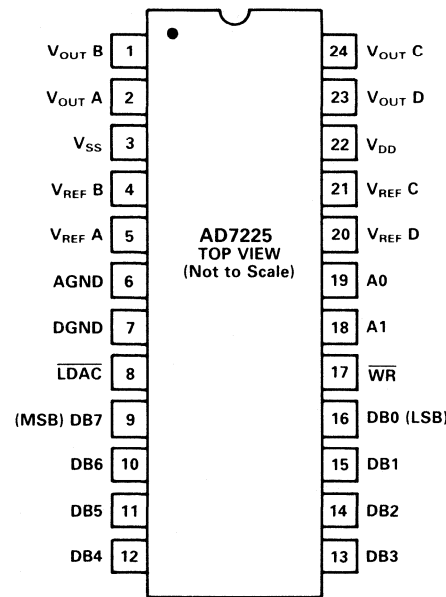
AD7225

3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)

E Package (LCC)

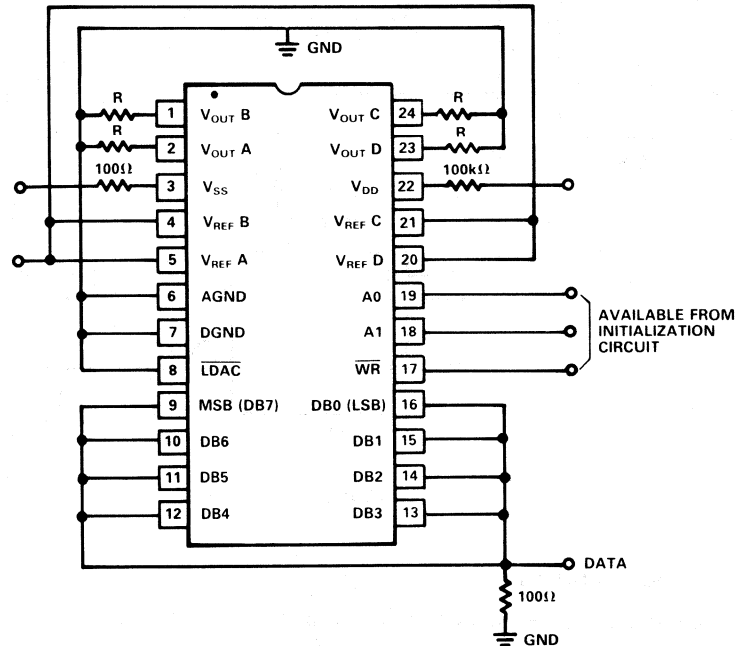


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



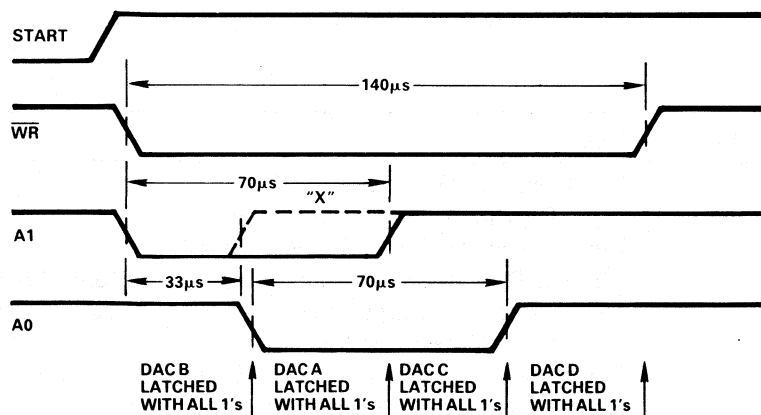
$V_{DD} = +15V$
 $V_{SS} = -5V$
 $V_{REF} = +10V$
 $DATA = V_{DD}$
 $R = 10k\Omega$
 $I_{DD} = 7mA$
 $I_{SS} = -5mA$
 $I_{REF} = 1mA$

INITIALIZATION PROCEDURE:

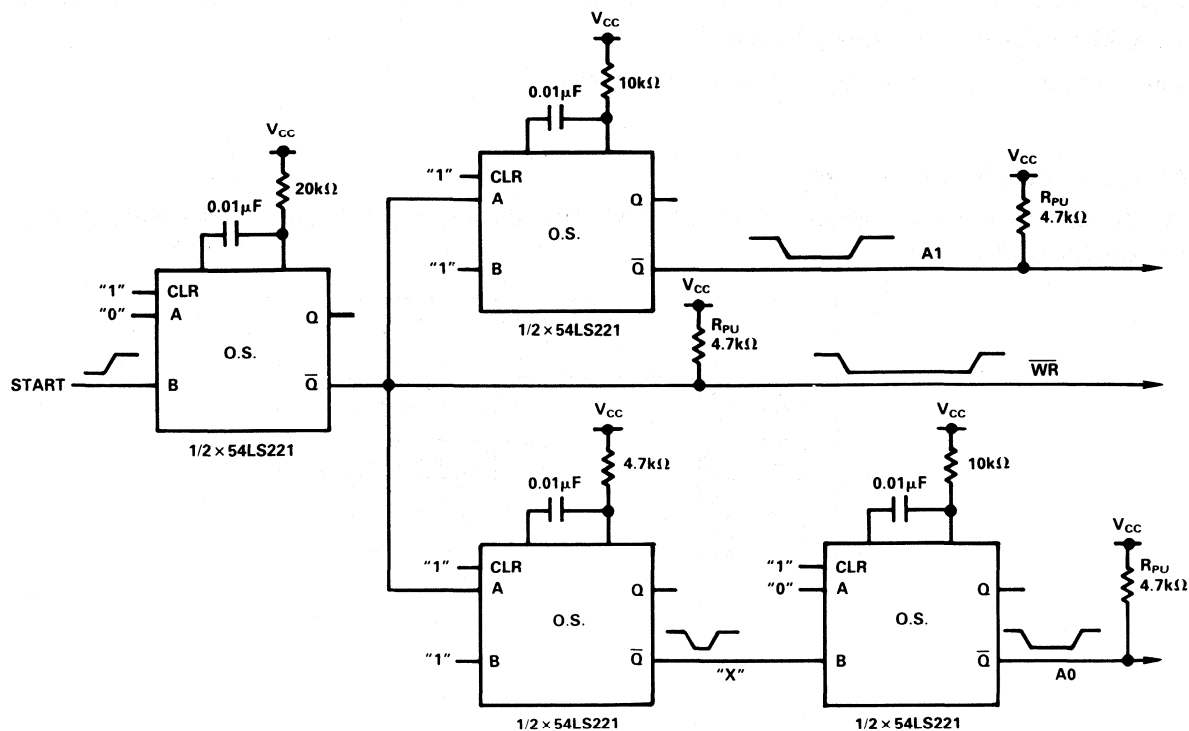
V_{DD} is turned on first, then V_{SS} , followed by V_{REF} . The V_{CC} of the initialization circuit is turned on. The START line is taken from "low" to "high", whereupon WR goes "low" for 140 μs . During this time, A0 and A1 go through the following states:

A1	A0	DAC ADDRESSED
GND	V_{CC}	DAC B
GND	GND	DAC A
V_{CC}	GND	DAC C
V_{CC}	V_{CC}	DAC D

Thus, all four DAC's are loaded with all 1's.



Timing Diagram and Initialization Circuit



Initialization Circuit

5.0 Interface Logic Information.

The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the input port. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table 3 shows the addressing for the input registers on the AD7225.

A1	A0	Selected Input Register
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table 3. AD7225 Addressing

$\overline{WR}$	$\overline{LDAC}$	Function
H	H	No Operation. Device Not Selected
L	H	Input Register of Selected DAC Transparent
	H	Input Register of Selected DAC Latched
H	L	All Four DAC Registers Transparent (i.e., Outputs Respond to Data Held in Respective Input Registers). Input Registers are Latched
H		All Four DAC Registers Latched
L	L	DAC Registers and Selected Input Register Transparent
	L	Output follows Input Data for Selected Channel

Table 4. AD7225 Truth Table

Only the data held in the DAC register determines the analog output of the converter. The $\overline{\text{LDAC}}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ signal is level triggered and therefore the DAC registers may be made transparent by tying $\overline{\text{LDAC}}$ LOW (in this case the outputs of the converters will respond to the data held in their respective input latches). $\overline{\text{LDAC}}$ is an asynchronous signal and is independent of $\overline{\text{WR}}$. This is useful in many applications. However, in systems where the asynchronous $\overline{\text{LDAC}}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{\text{LDAC}}$ is activated prior to the rising edge of $\overline{\text{WR}}$ (or $\overline{\text{WR}}$ occurs during $\overline{\text{LDAC}}$), then $\overline{\text{LDAC}}$ must stay LOW for t_6 or longer after $\overline{\text{WR}}$ goes HIGH to ensure correct data is latched through to the output. Table 4 shows the truth table for AD7225 operation. Figure 1 shows the input control logic for the part and the write cycle timing diagram is given in Figure 2.

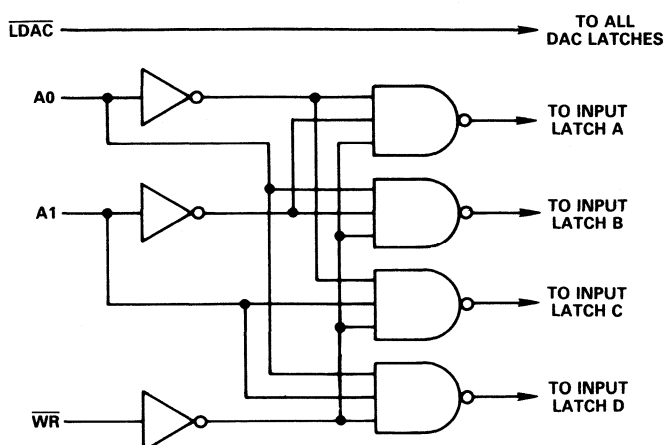


Figure 1. Input Control Logic

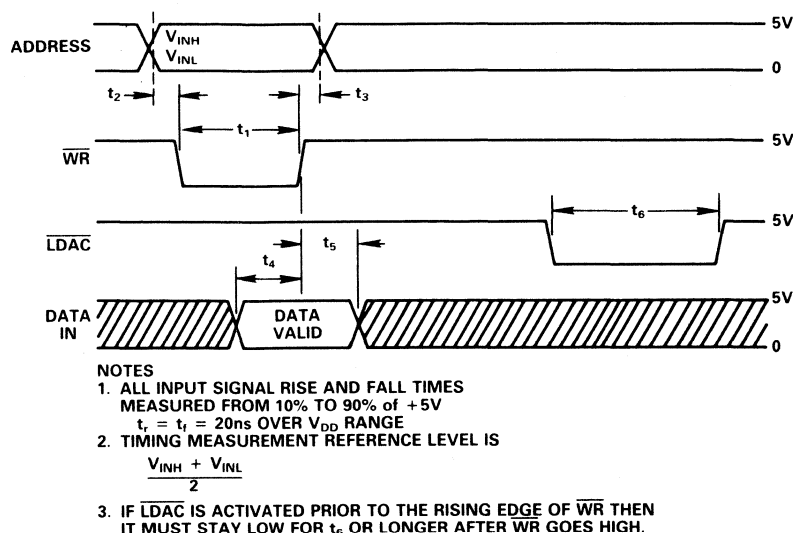


Figure 2. Write Cycle Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS Quad 8-bit digital-to-analog converter, with output buffer amplifiers and interface logic. Separate on-chip latches are provided for each of the four D/A converters.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
– 1	AD7226T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to AGND	–0.3V, +17V
V_{DD} to DGND	–0.3V, +17V
V_{SS} to AGND	–7V, V_{DD}
V_{SS} to DGND	–7V, V_{DD}
V_{DD} to V_{SS}	–0.3V, +24V
AGND to DGND	–0.3V, V_{DD}
Digital Input Voltage to DGND	–0.3V, V_{DD}
V_{REF} to AGND	–0.3V, V_{DD}
V_{OUT} to AGND	V_{SS} , V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	500mW
Derates above $+75^\circ\text{C}$	2mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-20 and E-20A

AD7226 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Resolution	RES	– 1	8				Bits
Relative Accuracy	RA	– 1	± 1	± 1	± 1	$V_{DD} = +14V$; $V_{SS} = -5V$; $V_{REF} = +10V$	LSB max
Total Unadjusted Error	E_T	– 1	± 2	± 2	± 2	$V_{DD} = +14V$; $V_{SS} = -5V$; $V_{REF} = +10V$	LSB max
Differential Nonlinearity	DNL	– 1	± 1	± 1	± 1	$V_{DD} = +14V$; $V_{SS} = -5V$; $V_{REF} = +10V$ Guaranteed Monotonic to 8-Bits	LSB max
Full-Scale Error	A_E	– 1	$\pm 3/2$	$\pm 3/2$	$\pm 3/2$	$V_{DD} = +14V$; $V_{SS} = -5V$; $V_{REF} = +10V$	LSB max
Zero Code Error	A_{ZCE}	– 1	± 30	± 30	± 30	$V_{DD} = 16.5V, 11.4V$ and $14V$; $V_{SS} = -5V$; $V_{REF} = V_{DD} - 4$	mV max
Voltage Output Settling Time ²	t_{SL}	– 1	5			Positive Full-Scale Change	μs max
			7			Negative Full-Scale Change	
Voltage Output Slew Rate	t_{SR}	– 1	2.5				V/ μs min
Minimum Load Resistance	$R_{L_{MIN}}$	– 1	2	2	2	$V_{OUT} = +10V$; $V_{DD} = +14V$	k Ω min
Reference Input Resistance	R_I	– 1	2	2	2	$V_{DD} = 14V$	k Ω min
Reference Input Capacitance	C_I	– 1	65			Occurs when DAC is loaded with all 0's	pF min
			300			Occurs when DAC is loaded with all 1's	pF max
Digital Input High Voltage	V_{IH}	– 1	2.4	2.4	2.4	$V_{DD} = 11.4V$; $V_{REF} = V_{DD} - 4$	V min
Digital Input Low Voltage	V_{IL}	– 1	0.8	0.8	0.8	$V_{DD} = 11.4V$; $V_{REF} = V_{DD} - 4$	V max
Digital Input Leakage Current	I_{IN}	– 1	1	1	1	$V_{IN} = 0V$ or V_{DD} ; $V_{DD} = 16.5V$	$\pm \mu A$ max
Digital Input Capacitance	C_{IN}	– 1	8				pF max
Address to Write Setup Time	t_{AS}	– 1	0				ns min
Address to Write Hold Time	t_{AH}	– 1	10				ns min
Data Valid to Write Setup Time	t_{DS}	– 1	100				ns min
Data Valid to Write Hold Time	t_{DH}	– 1	10				ns min
Write Pulse Width	t_{WR}	– 1	200				ns min
Power Supply Voltage Range	V_{DD}	– 1	11.4			For Specified Performance	+ V min
			16.5				+ V max
	V_S	– 1	– 4.5				– V min
			– 5.5				– V max
Power Supply Current	I_{DD}	– 1	13	13	13	Outputs Unloaded: $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 16.5V$; $V_{SS} = -5.5V$; $V_{REF} = 12.5V$	mA max
	I_{SS}	– 1	11	11	11		

NOTES

¹ $V_{DD} = +11.4V$ to $16.5V$; $V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$ unless otherwise stated.

² $V_{REF} = +10V$; Settling Time to $\pm 1/2$ LSB.

Table I.

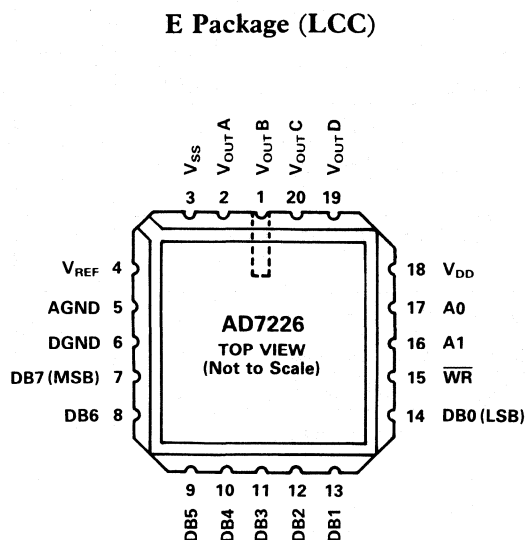
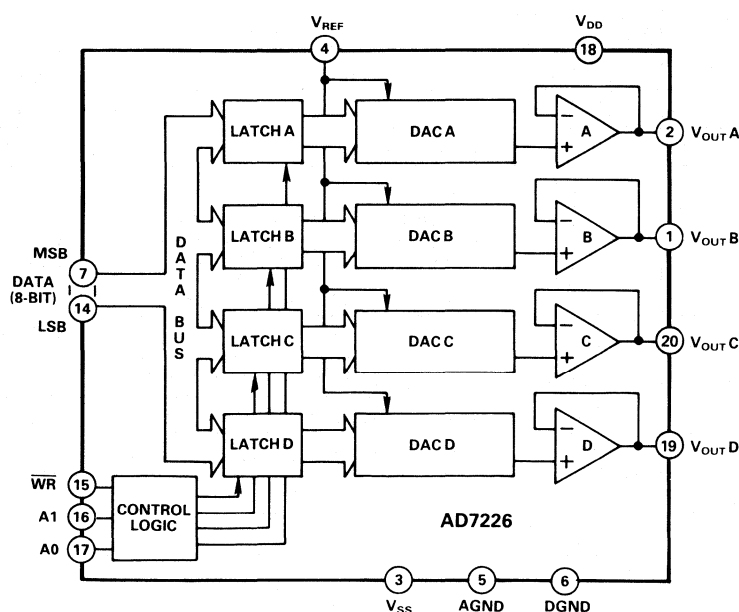
Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Resolution	RES	-1	8				Bits
Total Unadjusted Error	E_T	-1	2	2	2	$V_{DD} = +14V$	$\pm$ LSB max
Differential Nonlinearity	DNL	-1	1	1	1	$V_{DD} = +14V$ Guaranteed Monotonic to 8-Bits	$\pm$ LSB max
Voltage Output Settling Time ²	t_{SL}	-1	5			Positive Full-Scale Change	μs max
			20			Negative Full-Scale Change	
Voltage Output Slew Rate	t_{SR}	-1	2				V/ μs min
Minimum Load Resistance	$R_{L_{MIN}}$	-1	2	2	2	$V_{OUT} = +10V$; $V_{DD} = +15V$	k Ω min
Reference Input Resistance	V_{REF}	-1	2			$V_{DD} = 14.25V$	k Ω min
Reference Input Capacitance	C_I	-1	65			Occurs when DAC is loaded with all 0's	pF min
			300			Occurs when DAC is loaded with all 1's	pF max
Digital Input High Voltage	V_{IH}	-1	2.4	2.4	2.4	$V_{DD} = +14.25V$	V min
Digital Input Low Voltage	V_{IL}	-1	0.8	0.8	0.8	$V_{DD} = +14.25V$	V max
Digital Input Leakage Current	I_{IN}	-1	1			$V_{IN} = 0V$ or V_{DD} ; $V_{DD} = +14.25V$	$\pm \mu A$ max
Digital Input Capacitance	C_I	-1	8				pF max
Address to Write Setup Time	t_{AS}	-1	0				ns min
Address to Write Hold Time	t_{AH}	-1	10				ns min
Data Valid to Write Setup Time	t_{DS}	-1	100				ns min
Data Valid to Write Hold Time	t_{DH}	-1	10				ns min
Write Pulse Width	t_{WR}	-1	200				ns min
Power Supply Voltage Range	V_{DD}	-1	14.25			For Specified Performance	+ V min
			15.75				+ V max
Power Supply Current	I_{DD}	-1	13			Outputs Unloaded; $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 15.75V$	mA max

NOTES

¹ $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Settling Time to $\pm 1/2LSB$.

Table 2.

3.2.1 Functional Block Diagram and Terminal Assignments.

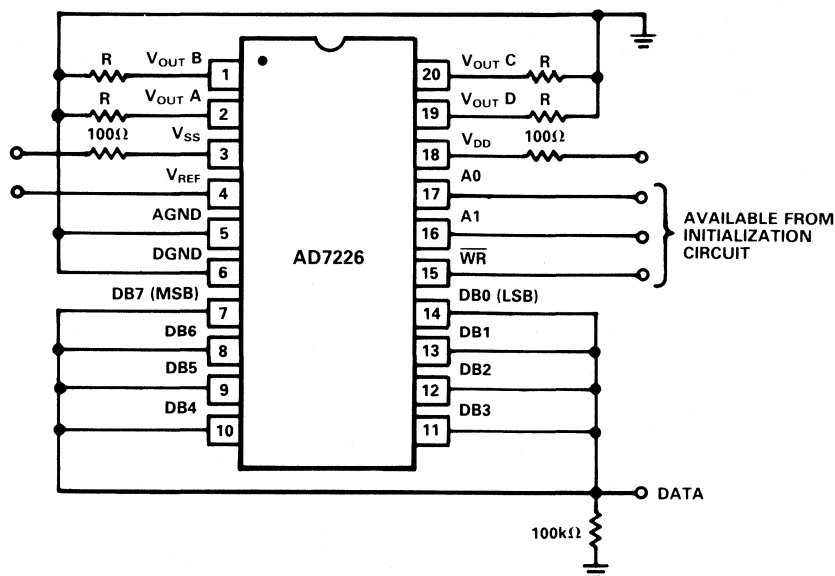


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

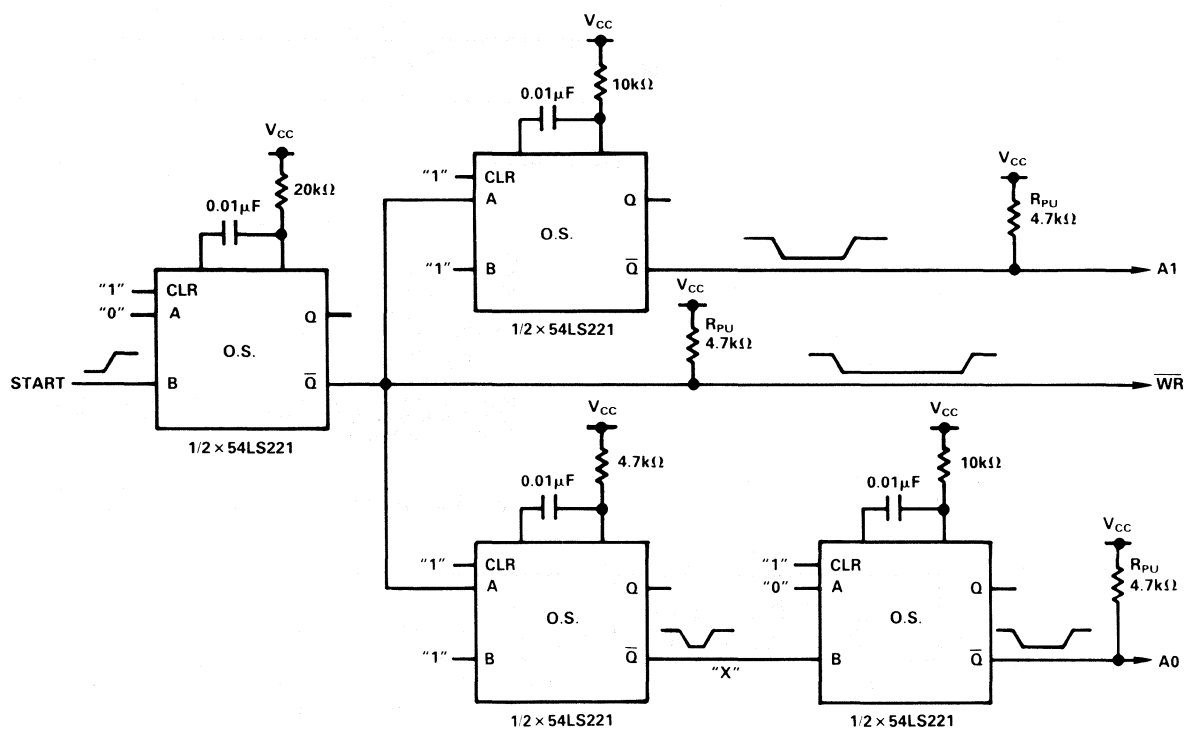


V_{DD}	=	+ 15V
V_{SS}	=	- 5V
V_{REF}	=	+ 5V
DATA	=	V_{DD}
R	=	10k Ω
I_{DD}	=	6.5mA
I_{SS}	=	- 5.0mA
I_{REF}	=	0.5mA

INITIALIZATION PROCEDURE: (SEE SHEET 3)
 V_{DD} IS TURNED ON FIRST, THEN V_{SS} , FOLLOWED BY V_{REF} .
 THE V_{CC} OF THE INITIALIZATION CIRCUIT IS TURNED ON.
 THE START LINE IS TAKEN FROM "LOW" TO "HIGH", WHERE-
 UPON WR GOES LOW FOR 140 μ S. DURING THIS TIME A0
 AND A1 GO THROUGH THE FOLLOWING STATES:

A1	A0	DAC ADDRESSED
GND	V_{CC}	DAC B
GND	GND	DAC A
V_{CC}	GND	DAC C
V_{CC}	V_{CC}	DAC D

THUS, ALL FOUR DAC'S ARE LOADED WITH ALL 1's.



AD7226

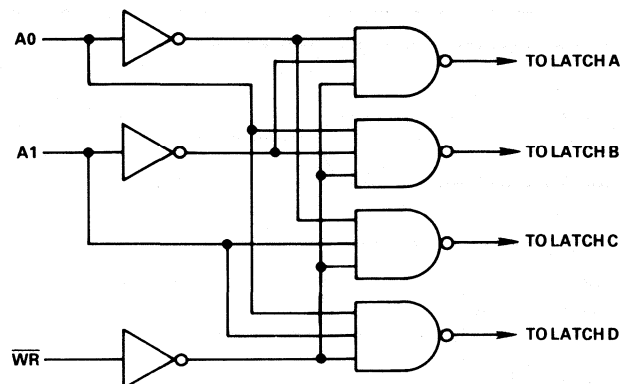
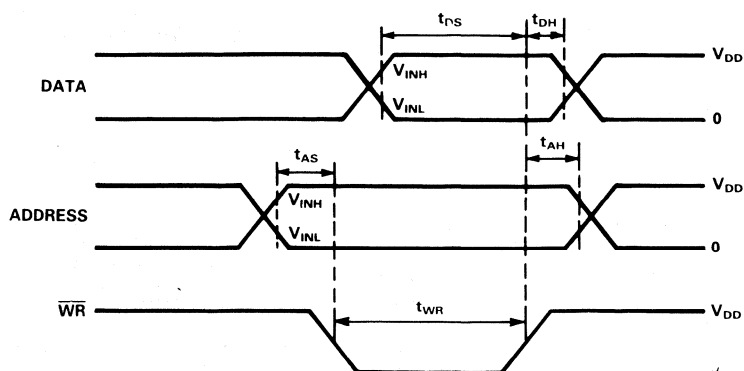


Figure 3. Input Control Logic



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} .
 $t_r = t_f = 20\text{ns}$ OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS
 $\frac{V_{INH} + V_{INL}}{2}$
3. SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS.

Figure 4. Write Cycle Timing Diagram

AD7226 Control Inputs			AD7226 Operation
$\overline{WR}$	A1	A0	
H	X	X	No Operation Device Not Selected
L	L	L	DACA Transparent
L	L	L	DACA Latched
L	L	H	DACB Transparent
L	L	H	DACB Latched
L	H	L	DACC Transparent
L	H	L	DACC Latched
L	H	H	DACD Transparent
L	H	H	DACD Latched

L = Low State, H = High State, X = Don't Care

Table 3. AD7226 Truth Table

REV A.

1.1 Scope.

This specification covers the detail requirements for an octal CMOS digital-to-analog converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7228T(X)/883B
-2	AD7228U(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3" Width
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND		-0.3 V to +17 V
V_{DD} to V_{SS}		+0.3 V to +24 V
Digital Input Voltage		-0.3 V, V_{DD}
V_{REF} to GND		-0.3 V, V_{DD}
V_{OUT} to GND ¹		V_{SS} , V_{DD}
Power Dissipation		
Up to $+75^\circ\text{C}$		1000 mW
Derates above $+75^\circ\text{C}$		2.0 mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Thermal Resistance (θ_{JC}):		
Case 1 (Q-24)		See MIL-M-38510, Appendix C
Case 3 (E-28A)		See MIL-M-38510, Appendix C
Storage Temperature		-65°C to $+125^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)		$+300^\circ\text{C}$
Junction Temperature		$+175^\circ\text{C}$

NOTE

¹Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit for a short to V_{SS} is 50 mA.

AD7228 – SPECIFICATIONS

Test	Symbol	Device	Design Min Max		Sub Group	Test Condition ¹	Units
Total Unadjusted Error ²	TUE	–1, 2	–2	+2	1	V _{DD} = 15 V ±10%, V _{REF} = +10 V (Single Supply Only)	LSB
		–1	–2	+2	2, 3		
		–2	–1	+1	2, 3		
		–2	–1	+1	4		
Total Unadjusted Error	TUE	–1	–2	+2	13, 14, 15	Dual Supply Only	LSB
		–2	–1	+1			
Relative Accuracy	RA	–1, 2	–1	+1	1		LSB
		–1	–1	+1	2, 3		
		–2	–0.5	+0.5	2, 3		
		–2	–0.5	+0.5	12		
Differential Nonlinearity	DNL	–1, 2	–1	+1	1, 2, 3	Guaranteed Monotonic (Single Supply Only)	LSB
Differential Nonlinearity	DNL	–1, 2	–1	+1	13, 14, 15	Dual Supply Only	LSB
Full-Scale Error ³	A _E	–1, 2	–1	+1	1		mV
		–1	–1	+1	2, 3		
		–2	–0.5	+0.5	2, 3		
		–2	–0.5	+0.5	12		
Zero Code Error	A _{ZCE}	–1, 2	–25	+25	1		mV
		–1	–30	+30	2, 3		
		–2	–20	+20	2, 3		
		–2	–15	+15	12		
Load Resistance	R _L	–1, 2	2		1, 2, 3	V _{OUT} = ±10 V (Dual Supply & Single Supply)	kΩ
Reference Input Voltage Range	V _{REF}	–1, 2	2	10	1, 2, 3		V
Reference Input Resistance	R _{IN}	–1, 2	2		1, 2, 3	Dual Supply Only	kΩ
Reference Input Capacitance ⁴	C _{IN} (REF)	–1, 2	500		13, 14, 15	Dual and Single Supply	pF
Digital Input High Voltage	V _{INH}	–1, 2	2.4		1, 2, 3	Dual Supply Only	V
Digital Input Low Voltage	V _{INL}	–1, 2	0.8		1, 2, 3	Input Coding Is Binary	V
Digital Input Leakage Current	I _{ILC}	–1, 2	–1	+1	1, 2, 3		μA
Digital Input Capacitance	C _{IN}	–1, 2	8		13, 14, 15		pF
Voltage Output Slew Rate	SR	–1, 2	2		13, 14, 15	Dual and Single Supply	V/μs
Voltage Output Settling Time ⁵ Positive Full-Scale Change	t _{SL}	–1, 2	5		13, 14, 15	Dual and Single Supply	μs
			5			Dual Supply	
			7			Single Supply	
Power Supply Current	I _{DD}	–1, 2	16 22		1 2, 3	Dual Supply Only	mA
	I _{SS}	–1, 2	14 20		1 2, 3		
Function Tests ⁶		–1, 2			7		
Address to $\overline{\text{WR}}$ Setup Time	t ₁	–1, 2	0		9, 10, 11	Dual and Single Supply See Figure 2 and Note 7	ns
Address to $\overline{\text{WR}}$ Hold Time	t ₂	–1, 2	0		9, 10, 11		
Data Valid to $\overline{\text{WR}}$ Setup Time	t ₃	–1, 2	70		9		
			100		10, 11		
Data Valid to $\overline{\text{WR}}$ Hold Time	t ₄	–1, 2	10		9, 10, 11		ns

Test	Symbol	Device	Design Min Max	Sub Group	Test Condition ¹	Units
Write Pulse Width	t_5	-1, 2	95	9		ns
			150	10, 11		

NOTES

¹ $-55^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$, Dual Supply unless otherwise specified. $R_L = 2\text{k}$, $C_L = 100\text{ pF}$ unless otherwise stated. Parameters in subgroups 13, 14, 15 are characterized at initial design and after any subsequent redesigns.

² Includes zero code error, relative accuracy and full-scale error.

³ Calculated after zero code error has been adjusted out.

⁴ Occurs when each DAC is loaded with all 1s.

⁵ $V_{\text{REF}} = +10\text{ V}$; settling time to $\pm 1/2\text{ LSB}$.

⁶ Subgroup 7 tests are for the purpose of verifying the truth table.

⁷ All input rise and fall times measured from 10% to 90% of $+5\text{ V}$, $t_R = t_F = 5\text{ ns}$.

Timing measurement reference level is $\frac{V_{\text{INH}} + V_{\text{INL}}}{2}$.

Table 1.

1.3.1 Recommended Operating Conditions.

Operating Voltage Range for Dual Supply

Positive Supply (V_{DD})	+10.8 V to +16.5 V
Negative Supply (V_{SS})	-4.5 V to -5.5 V
Reference Voltage (V_{REF}) ¹	+2.0 V to +10.0 V

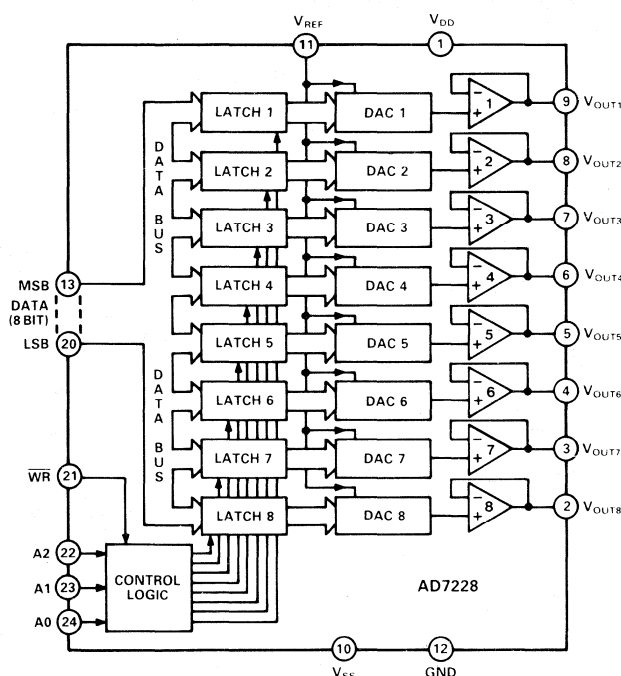
Operating Voltage Range for Single Supply

Positive Supply (V_{DD})	+13.5 V to +16.5 V
Negative Supply (V_{SS})	0 V
Reference Voltage (V_{REF}) ¹	+10 V

NOTE

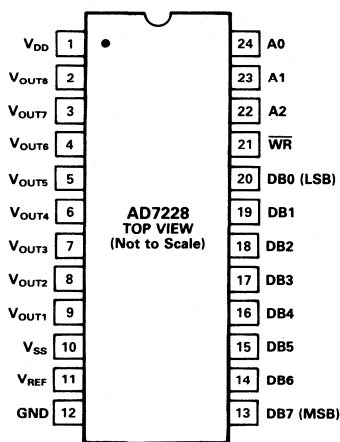
¹ V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.

3.2.1 Functional Block Diagram and Terminal Assignments.

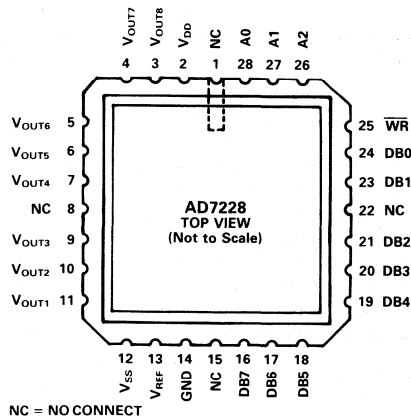


AD7228

Q Package (Cerdip)



E Package (LCC)



AD7228 Control Inputs

WR	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
L	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State L = Low State X = Don't Care

Table 2. Truth Table

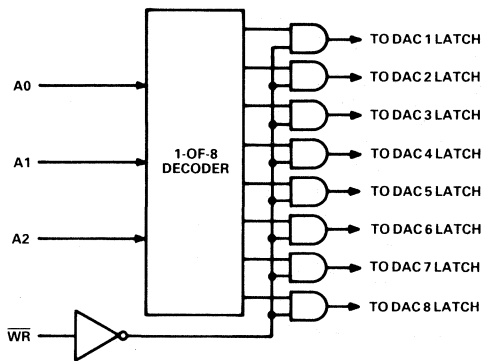
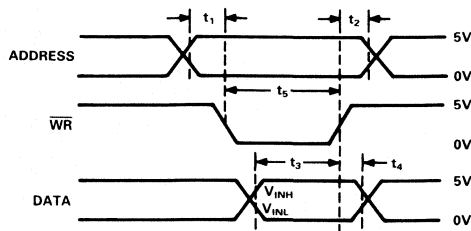


Figure 1. Input Control Logic



NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE WR IS LOW,
THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

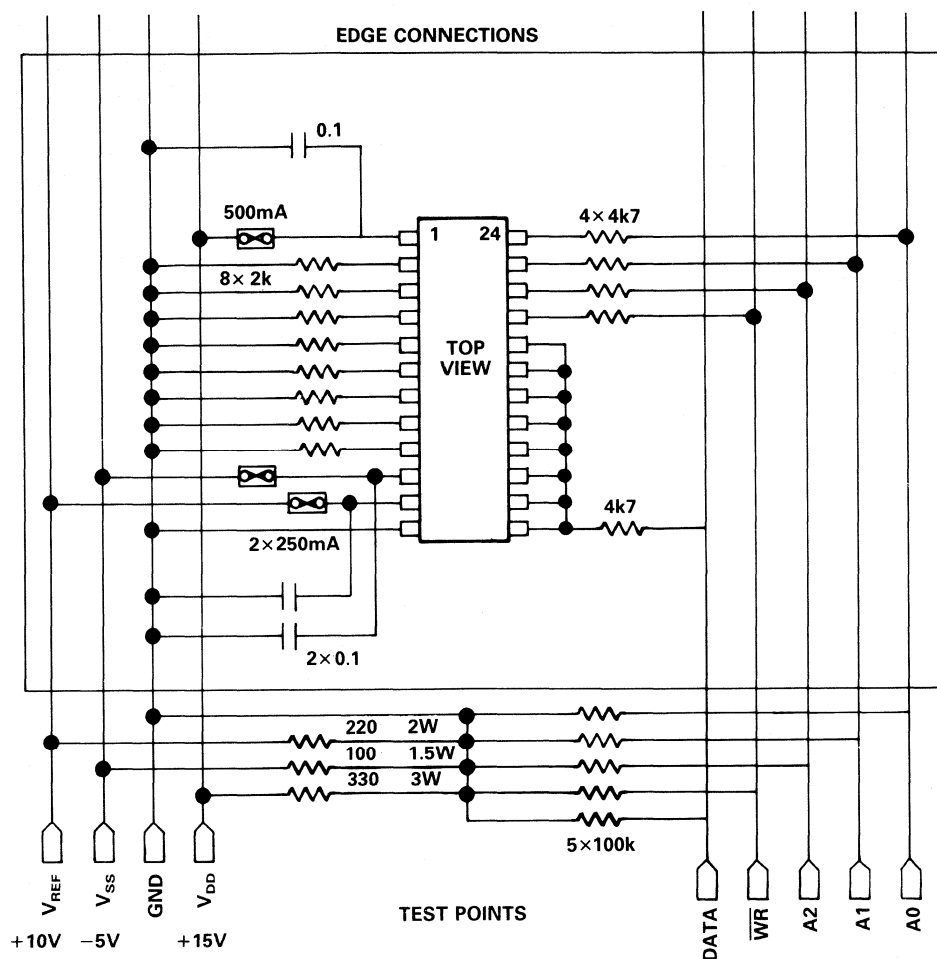
Figure 2. Write Cycle Timing Diagram

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

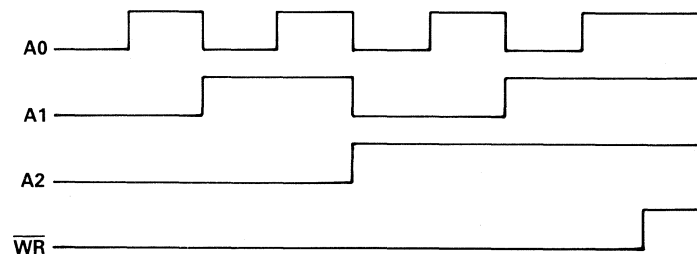
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



TO INITIALIZE, APPLY THE FOLLOWING WAVEFORMS:
EACH PULSE OF A0 SHOULD BE AT LEAST 50 μ s.

DATA = 15V



THIS SEQUENCE ENSURES ALL DACS ARE LOADED.

Burn-In Conditions

1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS dual 12-bit DACPORTs™, each consisting of two 12-bit DACs, output amplifiers and reference. The AD7237 has an (8+4) microprocessor loading structure, while the AD7247 has a parallel loading structure.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD7237TQ/883B, AD7247TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package Description

Q-24 24-Pin Cerdip, 0.3" Width

(For volume applications, the AD7237 and AD7247 are available in the LCC package. Contact your local Analog Devices Sales Office.)

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND (AD7247)	+0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237)	–0.3 V to +17 V
V_{DD} to V_{SS}	–0.3 V to +34 V
AGND to DGND (AD7237)	+0.3 V, $V_{DD} + 0.3$ V
V_{OUTA} , V_{OUTB} to AGND (GND)	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
REFOUT ¹ to AGND (GND)	0 V to V_{DD}
REFIN to AGND (GND)	–0.3 V to $V_{DD} + 0.3$ V
Digital Inputs to DGND (GND)	–0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation (Any Package) to +75°C	1000 mW
Derates above +75°C by	10 mW/°C

NOTE

¹The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

AD7237/AD7247 – SPECIFICATIONS

Test	Symbol	Device	Limits Min Max		Sub Groups	Test Condition ¹	Unit
Resolution	RES	–1		12	1, 2, 3		Bits
Relative Accuracy	RA	–1	–0.5	+0.5	1, 2, 3		LSB
Differential Nonlinearity	DNL	–1	–0.9	+0.9	1, 2, 3	Guaranteed Monotonic	LSB
Unipolar Offset Error	OFS	–1	–3	+3	1, 2, 3	V _{SS} = 0 V or –15 V. DAC Latch Contents All Zeroes	LSB
Bipolar Zero Error	Z _E	–1	–4	+4	1, 2, 3	V _{SS} = –15 V. DAC Latch Contents 1000 0000 0000	LSB
Full-Scale Error ²	A _E	–1	–5	+5	1, 2, 3		LSB
Reference Output	REF OUT	–1	4.95	5.05	1, 2, 3		V
Reference Load Change	ΔREF	–1		–1	1, 2, 3	ΔREFOUT vs. Δ I Reference Load Current Change (0–100 mA)	mV
Reference Input Range	REFIN	–1	4.75	5.25	1, 2, 3		V
Input Current	I _{IN}	–1	–5	+5	13, 14, 15		μA
Digital Input High Voltage	V _{INH}	–1	2.4		1, 2, 3		V
Digital Input Low Voltage	V _{INL}	–1		0.8	1, 2, 3		V
Digital Input Current ³	I _{IN}	–1	–10	+10	1, 2, 3	Data Inputs; V _{IN} = 0 V to V _{DD}	μA
	I _{INH}		–10	+10		Control Inputs; V _{IN} = V _{DD}	
	I _{INL}			–150		Control Inputs; V _{IN} = 0 V	
Input Capacitance	C _{IN}	–1		16	13, 14, 15		pF
Output Range Resistors		–1	15	30	1, 2, 3		kΩ
Output Voltage Ranges		–1	+5	+10	1, 2, 3	V _{SS} = 0 V; Pin Strappable	V
Output Voltage Ranges		–1	+5, +10, ±5		1, 2, 3	V _{SS} = –15 V; Pin Strappable	V
Voltage Output Settling Time Full-Scale Change	t _{SL}	–1		12	13, 14, 15	V _{DD} = +15 V, V _{SS} = –15 V Settling to ±1/2 LSB	μs
Power Supply Current	I _{DD}	–1		15	1, 2, 3	Outputs Unloaded	mA
	I _{SS}	–1		5	1, 2, 3	Outputs Unloaded (Dual Supplies)	mA
CS to WR Setup Time	t ₁	–1	0		9, 10, 11	See Note 4.	ns
CS to WR Hold Time	t ₂	–1	0		9, 10, 11		ns
WR Pulse Width	t ₃	–1	150		9, 10, 11		ns
Data Valid to Write Setup Time	t ₄	–1	150		9, 10, 11		ns
Data Valid to Write Hold Time	t ₅	–1	15		9, 10, 11		ns
Address to Write Setup Time	t ₆ ⁵	–1	0		9, 10, 11		ns
Address to Write Hold Time	t ₇ ⁵	–1	0		9, 10, 11		ns
LDAC Pulse Width	t ₈ ⁵	–1	100		9, 10, 11		ns

NOTES

¹V_{DD} = 15 V ± 15%, V_{SS} = 0 V or –15 V ± 5%; AGND = DGND = 0 V (AD7237), GND = 0 V (AD7247); R_L = 2 kΩ, C_L = 100 pF. Parts are functional at V_{DD} = +12 V and V_{SS} = 0 V or –12 V ± 5%. Subgroups 10, 11, 13, 14, 15 are characterized at initial design and after any design changes and are not production tested.

²Measured with respect to REFIN and includes unipolar/bipolar offset error.

³Control inputs are A0, A1, CS, WR and LDAC for the AD7237 and CSA, CSB and WR for the AD7247.

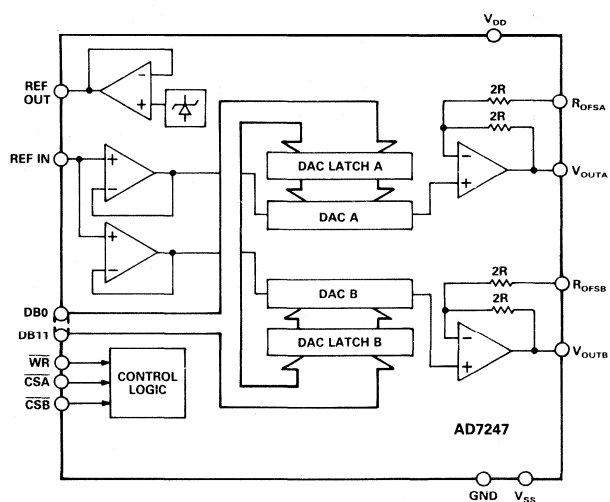
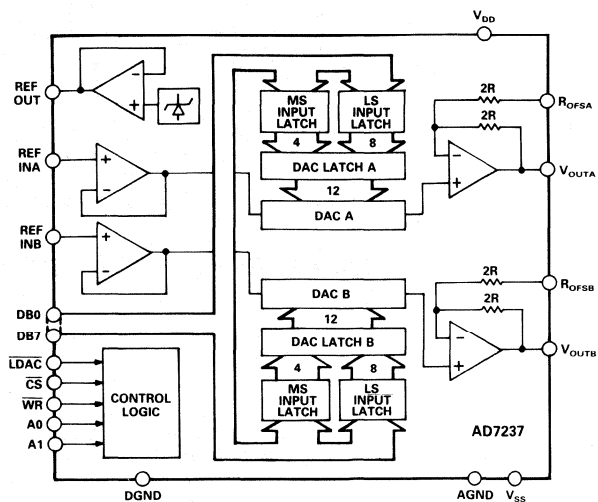
⁴All input signals are specified with t_r = t_f = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

⁵Applies to AD7237 only.

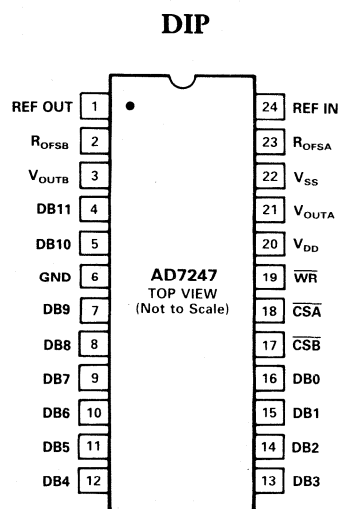
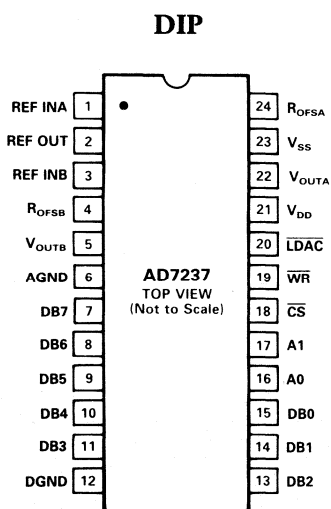
Table 1.

AD7237/AD7247

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments



AD7237/AD7247

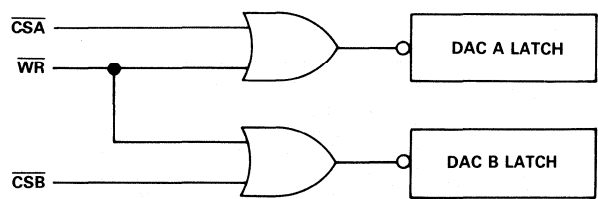


Figure 1. Input Control Logic AD7247

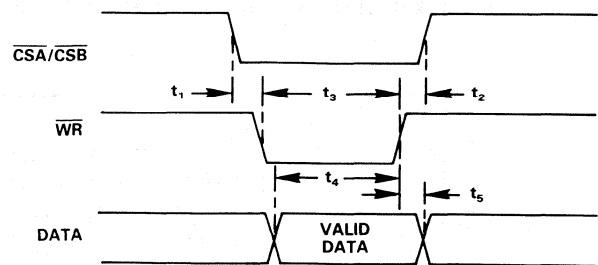


Figure 2. Timing Diagram AD7247

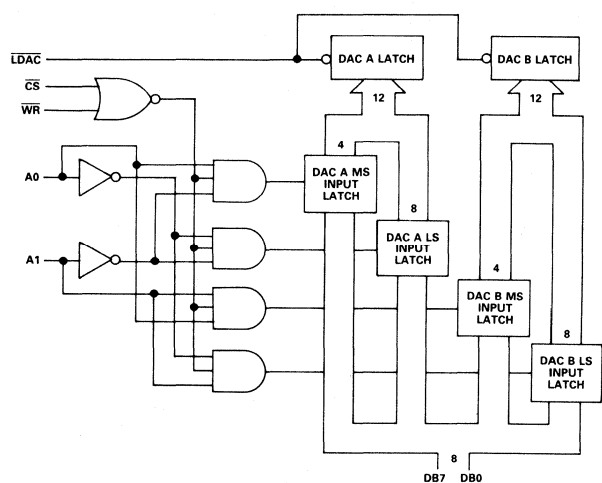


Figure 3. Input Control Logic AD7237

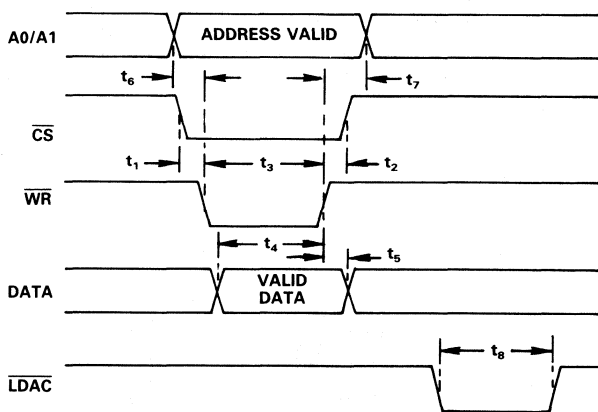


Figure 4. Timing Diagram AD7237

CSA	CSB	WR	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	0	DACA Latch Transparent
1	0	0	DACB Latch Transparent
0	0	0	Both DAC Latches Transparent

X=Don't Care

Table 2. AD7247 Truth Table

CS	WR	A1	A0	LDAC	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

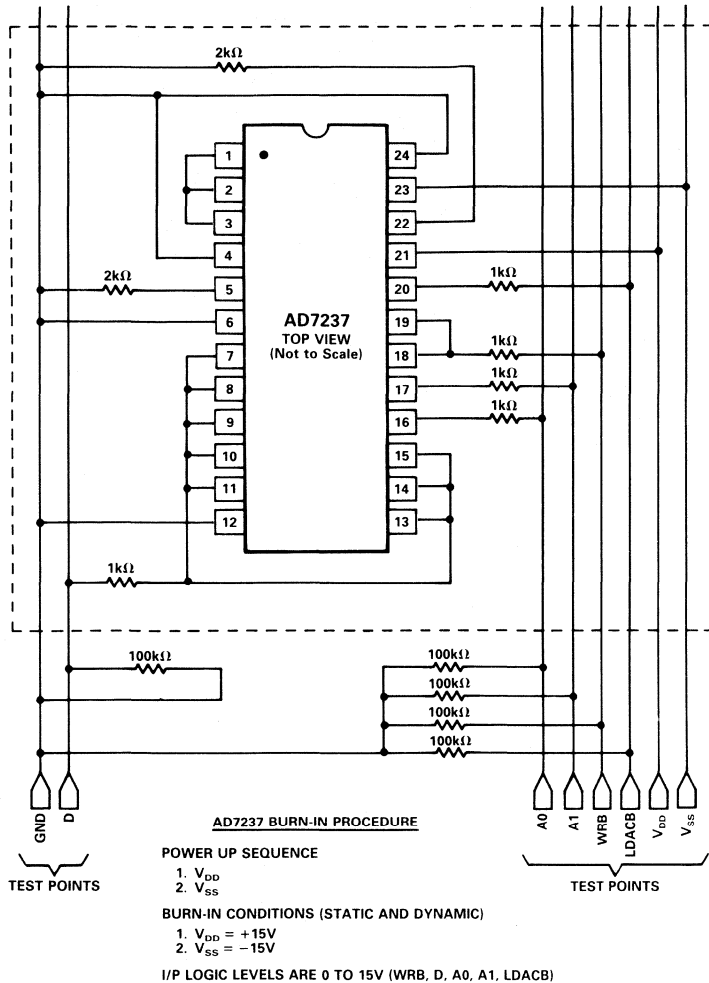
Table 3. AD7237 Truth Table

3.2.4 Microcircuit Technology Group.

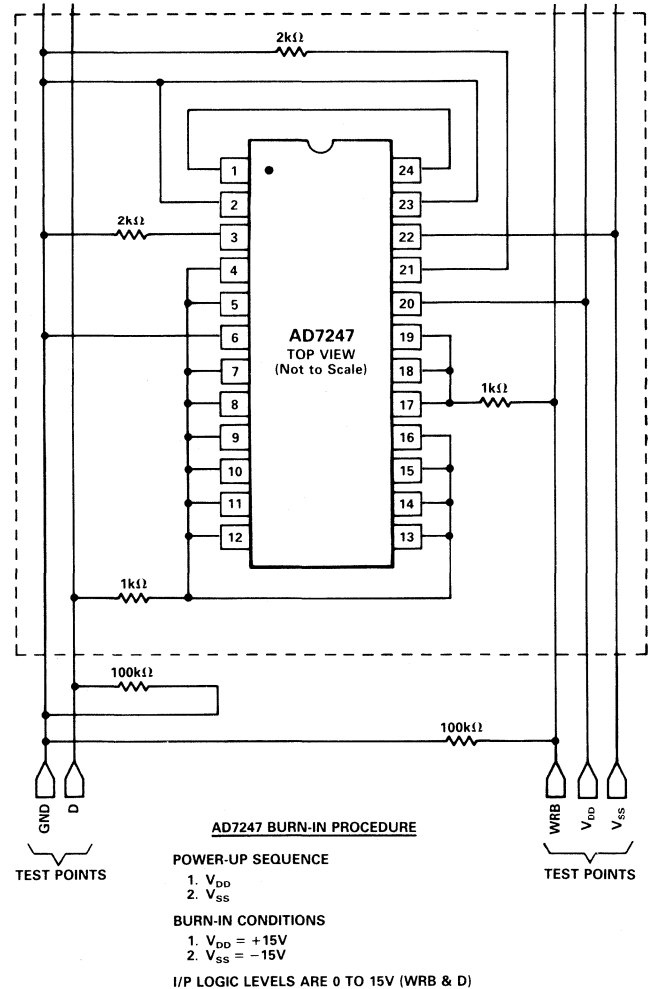
This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7237 Burn-In Diagram



AD7247 Burn-In Diagram

1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS DACPORTs™, each consisting of a 12-bit D/A converter, reference and output amplifier. The AD7245 has a parallel loading structure, while the AD7248 has an (8 + 4) loading structure.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number ¹
-1	AD7245S(X)/883B
-1	AD7248S(Y)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

Q	Q-24	24-Pin Cerdip, 0.3" Width
E	E-28A	28-Contact LCC

(Y) Package Description

Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V _{DD} to AGND		-0.3 V, +17 V
V _{DD} to DGND		-0.3 V, +17 V
V _{DD} to V _{SS}		-0.3 V, +34 V
AGND to DGND		-0.3 V, V _{DD}
Digital Input Voltage to DGND		-0.3 V, V _{DD} , +0.3 V
V _{OUT} to AGND ¹		V _{SS} , V _{DD}
V _{OUT} to V _{SS} ¹		0 V, +24 V
V _{OUT} to V _{DD} ¹		-32 V, 0 V
REF OUT ¹ to AGND		0 V, V _{DD}
Power Dissipation		
Up to +75°C		450 mW
Derates above +75°C by		6 mW/°C
Operating Temperature Range		-55°C to +125°C
Storage Temperature Range		-65°C to +125°C
Lead Temperature (Soldering 10 sec)		+300°C

NOTE

¹The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

AD7245/AD7248 – SPECIFICATIONS

Test	Symbol	Device	Limits Min Max		Sub Group	Test Condition ¹	Units
Resolution	RES	–1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	–1, 2	–1	+1	1, 2, 3	$V_{DD} = 11.4 \text{ V to } +14.25 \text{ V}$ $V_{SS} = 11.4 \text{ V to } -14.25 \text{ V}$	LSB
		–1, 2	–1.5	+1.5	13, 14, 15	$V_{DD} = 14.25 \text{ V to } +15.75 \text{ V}$ $V_{SS} = 14.25 \text{ V to } -15.75 \text{ V}$	
Differential Nonlinearity	DNL	–1, 2	–1	+1	1, 2, 3	Guaranteed Monotonic	LSB
Bipolar Offset Error	B _{POE}	–1, 2	–3 –5	+3 +5	1 2, 3		LSB
DAC Gain Error ²	GE	–1, 2	–2	+2	1, 2, 3		LSB
Full-Scale Output Voltage Error ³	V _{OUT} E	–1, 2	–0.2	+0.2	1	$V_{DD} = +12 \text{ V and } +15 \text{ V}$	% of FSR
			–0.6	+0.6	2, 3	$V_{SS} = -12 \text{ V and } -15 \text{ V}$	
Δ Full Scale/ Δ V _{DD}		–1, 2	–0.12	+0.12	1	$V_{DD} = \pm 5\%$	% of FSR/V
Δ Full Scale/ Δ V _{SS}		–1, 2	–0.1	+0.1	1	$V_{SS} = \pm 5\%$	% of FSR/V
Δ Offset/ Δ V _{DD}		–1, 2	–2	+2	1, 2, 3	$V_{DD} = \pm 5\%$	mW
Δ Offset/ Δ V _{SS}		–1, 2	–1	+1	1, 2, 3	$V_{SS} = \pm 5\%$	mV
Reference Output		–1, 2	4.99	5.01	1	$V_{DD} = +12 \text{ V and } +15 \text{ V}$ $V_{SS} = -12 \text{ V and } -15 \text{ V}$	V
Δ Reference/ Δ V _{DD}		–1, 2		6	1	$V_{DD} = \pm 5\%$	mV/V
Reference Load Sensitivity		–1, 2	–1.5	+1.5	1, 2, 3	Reference Load Current Change (0–100 μA) Not Including R _{OFFS} Current	mV
Digital Input High Voltage	V _{INH}	–1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V _{INL}	–1, 2		0.8	1, 2, 3		V
Digital Input Current for Data Inputs	I _{IN}	–1, 2	–1	+1	1	$V_{IN} = 0 \text{ or } V_{DD}$	μA
			–10	+10	2, 3		
Digital Input High for Control Inputs ⁴	I _{INH}	–1, 2	–1	+1	1	$V_{IN} = V_{DD}$	μA
			–10	+10	2, 3		
Digital Input Low Current for Control Inputs	I _{INL}	–1, 2		150	1	$V_{IN} = 0 \text{ V}$	μA
				200	2, 3		
Digital Input Capacitance	C _{IN}	–1		8	13, 14, 15		pF
		–2		16			
Output Range Resistors	R _{OUT}	–1, 2	15	30	1, 2, 3		k Ω
Output Ranges ⁵		–1, 2	0 0 –5	5 10 +5	1, 2, 3	Pin Strappable. Minimum Load Resistance is 2 k Ω to GND	V
Power Supply Current	I _{DD}	–1, 2		9 12	1 2, 3	Output Unloaded	mA
Output Voltage Settling Positive and Negative Full-Scale Change ⁶	t _{SL}	–1, 2		5	13	To ± 1 LSB, R _L = 5 k Ω	μs
Output Voltage Slew Rate	SR	–1, 2	2		13, 14, 15		V/ μs
Chip Select Pulse Width	t ₁	–1, 2	105		9		ns
Write Pulse Width	t ₂	–1, 2	105		9		ns
Chip Select to Write Setup Time	t ₃	–1, 2	0		9		ns
Chip Select to Write Hold Time	t ₄	–1, 2	0		9		ns

Table 1. (Continued on next page)

Test	Symbol	Device	Limits		Sub Group	Test Condition ¹	Units
			Min	Max			
Data Valid to Write Setup Time	t ₅	-1	155		9		ns
		-2	180		9		
Data Valid to Write Hold Time	t ₆	-1, 2	0		9		ns
Load DAC Pulse Width	t ₇	-1, 2	90		9		ns
Clear Pulse Width	t ₈	-1	140		9		ns

NOTES - DUAL SUPPLY

¹-55°C < T_A < +125°C unless otherwise specified. Dual Supply, V_{DD} = +11.4 V to +15.75 V, V_{SS} = -11.4 V to -15.75 V = AGND = DGND = 0 V, R_L = 2 kΩ to GND. C_L = 100 pF to GND. REF unloaded, unless otherwise state. Parameters in subgroups 13, 14, 15 are characterized at initial design and after any subsequent redesigns.

²This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

³This error is calculated w.r.t. an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full-scale temperature coefficient is ±30 ppm of FSR/°C.

⁴Control inputs are $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ for AD7245 and $\overline{\text{CSMSB}}$, $\overline{\text{CSLSB}}$, $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ for AD7248.

⁵0 to +10 applies to V_{DD} = +15 V ±5%, only and V_{SS} = -15 V ±5%.

⁶For positive full-scale change, DAC register loaded all 0s to all 1s. For negative full-scale change, DAC register loaded all 1s to all 0s.

Table 1.

AD7245/AD7248 – SPECIFICATIONS

Test	Symbol	Device	Limits		Sub Group	Test Condition ¹	Units
			Min	Max			
Resolution	RES	–1, 2	12		1, 2, 3		Bits
Relative Accuracy	RA	–1, 2	–1	+1	1, 2, 3	V _{DD} = 11.4 V to +14.25 V	LSB
		–1, 2	–1.5	+1.5	13, 14, 15	V _{DD} = 14.25 V to +15.75 V	
Differential Nonlinearity	DNL	–1, 2	–1	+1	1, 2, 3	Guaranteed Monotonic	LSB
Unipolar Offset Error		–1, 2	–3	+3	1		LSB
			–5	+5	2, 3		
DAC Gain Error ²	GE	–1, 2	–2	+2	1, 2, 3		LSB
Full-Scale Output Voltage Error ³	V _{OUT} E	–1, 2	–0.2	+0.2	1	V _{DD} = +12 V and +15 V	% of FSR
			–0.6	+0.6	2, 3		
Δ Full Scale/Δ V _{DD}			–0.12	+0.12	1	V _{DD} = ±5%	% of FSR/V
Δ Offset/Δ V _{DD}		–1, 2	–2	+2	1, 2, 3	V _{DD} = ±5%	mV
Reference Output		–1, 2	4.99	5.01	1	V _{DD} = +12 V and +15 V	V
Δ Reference/Δ V _{DD}		–1, 2	6		1	V _{DD} = ±5%	mV/V
Reference Load Sensitivity		–1, 2	–1.5	+1.5	1, 2, 3	Reference Load Current Change (0–100 μA) Not Including R _{OFS} Current	mV
Digital Input High Voltage	V _{INH}	–1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V _{INL}	–1, 2	0.8		1, 2, 3		V
Digital Input Current for Data Inputs	I _{IN}	–1, 2	–1	+1	1	V _{IN} = 0 or V _{DD}	μA
			–10	+10	2, 3		
Digital Input High for Control Inputs ⁴	I _{INH}	–1, 2	–1	+1	1	V _{IN} = V _{DD}	μA
			–10	+10	2, 3		
Digital Input Low Current for Control Inputs	I _{INL}	–1, 2	150		1	V _{IN} = 0 V	μA
			200		2, 3		
Digital Input Capacitance	C _{IN}	–1	8		13, 14, 15		pF
		–2	16				
Output Range Resistors	R _{OUT}	–1, 2	15	30	1, 2, 3		kΩ
Output Ranges ⁵		–1, 2	0	5 0	1, 2, 3	Pin Strappable. Minimum Load Resistance is 2 kΩ to GND	V
Power Supply Current	I _{DD}	–1, 2	9 12		1 2, 3	Output Unloaded	mA
Output Voltage Settling Positive and Negative Full-Scale Change ⁶	t _{SL}	–1, 2	5		13	To ±1 LSB, R _L = 5 kΩ	μs
Output Voltage Slew Rate	SR	–1, 2	2		13, 14, 15		V/μs
Chip Select Pulse Width	t ₁	–1, 2	105		9		ns
Write Pulse Width	t ₂	–1, 2	105		9		ns
Chip Select to Write Setup Time	t ₃	–1, 2	0		9		ns
Chip Select to Write Hold Time	t ₄	–1, 2			9		ns
Data Valid to Write Setup Time	t ₅	–1	155		9		ns
		–2	180		9		
Data Valid to Write Hold Time	t ₆	–1, 2	0		9		ns
Load DAC Pulse Width	t ₇	–1, 2	90		9		ns
Clear Pulse Width	t ₈	–1	140		9		ns

Table 2. (Continued on next page)

NOTES - SINGLE SUPPLY

¹ $-55^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ unless otherwise specified. Single Supply, $V_{DD} = +11.4\text{ V to } +15.75\text{ V}$, $V_{SS} = \text{AGND} = \text{DGND} = 0\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND. $C_L = 100\text{ pF}$ to GND. REF unloaded, unless otherwise state. Parameters in subgroups 13, 14, 15 are characterized at initial design and after any subsequent redesigns and are not production tested..

² This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

³ This error is calculated w.r.t. an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full-scale temperature coefficient is $\pm 30\text{ ppm}/^{\circ}\text{C}$.

⁴ Control inputs are $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ for AD7245 and $\overline{\text{CSMSB}}$, $\overline{\text{CSLSB}}$, $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ for AD7248.

⁵ 0 to +10 applies to $V_{DD} = +15\text{ V} \pm 5\%$, only and $V_{SS} = -15\text{ V} \pm 5\%$.

⁶ For positive full-scale change, DAC register loaded all 0s to all 1s. For negative full-scale change, DAC register loaded all 1s to all 0s.

Table 2.

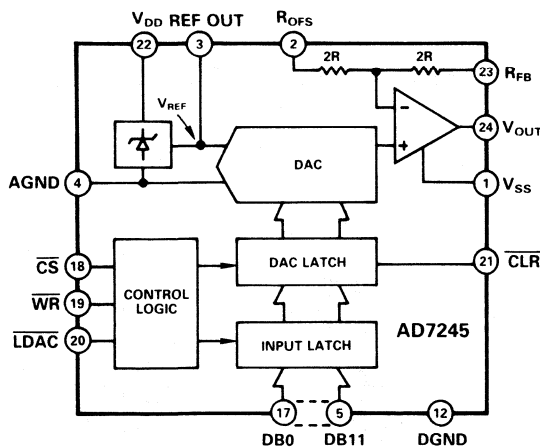
1.3.1 Recommended Operating Conditions.

Single Supply: $V_{DD} = +15\text{ V} \pm 5\%$; $V_{SS} = \text{AGND} = \text{DGND} = 0\text{ V}$.

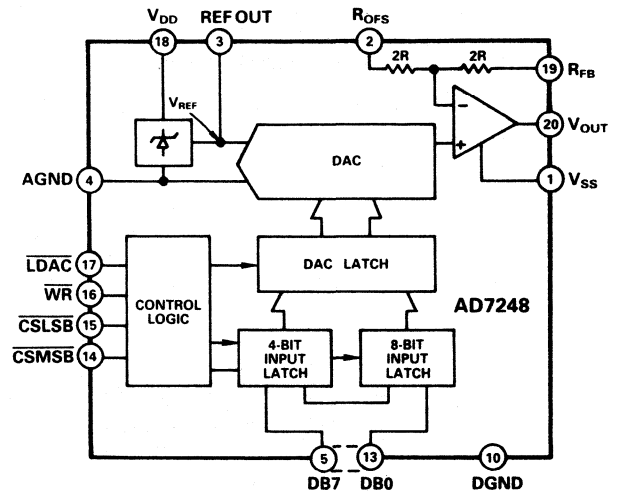
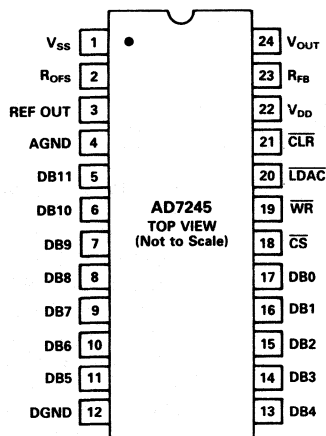
Dual Supply: $V_{DD} = +12\text{ V to } +15\text{ V} \pm 5\%$; $V_{SS} = -12\text{ V to } -15\text{ V} \pm 5\%$.

$R_L = 2\text{ k}\Omega$ to GND; $C_L = 100\text{ pF}$ to GND; REF OUT unloaded.

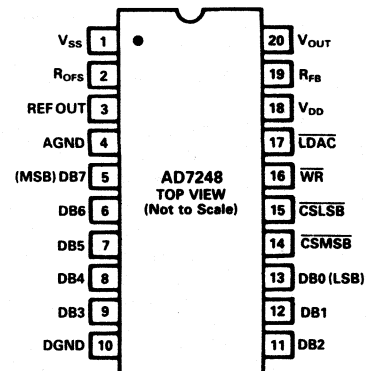
3.2.1 Functional Block Diagram and Terminal Assignments.



DIP (Q-24) Package

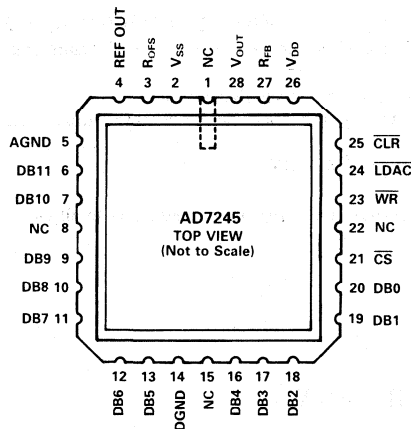


DIP (Q-20) Package



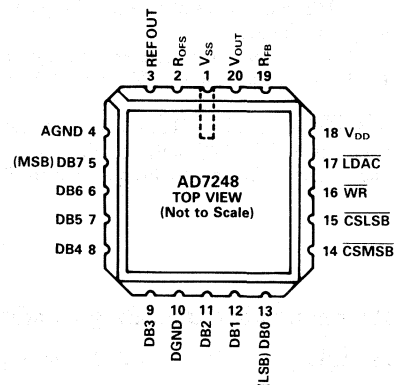
AD7245/AD7248

LCC (E-28A) Package



NC = NO CONNECT

LCC (E-20A) Package

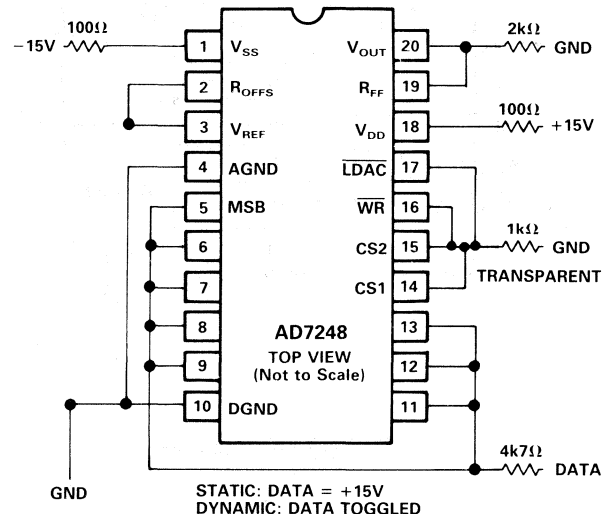
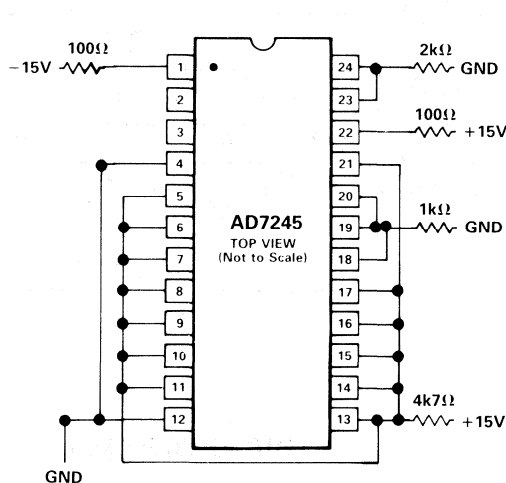


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



STATIC: DATA = +15V
DYNAMIC: DATA TOGGLED

CLR	LDAC	WR	CS	Function
H	L	L	L	Both Latches Are Transparent
H	H	H	X	Both Latches Are Latched
H	H	X	H	Both Latches Are Latched
H	H	L	L	Input Latches Transparent
H	H	L	L	Input Latches Latched
H	L	H	H	DAC Latches Transparent
H	L	H	H	DAC Latches Latched
L	X	X	X	DAC Latches Loaded with All 0s
L	H	H	H	DAC Latches Latched with All 0s and Output Remains at 0 V or -5 V
L	L	L	L	Both Latches Are Transparent and Output Follows Input Data

H = High State L = Low State X = Don't Care

Table 2. AD7245 Truth Table

CSLSB	CSMSB	WR	LDAC	Function
L	H	L	H	Loads LS Byte into Input Latch
L	H	H	H	Latches LS Byte into Input Latch
H	L	L	H	Loads MS Nibble into Input Latch
H	L	H	H	Latches MS Nibble into Input Latch
H	H	L	H	Latches MS Nibble into Input Latch
H	H	H	L	Loads Input Latch into DAC Latch
H	L	L	L	Latches Input Latch into DAC Latch
H	L	L	L	Loads MS Nibble into Input Latch and Loads Input Latch into DAC Latch
H	H	H	H	No Data Transfer Operation

H = High State L = Low State

Table 3. AD7248 Truth Table

REV. A

AD7501/AD7502/AD7503
1.1 Scope.

This specification covers the detail requirements for three monolithic CMOS analog multiplexers. The AD7501 and AD7503 are 8-channel versions which switch one of 8 inputs to a common output. The AD7503 differs from the AD7501 in that its "enable" logic is inverted. The AD7502 is a dual 4-channel multiplexer which switches two output buses to two of 8 inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7501S(X)/883B
-2	AD7502S(X)/883B
-3	AD7503S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-16	16-Pin Side-Brazed Ceramic
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	+17V
V_{SS} to GND	-17V
V Between Any Switch Terminals	+25V
Switch Current (I_S , Continuous)	35mA
Switch Current (I_S , Surge) 1ms Duration, 10% Duty Cycle	50mA
Digital Input Voltage Range	V_{DD} to GND
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for D-16, Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for D-16, Q-16 and E-20A

AD7501/AD7502/AD7503 — SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{\min}$ – $T_{\max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Switch “ON” Resistance ²	R_{ON}	– 1, 2, 3	300	300			$-10\text{V} < V_S < +10\text{V}$, $I_S = 1\text{mA}$	Ω max
Leakage Current, Switch Open	I_{SOFF}	– 1, 2, 3	50	0.5	50		$V_S = -10\text{V}$, $V_{\text{OUT}} = +10\text{V}$ and $V_S = +10\text{V}$, $V_{\text{OUT}} = -10\text{V}$	$\pm$ nA max
Output Current AD7501, AD7503 AD7502	I_{OUT}	– 1, 3 – 2	250 125	5 3	250 125		$V_S = -10\text{V}$, $V_{\text{OUT}} = +10\text{V}$ and $V_S = +10\text{V}$, $V_{\text{OUT}} = -10\text{V}$ AD7501/02 Enable Input = V_{IL} AD7503 Enable Input = V_{IH}	$\pm$ nA max
Difference Between Output and Input Current AD7501, AD7503 AD7502	$I_{\text{OUT}} - I_S$	– 1, 3 – 2	300 175	5.5 3.5	300 175		$V_S = 0\text{V}$	$\pm$ nA max
Digital Input Low Voltage	V_{IL}	– 1, 2, 3	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	– 1, 2, 3	2.4	2.4	2.4			V min
Input Leakage Current	I_{IN}	– 1, 2, 3	30	10	30			$\pm$ μA max
Enable to Switch “ON” Time ²	t_{ON}	– 1, 2, 3	2				$V_{\text{IN}} = 0$ to $+5\text{V}$ and $+5\text{V}$ to 0V	μs max
Enable to Switch “OFF” Time ²	t_{OFF}	– 1, 2, 3	2					μs max
Supply Current from V_{DD}	I_{DD}	– 1, 2, 3	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max
Supply Current from V_{SS}	I_{SS}	– 1, 2, 3	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max

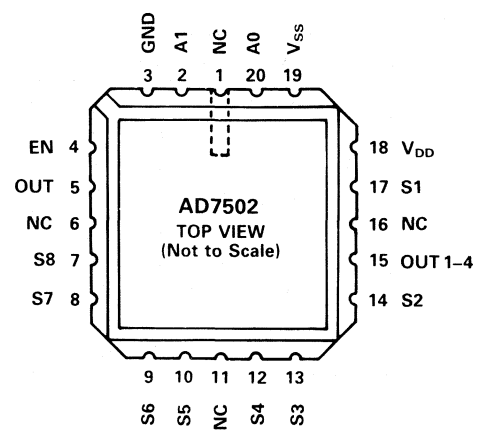
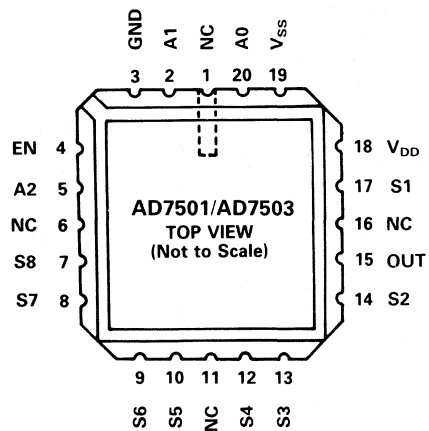
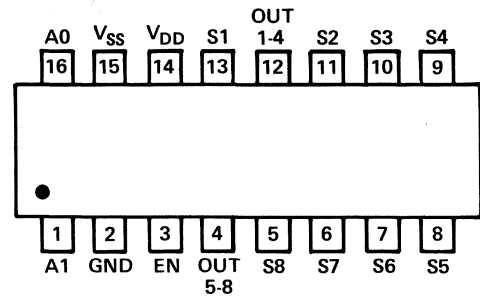
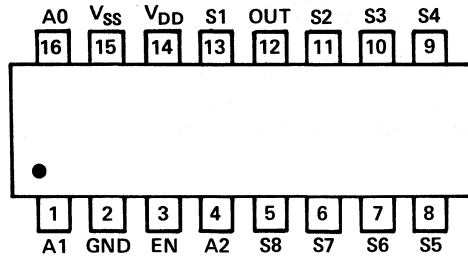
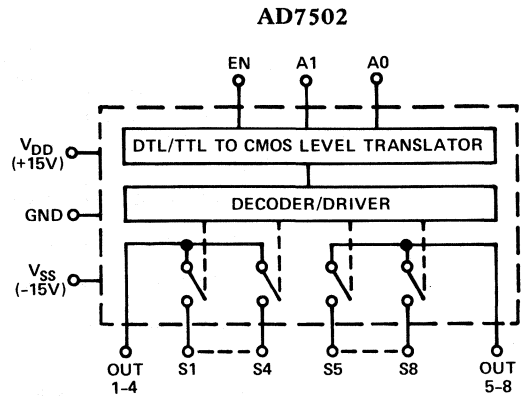
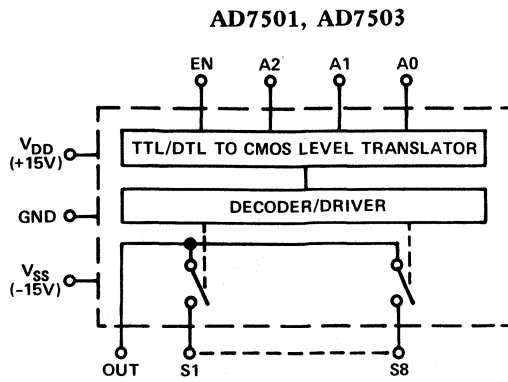
NOTES

¹ $V_{\text{DD}} = +15\text{V}$; $V_{\text{SS}} = -15\text{V}$, devices enabled unless otherwise stated.

²These design limits are for $+25^\circ\text{C}$ only.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



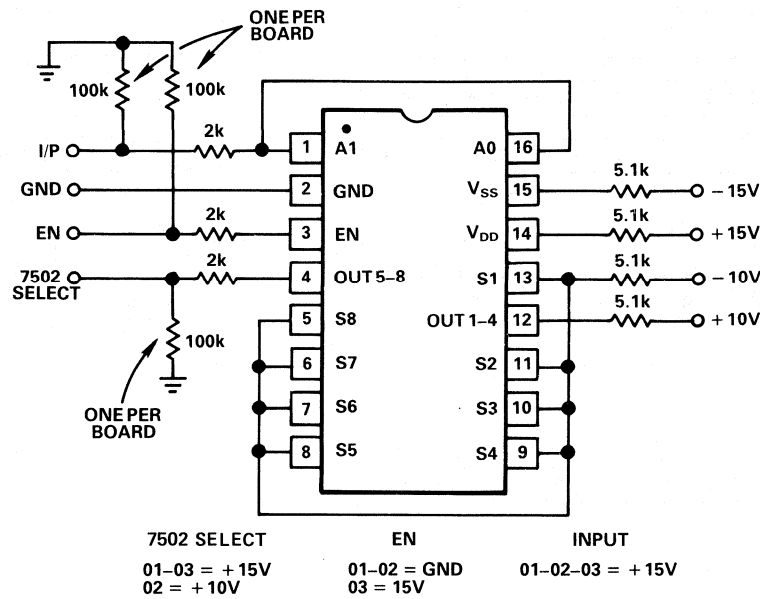
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

AD7501/AD7502/AD7503

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7501				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7503				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

AD7502			
A ₁	A ₀	E _N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

Table 2. Truth Table

1.1 Scope.

This specification covers the detail requirements for CMOS, bidirectional solid state switches with low on resistance and very high off resistance. The AD7506 provides 16-channel single ended multiplexing or demultiplexing of analog signals. The AD7507 provides 8-channel differential multiplexing or demultiplexing of common mode plus differential signals.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7506S(X)/883B
	AD7507S(X)/883B
-2	AD7506T(X)/883B
	AD7507T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Side-Brazed Ceramic
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND		+17V
V_{SS} to GND		-17V
V Between Any Switch Terminals		25V
Digital Input Voltage		V_{DD} to GND
Switch Current (I_S , Continuous)		35mA
Switch Current (I_S , Surge) 1ms Duration, 10% Duty Cycle		50mA
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derates above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for D-28, Q-28 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for D-28, Q-28 and E-28A

AD7506/AD7507 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Switch “ON” Resistance	R_{DS}	– 1, 2	500	400	500		$-10V < V_S < +10V, I_S = 1mA$	Ω max
Leakage Current, Switch Open	I_S	– 1, 2	50	1	50		$V_S = -10V, V_{OUT} = +10V$ and $V_S = +10V, V_{OUT} = -10V$ AD7506/07 Enable Input = V_{IL}	$\pm nA$ max
Output Current AD7506 AD7507	I_{OUT}	– 1, 2	500	10	500		$V_S = -10V, V_{OUT} = +10V$ and $V_S = +10V, V_{OUT} = -10V$ AD7506/07 Enable Input = V_{IL}	$\pm nA$ max
		– 1, 2	250	5	250			
Difference Between Output and Input Current AD7506 AD7507	$I_{OUT}-I_S$	– 1, 2	500	10	500		$V_S = 0V$	$\pm nA$ max
		– 1, 2	250	5	250			
Digital Input Low Voltage	V_{IL}	– 1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	– 1	3.0	3.0	3.0			V min
		– 2	2.4	3.0	2.4	2.4		
Input Leakage Current	I_{IN}	– 1, 2	30	10	30			$\pm \mu A$ max
Address Switch Delay	t_{TRAN}	– 1, 2	1.0				$V_{IN} = 0V$ to 3V and 3V to 0V	μs max
Address to Address Switch Time	t_{OPEN}	– 1, 2	50.0					ns min
Enable to Switch “ON”	t_{ON}	– 1, 2	1.5					μs max
Enable to Switch “OFF”	t_{OFF}	– 1, 2	1.0					μs max
Supply Current from V_{DD}	I_{DD}	– 1, 2	2.0	1.0	2.0		All Digital Inputs = V_{IL}	mA max
			2.0	1.0	2.0		All Digital Inputs = V_{IH}	mA max
Supply Current from V_{SS}	I_{SS}	– 1, 2	2.0	1.0	2.0		All Digital Inputs = V_{IL}	mA max
			2.0	1.0	2.0		All Digital Inputs = V_{IH}	mA max

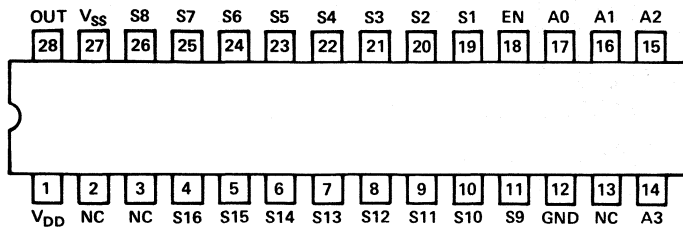
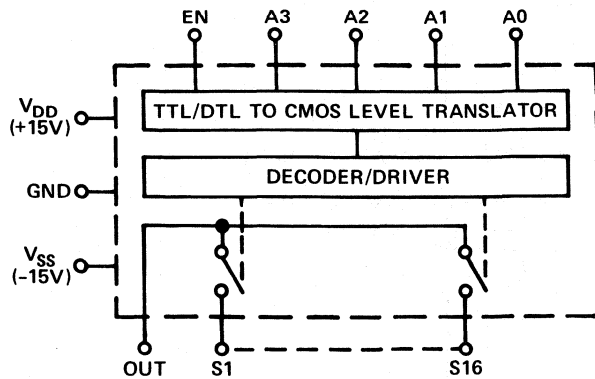
NOTE

¹ $V_{DD} = +15V; V_{SS} = -15V$; devices enabled, unless otherwise stated. Timing parameter design limits are for $+25^\circ C$ only.

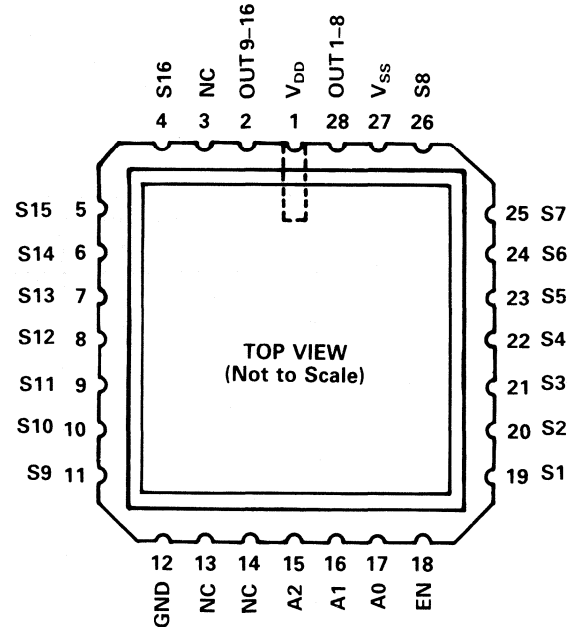
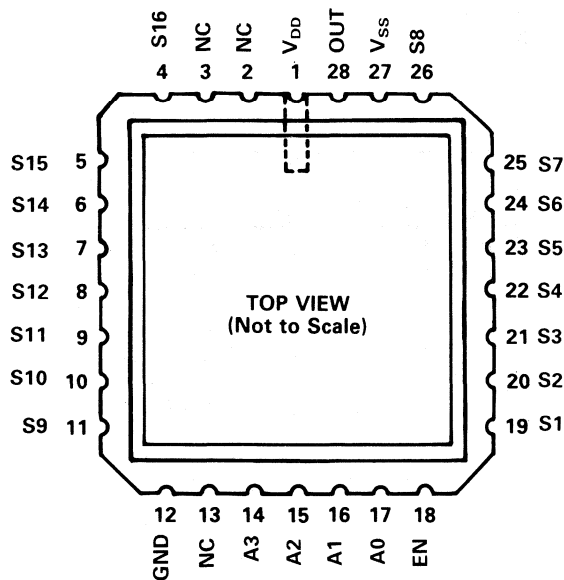
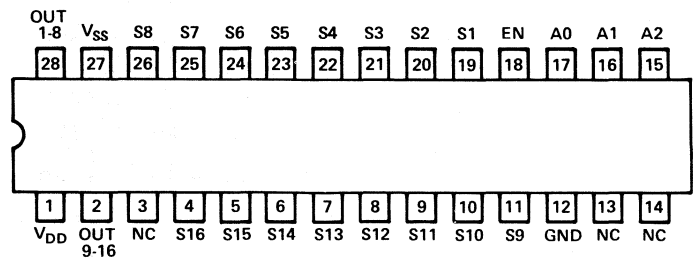
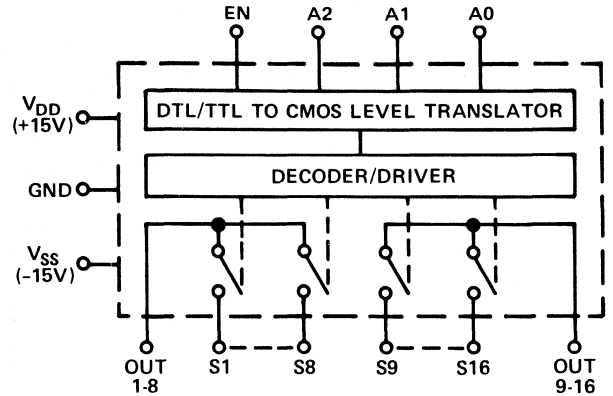
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

AD7506



AD7507



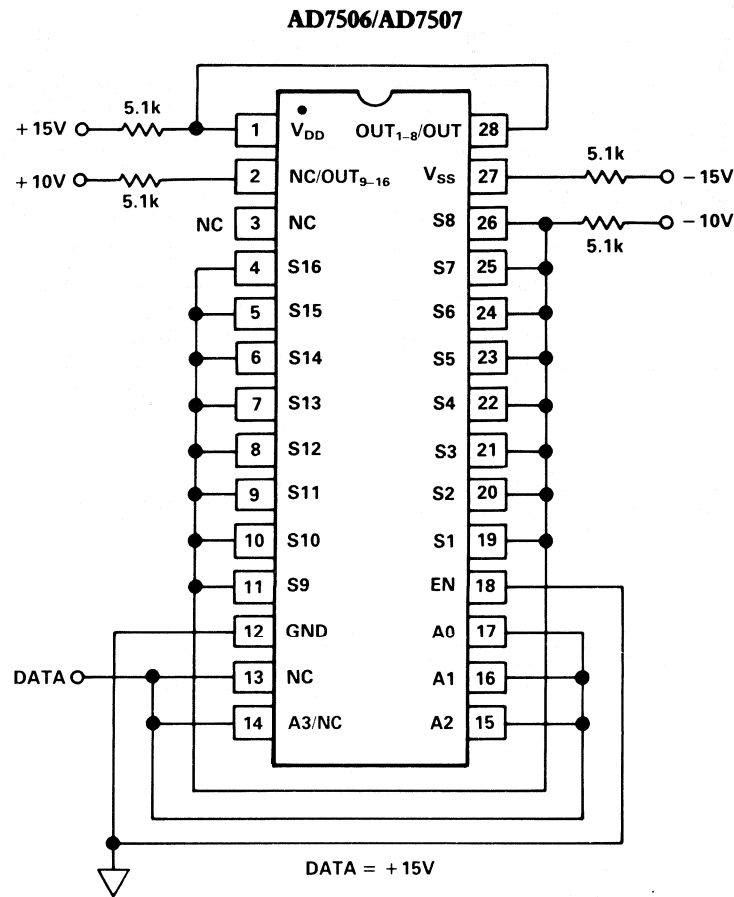
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

AD7506/AD7507

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7506					
A ₃	A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

AD7507				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

Table 2. Truth Tables

1.1 Scope.

This specification covers the detail requirements for two monolithic dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25V$ above the power supplies. Both parts consist of four independent single pole single-throw analog switches differing only in that the digital control logic is inverted on the AD7511DI.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7511DIS(X)/883B
-2	AD7510DIS(X)/883B
-2	AD7511DIT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-16	16-Pin Side-Brazed Ceramic
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ C$ unless otherwise noted)

V_{DD} to DGND	+17V
V_{SS} to GND	-17V
Overvoltage at V_D (V_S)	
(1 second surge)	$V_{DD} + 25V$ or $V_{SS} - 25V$
(Continuous)	$V_{DD} + 20V$ or $V_{SS} - 20V$
Switch Current (I_{DS} , Continuous)	50mA
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	-0.3V to $V_{DD} + 0.3V$
Power Dissipation	
Up to $+75^\circ C$	450mW
Derates above $+75^\circ C$	6mW/ $^\circ C$
Operating Temperature Range	$-55^\circ C$ to $+125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering 10sec)	$+300^\circ C$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ C/W$
 $\theta_{JA} = 120^\circ C/W$

AD7510DI/AD7511DI – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Switch “ON” Resistance	R_{ON}	– 1, 2	175	100	175		$-10V \leq V_D \leq +10V, I_{DS} = 1mA$	Ω max
Leakage Current, Switch Open	I_{DOFF}	– 1, 2	200		200	3	$V_D = -10V, V_S = +10V$ and $V_D = +10V, V_S = -10V$	$\pm nA$ max
Output Current	I_{DON}	– 1, 2	400		400	10	$V_D = V_S = +10V$ and $V_D = V_S = -10V$	$\pm nA$ max
Digital Input Low Voltage	V_{IL}	– 1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	– 1 – 2	3.0 2.4	3.0 2.4	3.0 2.4			V min
Input Leakage Current ²	I_{IN}	– 1, 2	10	10			$V_{IN} = 0V$ or V_{DD}	$\pm nA$ max
Enable to Switch “ON” ²	t_{ON}	– 1, 2	1.0				$V_{IN} = 0$ to $+3V$ and $+3V$ to $0V$	μs max
Enable to Switch “OFF” ²	t_{OFF}	– 1, 2	1.0					μs max
Supply Current from V_{DD}	I_{DD}	– 1, 2	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max
Supply Current from V_{SS}	I_{SS}	– 1, 2	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max

NOTES

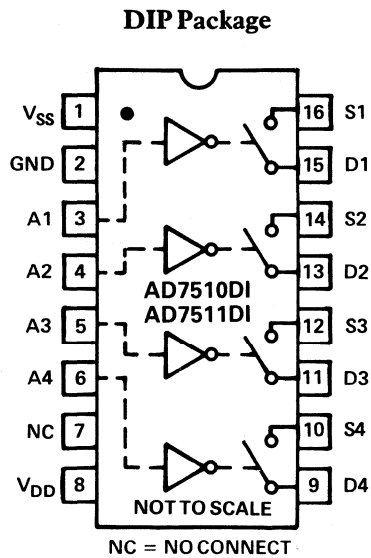
¹ $V_{DD} = +15V$; $V_{SS} = -15V$ unless otherwise stated.

²These design limits are at $+25^\circ C$ only.

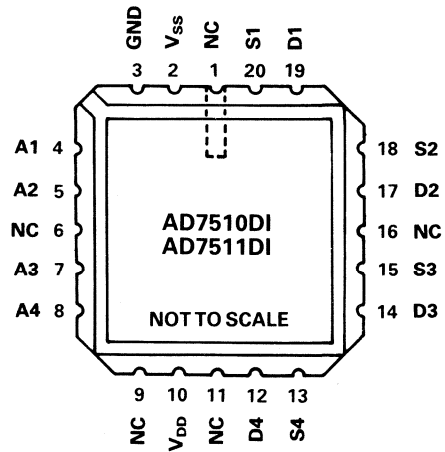
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



E Package (LCC)

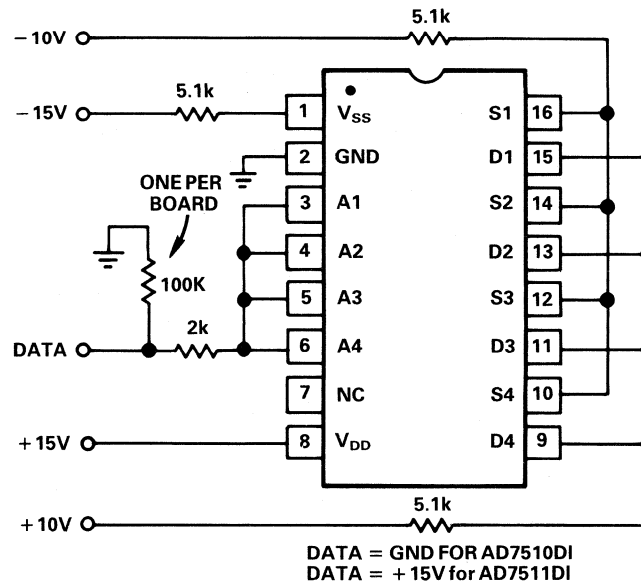


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7510DI: SWITCH "ON" FOR ADDRESS "HIGH"
AD7511DI: SWITCH "ON" FOR ADDRESS "LOW"

1.1 Scope.

This specification covers the detail requirements for a monolithic dielectrically isolated CMOS switch, consisting of two independent single pole double throw switches.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7512DISD/883B
-2	AD7512DITD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-14.

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND		+ 17V
V_{SS} to GND		- 17V
Overvoltage at V_D (V_S)		
(1 second surge)		$V_{DD} + 25\text{V}$ or $V_{SS} - 25\text{V}$
(Continuous)		$V_{DD} + 20\text{V}$ or $V_{SS} - 20\text{V}$
Switch Current (I_{DS} , Continuous)		50mA
1ms Duration, 10% Duty Cycle		150mA
Digital Input Voltage Range		- 0.3V to $V_{DD} + 0.3\text{V}$
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derate above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

AD7512DI – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Switch “ON” Resistance	R_{ON}	– 1, 2	175	100	175		$-10V \leq V_{OUT} \leq +10V, I_{DS} = 1mA$	Ω max
Leakage Current, Switch Open	I_S	– 1, 2	200		200	3	$V_{OUT} = -10V, V_S = +10V$ and $V_{OUT} = +10V, V_S = -10V$	$\pm nA$ max
Difference Between Output ² and Input Current	$I_{OUT}-I_S$	– 1, 2	600		600	9	$V_{OUT} = -10V, V_S = +10V$ and $V_{OUT} = +10V, V_S = -10V$	$\pm nA$ max
Digital Input Low Voltage	V_{IL}	– 1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	– 1 – 2	3.0 2.4	3.0 2.4	3.0 2.4			V min V min
Input Leakage Current ³	I_{IN}	– 1, 2	10	10			$V_{IN} = 0V$ or V_{DD}	$\pm nA$ max
Enable to Switch “ON” ³	t_{ON}	– 1, 2	1.0				$V_{IN} = 0$ to $+3V$ and $+3V$ to $0V$	μs max
Enable to Switch “OFF” ³	t_{OFF}	– 1, 2	1.0					μs max
Supply Current from V_{DD}	I_{DD}	– 1, 2	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max
Supply Current from V_{SS}	I_{SS}	– 1, 2	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max

NOTES

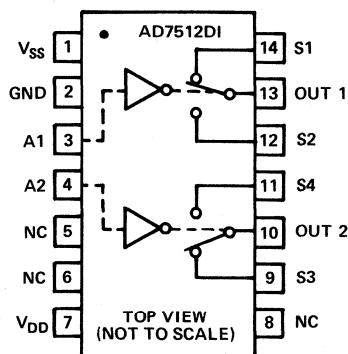
¹ $V_{DD} = +15V$; $V_{SS} = -15V$ unless otherwise stated.

²This is the leakage current flowing in the OUT terminal with 20V across the S terminals.

³These design limits are at $+25^\circ C$ only.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



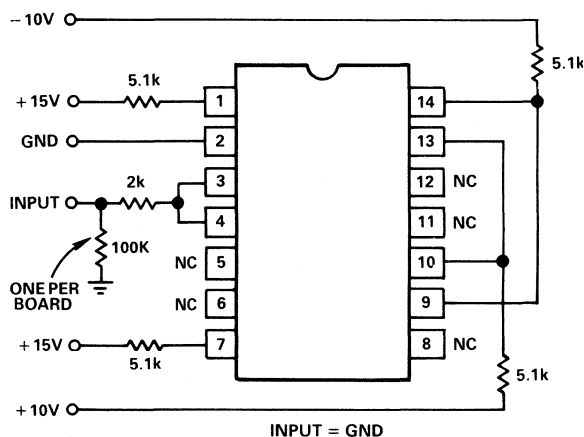
AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2.

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a 10- and a 12-bit monolithic CMOS multiplying digital-to-analog converters.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number
-1	AD7520SQ/883B
	AD7521SQ/883B
-2	AD7520TQ/883B
	AD7521TQ/883B
-3	AD7520UQ/883B
	AD7521UQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-16 – AD7520
Q-18 – AD7521

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND		+17V
V_{REF} to GND		$\pm 25\text{V}$
Digital Input Voltage Range		V_{DD} to GND
Output Voltage (Pins 1 and 2)		-100mV to V_{DD}
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derates above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Digital Input Voltage Range		V_{DD} to GND
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 or Q-18
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 or Q-18

AD7520/AD7521 SPECIFICATIONS

AD7520			Design Limit	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ V _{DD} = +15V	Units
Test	Symbol	Device	T _{min} –T _{max}					
Resolution	RES	–1, 2, 3	10					Bits
Relative Accuracy	RA	–1	2	2	2			± LSB max
		–2	1	2	1	1		
		–3	1/2	2	1/2	1/2		
Nonlinearity Tempco	TC _{NL}	–1, 2, 3	2					± ppm/°C max
Gain Tempco	TC _{AE}	–1, 2, 3	20					± ppm/°C max
Output Leakage Current Pin 1	I _{OUT1}	–1, 2, 3	200	200	200		Digital Inputs = V _{IL} .	± nA max
Pin 2	I _{OUT2}	–1, 2, 3	200	200	200		Digital Inputs = V _{IH} .	± nA max
Output Current Settling Time ²	t _{SL}	–1, 2, 3	500				To ± 1/2LSB. All Digital Inputs V _{IL} to V _{IH} and V _{IH} to V _{IL} .	ns max
Feedthrough Error ^{2,3}	FT	–1, 2, 3	30				V _{REF} = 20V p-p, 100kHz, All Digital Input = V _{IL} .	mV p-p max
Reference Input Resistance	R _{IN}	–1, 2, 3	5	5	5		Measured at Pin 15.	kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V _{IH}	–1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	–1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	–1, 2, 3	1.0					± μA max
Output Capacitance	C _{OUT1}	–1, 2, 3	120				All Digital Inputs V _{IH} .	pF max
		–1, 2, 3	37				All Digital Inputs V _{IH} .	pF max
	C _{OUT2}	–1, 2, 3	37				All Digital Inputs V _{IL} .	pF max
		–1, 2, 3	120				All Digital Inputs V _{IL} .	pF max
Supply Current from V _{DD}	I _{DD}	–1, 2, 3	2	2	2		All Digital Inputs V _{IL} or V _{IH} .	mA max

NOTES

¹V_{REF} = +10V, unless otherwise stated.

²These design limits are +25°C only.

³Feedthrough error can be further minimized by connecting the metal lid to ground.

Table 1.

AD7521 Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	-1, 2, 3	12					Bits
Relative Accuracy	RA	-1	8	8	8			$\pm$ LSB max
		-2	4	8	4	4		
		-3	2	8	2	2		
Nonlinearity Tempco	TC _{NL}	-1, 2, 3	2					$\pm$ ppm/ $^{\circ}C$ max
Gain Tempco	TC _{AE}	-1, 2, 3	20					$\pm$ ppm/ $^{\circ}C$ max
Output Leakage Current Pin 1	I _{OUT1}	-1, 2, 3	200	200	200		Digital Inputs = V_{IL} .	$\pm$ nA max
Pin 2	I _{OUT2}	-1, 2, 3	200	200	200		Digital Inputs = V_{IH} .	$\pm$ nA max
Output Current Settling Time ²	t _{SL}	-1, 2, 3	500				To $\pm 1/2$ LSB. All Digital Inputs V_{IL} to V_{IH} and V_{IH} to V_{IL} .	ns max
Feedthrough Error ^{2,3}	FT	-1, 2, 3	30				$V_{REF} = 20V$ p-p, 100kHz, All Digital Input = V_{IL} .	mV p-p max
Reference Input Resistance	R _{IN}	-1, 2, 3	5 20	5 20	5 20		Measured at Pin 17.	k Ω min k Ω max
Digital Input High Voltage	V _{IH}	-1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	-1, 2, 3	1.0					$\pm$ μ A max
Output Capacitance Pin 1	C _{OUT1}	-1, 2, 3	120				All Digital Inputs V_{IH} .	pF max
Pin 2	C _{OUT2}	-1, 2, 3	37				All Digital Inputs V_{IH} .	pF max
Pin 1	C _{OUT1}	-1, 2, 3	37				All Digital Inputs V_{IL} .	pF max
Pin 2	C _{OUT2}	-1, 2, 3	120				All Digital Inputs V_{IL} .	pF max
Supply Current from V_{DD}	I _{DD}	-1, 2, 3	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max

NOTES

¹ $V_{REF} = +10V$, unless otherwise stated.

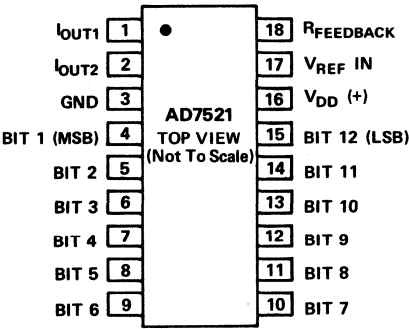
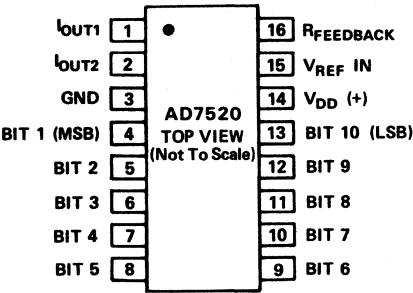
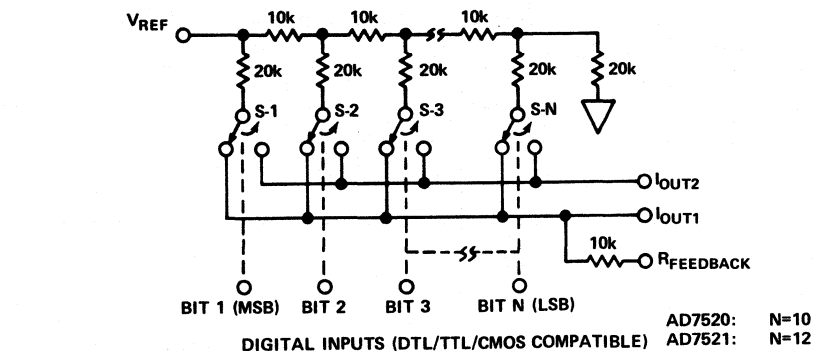
²These design limits are $+25^{\circ}C$ only.

³Feedthrough error can be further minimized by connecting the metal lid to ground.

Table 2.

AD7520/AD7521

3.2.1 Functional Block Diagram and Terminal Assignments.

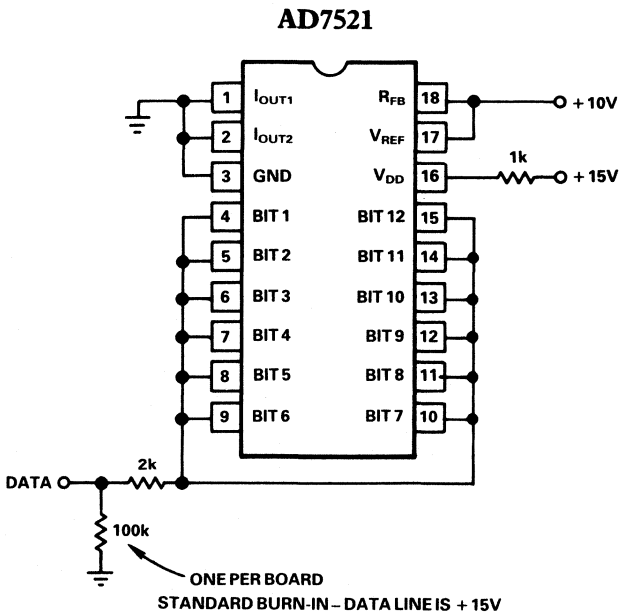
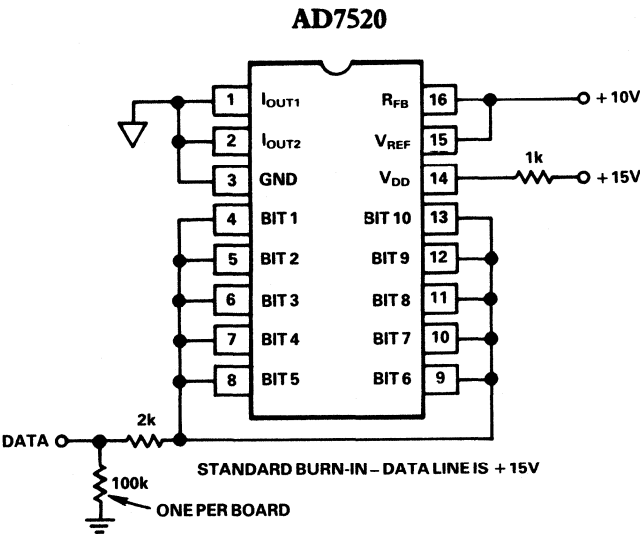


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 10-bit multiplying digital-to-analog converter with an input buffer and a holding register, allowing direct interface with microprocessors.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7522SQ/883B
-2	AD7522TQ/883B
-3	AD7522UQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-28

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{REF} to GND	$\pm 25\text{V}$
V_{DD} to DGND	0V, +17V
V_{CC} to GND	$\pm 17\text{V}$
V_{CC} to V_{DD}	$\pm 0.4\text{V}$
Output Voltage (Pins 6 and 7)	-0.3V, V_{DD}
Digital Input Voltage Range	V_{DD} to GND
Power Dissipation	
Up to $+50^\circ\text{C}$	1000mW
Derates above $+75^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

AD7522 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2, 3	10				SC8 = "1"	Bits
Nonlinearity	NL	-1 -2 -3	2 1 1/2	2 2 2	2 1 1/2	1 1/2		± LSB max
Nonlinearity Tempco	TC _{NL}	-1, 2, 3	2					± ppm/°C max
Gain Tempco	TC _{GA}	-1, 2, 3	30					± ppm/°C max
Output Leakage Current Pin 6 Pin 7	I _{OUT1} I _{OUT2}	-1, 2, 3 -1, 2, 3	200 200	200 200	200 200		DB0 thru DB9 = 0 DB0 thru DB9 = 1	± nA max ± nA max
Feedthrough Error	FT	-1, 2, 3	10				V _{REF} = 20V p-p, 10kHz @ +25°C	mV p-p max
Reference Input Resistance	R _{IN}	-1, 2, 3	5 20	5 20	5 20			kΩ min kΩ max
Digital Input High Voltage	V _{IH}	-1, 2, 3	2.4 13.5	2.4 13.5	2.4 13.5		V _{CC} = +5V V _{CC} = +15V	V min V min
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8 1.5	0.8 1.5	0.8 1.5		V _{CC} = +5V V _{CC} = +15V	V max V max
LDAC Pulse Width	t _{LD}	-1, 2, 3	500				LDAC: 0 to +3V	ns min
HBS, LBS Pulse Width	t _{BS}	-1, 2, 3	500				HBS, LBS: 0 to +3V	ns min
Serial Clock Frequency	t _{CLK}	-1, 2, 3	1					MHz max
HBS, LBS Data Setup ²	t _{DS}	-1, 2, 3	250					ns min
Data Hold Time ³	t _{DH}	-1, 2, 3	500					ns min
Supply Current from V _{DD}	I _{DD}	-1, 2, 3	2	2	2		In Quiescent State at +25°C All Logic Input V _{IL} or V _{IH} .	mA max
Supply Current from V _{CC}	I _{CC}	-1, 2, 3	2	2	2		In Quiescent State at +25°C All Logic Input V _{IL} or V _{IH} .	mA max

NOTES

¹V_{DD} = +15V; V_{CC} = +5V, V_{REF} = +10V unless otherwise stated.

²Data setup time is the minimum amount of time required for DB0–DB9 to be stable prior to strobing HBS, LBS.

³Data hold time is the minimum amount of time required for DB0–DB9 to be stable after strobing HBS, LBS.

Table 1.

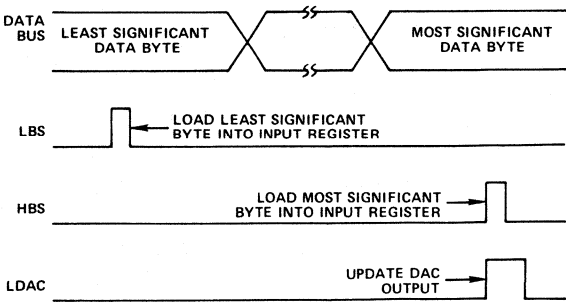


Figure 1. Timing Diagram

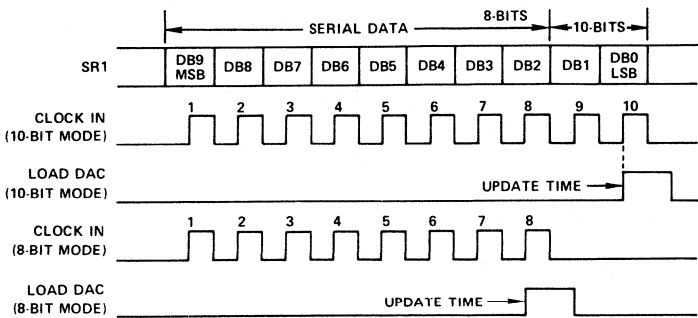


Figure 2. Timing Diagram for Serial 8- and 10-Bit Loading

1.1 Scope.

This specification covers the detail requirements for an 8-bit monolithic CMOS multiplying digital-to-analog converter with on-chip latches for direct interface to most microprocessors. The AD7524 can be used with any supply voltage from +5V to +15V.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7524S(X)/883B
-2	AD7524T(X)/883B
-3	AD7524U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
V_{RFB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage to GND	−0.3V to V_{DD}
V_{OUT1} , V_{OUT2} (Pin 1, Pin 2) to Ground	−0.3V to V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

Note: "Pin numbers refer to DIP package ONLY"

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

AD7524 - SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	- 1, 2, 3	8					Bits
Relative Accuracy	RA	- 1	1/2	1/2	1/2			± LSB max
		- 2	1/4	1/2	1/4	1/4		
		- 3	1/8	1/2	1/8	1/8		
Gain Error ²	AE	- 1, 2, 3	0.6	0.5	0.6			± % FSR max
Gain Tempco	TC _{AE}	- 1, 2, 3	10				From + 25°C to T_{max} to T_{min}	± ppm/°C max
Power Supply Rejection	PSRR	- 1, 2, 3	0.04	0.02	0.04		$\Delta V_{DD} = \pm 10\%$	± %/% max
Output Leakage Current I _{OUT1} I _{OUT2}	I _{OL}	- 1, 2, 3	200	50	200		DB0-DB7 = 0V, $\overline{WR} = \overline{CS} = 0V$	± nA max
	I _{OL}	- 1, 2, 3	200	50	200		DB0-DB7 = V_{DD} , $\overline{WR} = \overline{CS} = 0V$	± nA max
Output Current Settling Time	t _{SL}	- 1, 2, 3	350				To ± 1/2LSB; R _{OUT1} = 100Ω C _{OUT1} = 13pF; $\overline{WR} = \overline{CS} = 0V$; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V	ns max
Feedthrough Error ³	FT	- 1, 2, 3	50				V _{REF} = + 10V, 100kHz Sinewave; DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	mV p-p max
Input Resistance (Pin 15)	R _{IN}	- 1, 2, 3	5	5	5			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V _{IH}	- 1, 2, 3	13.5	13.5	13.5			V min
Digital Input Low Voltage	V _{IL}	- 1, 2, 3	1.5	1.5	1.5			V max
Digital Input Leakage Current	I _{IN}	- 1, 2, 3	10	1	10		V _{IN} = 0V or V_{DD}	± μA max
Digital Input Capacitance DB0-DB7 $\overline{WR}, \overline{CS}$	C _{IN}	- 1, 2, 3	5					pF max
			20					pF max
Output Capacitance	C _{OUT1}	- 1, 2, 3	120				DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$	pF max
	C _{OUT2}	- 1, 2, 3	30					
	C _{OUT1}	- 1, 2, 3	30				DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	pF max
	C _{OUT2}	- 1, 2, 3	120					
Supply Current	I _{DD}	- 1, 2, 3	2	2	2		All Digital Inputs = V _{IL} or V _{IH} All Digital Inputs = 0V or V_{DD}	mA max
			500	100	500			μA max
Chip Select to Write Setup Time ⁴	t _{CS}	- 1, 2, 3	150					ns min
Chip Select to Write Hold Time ⁴	t _{CH}	- 1, 2, 3	0					ns min
Write Pulse Width ⁴	t _{WR}	- 1, 2, 3	150					ns min
Data Setup Time ⁴	t _{DS}	- 1, 2, 3	100					ns min
Data Hold Time ⁴	t _{DH}	- 1, 2, 3	10					ns min

NOTES

¹V_{OUT1} = V_{OUT2} = 0V; V_{REF} = + 10V unless otherwise stated.

²Measured using internal R_{FB} and includes effect of leakage current and gain TC.

³Feedthrough error can be reduced by connecting the metal lid on the package to ground.

⁴Timing per Figure 1.

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Resolution	RES	-1, 2, 3	8					Bits
Relative Accuracy	RA	-1, 2, 3	1/2	1/2	1/2			± LSB max
Gain Error ²	AE	-1, 2, 3	1.4	1.0	1.4			± % FSR max
Gain Tempco	TC _{AE}	-1, 2, 3	40				From +25°C to T_{max} to T_{min}	± ppm/°C max
Power Supply Rejection	PSRR	-1, 2, 3	0.16	0.08	0.16		$\Delta V_{DD} = \pm 10\%$	± %/% max
Output Leakage Current I_{OUT1} I_{OUT2}	I_{OL}	-1, 2, 3	400	50	400		DB0-DB7 = 0V, $\overline{WR} = \overline{CS} = 0V$	± nA max
	I_{OL}	-1, 2, 3	400	50	400		DB0-DB7 = V_{DD} , $\overline{WR} = \overline{CS} = 0V$	± nA max
Output Current Settling Time	t_{SL}	-1, 2, 3	500				To $\pm 1/2LSB$; $R_{OUT1} = 100\Omega$ $C_{OUT1} = 13pF$; $\overline{WR} = \overline{CS} = 0V$; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V	ns max
Feedthrough Error ³	FT	-1, 2, 3	50				$V_{REF} = +10V$, 100kHz Sinewave; DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	mV p-p max
Input Resistance (Pin 15)	R_{IN}	-1, 2, 3	5	5	5			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V_{IH}	-1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2, 3	10	1	10		$V_{IN} = 0V$ or V_{DD}	± μA max
Digital Input Capacitance DB0-DB7 $\overline{WR}$, $\overline{CS}$	C_{IN}	-1, 2, 3	5					pF max
			20					pF max
Output Capacitance	C_{OUT1}	-1, 2, 3	120				DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$	pF max
	C_{OUT2}	-1, 2, 3	30					
	C_{OUT1}	-1, 2, 3	30				DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	pF max
	C_{OUT2}	-1, 2, 3	120					
Supply Current	I_{DD}	-1, 2, 3	2	2	2		All Digital Inputs = V_{IL} or V_{IH}	mA max
			500	100	500		All Digital Inputs = 0V or V_{DD}	μA max
Chip Select to Write Setup Time ⁴	t_{CS}	-1, 2, 3	240					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1, 2, 3	0					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2, 3	240					ns min
Data Setup Time ⁴	t_{DS}	-1, 2, 3	170					ns min
Data Hold Time ⁴	t_{DH}	-1, 2, 3	10					ns min

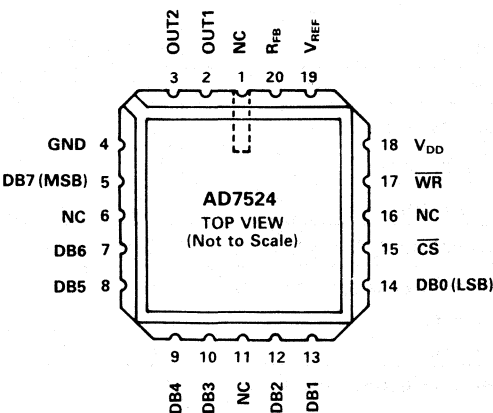
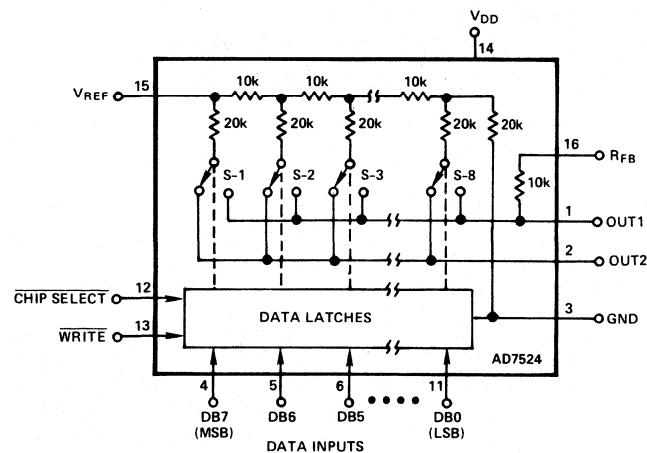
NOTES

¹ $V_{OUT1} = V_{OUT2} = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Measured using internal R_{FB} and includes effect of leakage current and gain TC.³Feedthrough error can be reduced by connecting the metal lid on the package to ground.⁴Timing per Figure 1.

Table 2.

AD7524

3.2.1 Functional Block Diagram and Terminal Assignments.

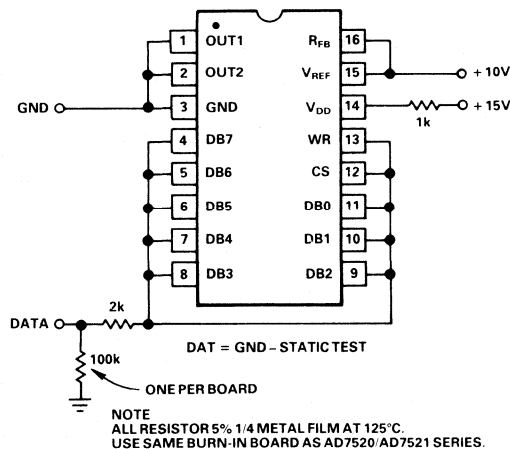


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

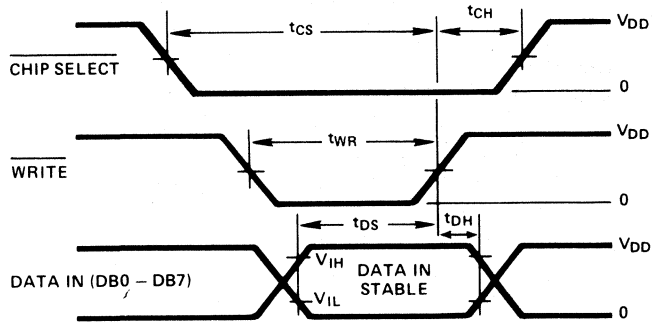
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



$\overline{\text{CS}}$	$\overline{\text{WR}}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when WR or CS assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

Table 3. Mode Selection Table



- NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD} . $V_{DD} = +5V$, $t_r = t_f = 20ns$; $V_{DD} = +15V$, $t_r = t_f = 40ns$.
 2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
 3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at $+25^\circ C$, $V_{DD} = +5V$ and $t_{wr} = 170ns$ min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10ns$, t_{DS} may be reduced accordingly up to the limit $t_{DS} = 65ns$, $t_{DH} = 80ns$.

Figure 1. Write Cycle Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a monolithic dual 8-bit CMOS multiplying digital-to-analog converter with on-chip latches for each DAC to allow easy microprocessor interface.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7528S(X)/883B
-2	AD7528T(X)/883B
-3	AD7528U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, $V_{DD} + 0.3V$
DGND to AGND	V_{DD}
Digital Input Voltage to DGND	-0.3V to +15V
V_{PIN2} , V_{PIN20} to AGND	-0.3V to +15V
V_{REFA} , V_{REFB} to AGND	$\pm 25V$
V_{RFBA} , V_{RFBB} to DGND	$\pm 25V$
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-20 and E-20A

AD7528 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	–1, 2, 3	8					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
		–3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 8 Bits Over Operating Temperature Range	± LSB max
Gain Error ²	A_E	–1	5	4	5			± LSB max
		–2	3	4	3	2		
		–3	1	4	1	1		
Gain Tempco	dA_E/dT	–1, 2, 3	35					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2, 3	0.02	0.01	0.02		$\Delta V_{DD} = \pm 5\%$	± %/% max
Output Leakage Current Pin 2	I_{OL}	–1, 2, 3	200	50	200		DAC Latches Loaded with 0000 0000.	± nA max
Pin 20	I_{OL}	–1, 2, 3	200	50	200		DAC Latches Loaded with 0000 0000.	± nA max
Output Current Settling Time	t_{SL}	–1, 2, 3	350				$T_O \pm 1/2LSB$; $R_{OUTA}/R_{OUTB} = 100\Omega$, $C_{OUTA}/C_{OUTB} = 13pF$; $\overline{WR} = \overline{CS} = 0V$; DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V.	ns max
Feedthrough Error ³ V_{REFA} to OUTA V_{REFB} to OUTB	FTE FTE	–1, 2, 3 –1, 2, 3	55 55				$V_{REFA}/V_{REFB} = \pm 10V$, 100kHz Sinewave; DAC Latches Loaded with 0000 0000.	– dB max
Channel-to-Channel Isolation V_{REFA} to OUTB	V_{CT}	–1, 2, 3	60				$V_{REFA} = \pm 10V$, 100kHz Sinewave; $V_{REFB} = 0V$.	– dB max
V_{REFB} to OUTA		–1, 2, 3	60				$V_{REFB} = \pm 10V$, 100kHz Sinewave; $V_{REFA} = 0V$.	– dB max
Reference Input Resistance V_{REFA} , V_{REFB}	R_I	–1, 2, 3	8 15					k Ω min k Ω max
Reference Input Resistance Match	RM_{IN}	–1, 2, 3	1	1	1			± % max
Digital Input High Voltage	V_{IH}	–1, 2, 3	13.5	13.5	13.5			V min
Digital Input Low Voltage	V_{IL}	–1, 2, 3	1.5	1.5	1.5			V max
Digital Input Leakage Current	I_{IN}	–1, 2, 3	10	1	10		$V_{IN} = 0V$ or V_{DD}	± μA max
Digital Input Capacitance DB0–DB7 $\overline{WR}$, $\overline{CS}$, DACB/DACB	C_I	–1, 2, 3	10 15					pF max
Output Capacitance Pin 2 Pin 20	C_O C_O	–1, 2, 3 –1, 2, 3	50 50				DAC Latches Loaded with 0000 0000.	pF max
Pin 2 Pin 20	C_O C_O	–1, 2, 3 –1, 2, 3	120 120				DAC Latches Loaded with 1111 1111.	pF max
Supply Current from V_{DD}	I_{DD} I_{DD}	–1, 2, 3 –1, 2, 3	2 500	100	500		All Digital Inputs = V_{IL} or V_{IH} All Digital Inputs = 0V or V_{DD}	mA max μA max
Chip Select to Write Setup Time ⁴	t_{CS}	–1, 2, 3	180					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	–1, 2, 3	10					ns min
DAC Select to Write Setup Time ⁴	t_{AS}	–1, 2, 3	180					ns min
DAC Select to Write Hold Time ⁴	t_{AH}	–1, 2, 3	10					ns min
Data Valid to Write Setup Time ⁴	t_{DS}	–1, 2, 3	180					ns min
Data Valid to Write Hold Time ⁴	t_{DH}	–1, 2, 3	10					ns min
Write Pulse Width ⁴	t_{WR}	–1, 2, 3	180					ns min

NOTES

¹ $V_{OUTA} = V_{OUTB} = 0V$; $V_{REF} = +10V$ unless otherwise stated.

²Measured using internal R_{FB} and includes effect of leakage current and gain TC.

³Feedthrough error can be reduced by connecting the lid on the package to ground.

⁴Timing per Figure 1.

Table 1.

REV. C

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Resolution	RES	-1, 2, 3	8					Bits
Relative Accuracy	RA	-1 -2 -3	1 1/2 1/2	1 1 1	1 1/2 1/2			$\pm$ LSB max
Differential Nonlinearity	DNL	-1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 8 Bits Over Operating Temperature Range	$\pm$ LSB max
Gain Error ²	A_E	-1 -2 -3	6 4 3	4 4 4	6 4 3	2 1		$\pm$ LSB max
Gain Tempco	dA_E/dT	-1, 2, 3	70					$\pm$ ppm/ $^{\circ}C$ max
Power Supply Rejection	PSRR	-1, 2, 3	0.04	0.02	0.04		$\Delta V_{DD} = \pm 5\%$	$\pm$ %/% max
Output Leakage Current Pin 2	I_{OL}	-1, 2, 3	400	50	400		DAC Latches Loaded with 0000 0000.	$\pm$ nA max
Pin 20	I_{OL}	-1, 2, 3	400	50	400		DAC Latches Loaded with 0000 0000.	$\pm$ nA max
Output Current Settling Time	t_{SL}	-1, 2, 3	600				To $\pm 1/2$ LSB; $R_{OUTA}/R_{OUTB} = 100\Omega$, $C_{OUTA}/C_{OUTB} = 13pF$; $\overline{WR} = CS = 0V$; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.	ns max
Feedthrough Error ³ V_{REFA} to OUTA V_{REFB} to OUTB	FTE FTE	-1, 2, 3 -1, 2, 3	55 55				$V_{REFA}/V_{REFB} = \pm 10V$, 100kHz Sinewave; DAC Latches Loaded with 0000 0000.	- dB max
Channel-to-Channel Isolation V_{REFA} to OUTB	V_{CT}	-1, 2, 3	60				$V_{REFA} = \pm 10V$, 100kHz Sinewave; $V_{REFB} = 0V$.	- dB max
V_{REFB} to OUTA		-1, 2, 3	60				$V_{REFB} = \pm 10V$, 100kHz Sinewave; $V_{REFA} = 0V$.	- dB max
Reference Input Resistance V_{REFA} , V_{REFB}	R_I	-1, 2, 3	8 15	8 15	8 15			k Ω min k Ω max
Reference Input Resistance Match	R_{MIN}	-1, 2, 3	1					$\pm$ % max
Digital Input High Voltage	V_{IH}	-1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2, 3	10				$V_{IN} = 0V$ or V_{DD}	$\pm$ μA max
Digital Input Capacitance DB0-DB7 $\overline{WR}$, $\overline{CS}$, $\overline{DACA}/\overline{DACB}$	C_I	-1, 2, 3	10 15					pF max
Output Capacitance Pin 2 Pin 20	C_O C_O	-1, 2, 3 -1, 2, 3	50 50				DAC Latches Loaded with 0000 0000.	pF max
Pin 2 Pin 20	C_O C_O	-1, 2, 3 -1, 2, 3	120 120				DAC Latches Loaded with 1111 1111.	pF max
Supply Current from V_{DD}	I_{DD} I_{DD}	-1, 2, 3 -1, 2, 3	2 500	2	2		All Digital Inputs = V_{IL} or V_{IH} All Digital Inputs = 0V or V_{DD}	mA max μA max
Chip Select to Write Setup Time ⁴	t_{CS}	-1, 2, 3	250					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1, 2, 3	20					ns min
DAC Select to Write Setup Time ⁴	t_{AS}	-1, 2, 3	250					ns min
DAC Select to Write Hold Time ⁴	t_{AH}	-1, 2, 3	20					ns min
Data Valid to Write Setup Time ⁴	t_{DS}	-1, 2, 3	220					ns min
Data Valid to Write Hold Time ⁴	t_{DH}	-1, 2, 3	10					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2, 3	220					ns min

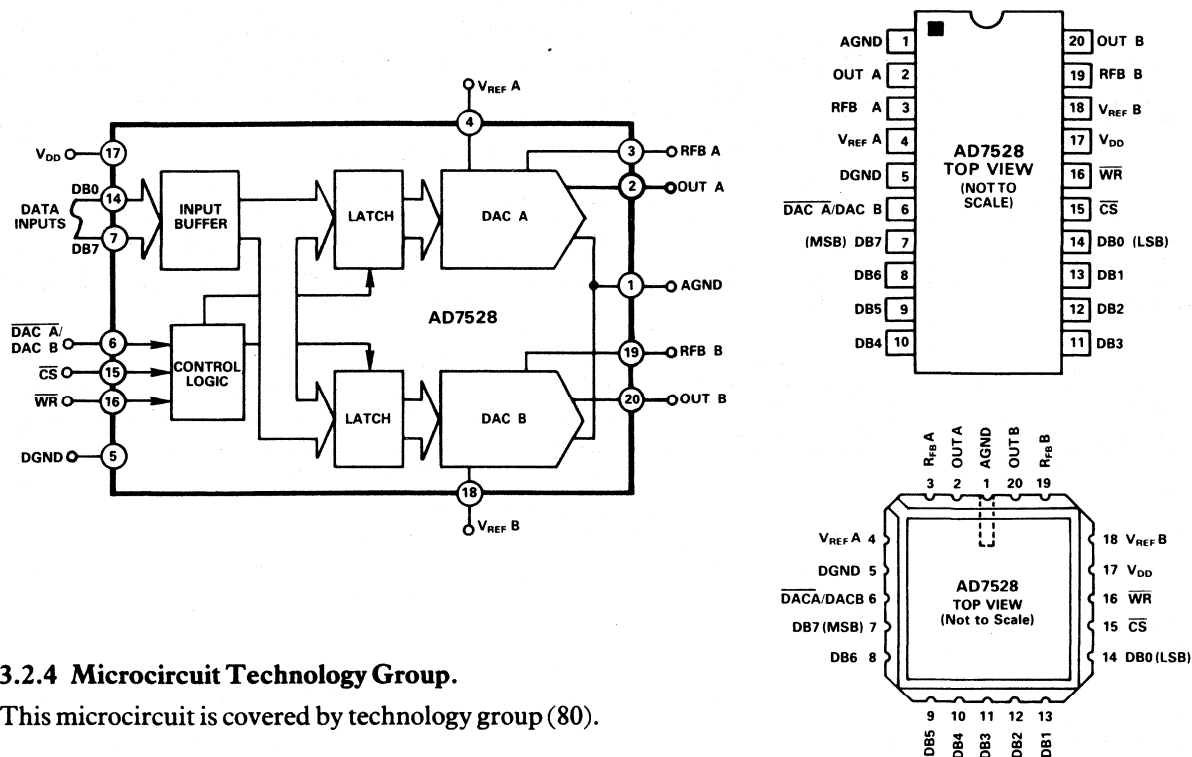
NOTES

¹ $V_{OUTA} = V_{OUTB} = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Measured using internal R_{FB} and includes effect of leakage current and gain TC.³Feedthrough error can be reduced by connecting the lid on the package to ground.⁴Timing per Figure 1.

Table 2.

AD7528

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

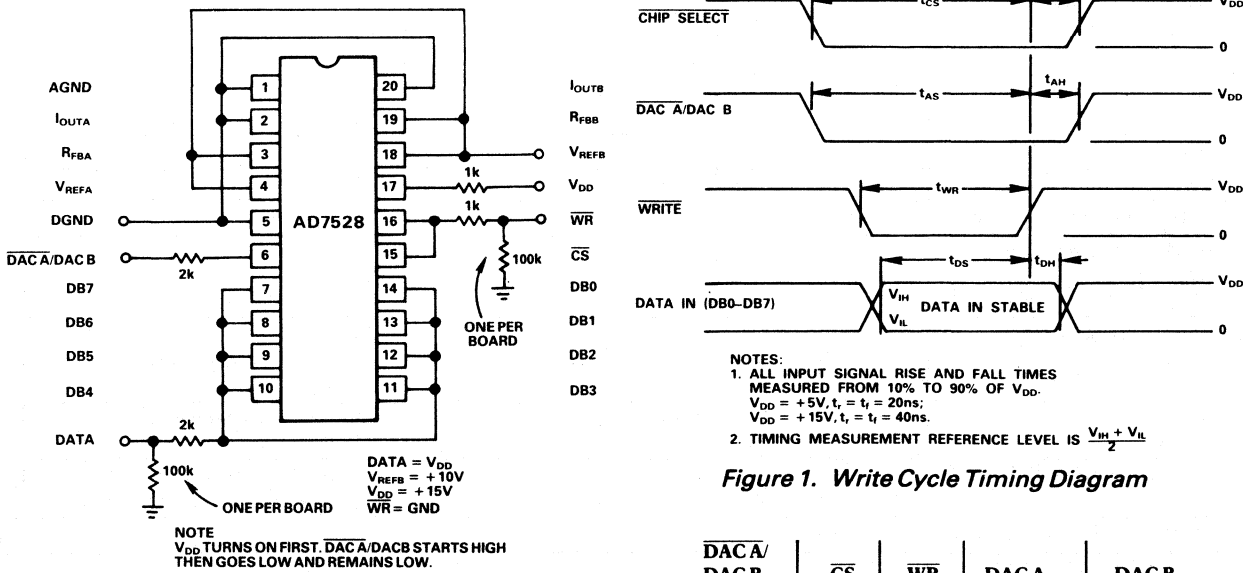


Figure 1. Write Cycle Timing Diagram

$\overline{DAC A/DAC B}$	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Table 3. Mode Selection Table

1.1 Scope.

This specification covers the detail requirements for a monolithic 10-bit CMOS multiplying digital-to-analog converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7533S(X)/883B
-2	AD7533T(X)/883B
-3	AD7533U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	−0.3V to V_{DD}
Power Dissipation	
Up to +50°C	1000mW
Derates above +50°C	10mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: "Pin numbers refer to DIP package ONLY"

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

AD7533 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	- 1, 2, 3	10					Bits
Relative Accuracy	RA	- 1 - 2 - 3	2 1 1/2	2 2 2	2 1 1/2	1 1/2		± LSB max
Gain Error ²	AE	- 1, 2, 3	15	14	15			± LSB max
Gain Tempco	TC _{AE}	- 1, 2, 3	10					± ppm/°C max
Power Supply Rejection	PSRR	- 1, 2, 3	0.008	0.005	0.008		Digital Inputs = V_{IH} ; V_{DD} = 14V to + 17V	± %/% max
Output Leakage Current I_{OUT1} (Pin 1)	I_{OL}	- 1, 2, 3	200	50	200		Digital Inputs = V_{IL} ; (V_{REF} = + 10V)	± nA max
I_{OUT2} (Pin 2)	I_{OL}	- 1, 2, 3	200	50	200		Digital Inputs = V_{IH} ; (V_{REF} = + 10V)	± nA max
Output Current Settling Time	t_{SL}	- 1, 2, 3	800				To ± 1/2LSB; R_{OUT1} = 100Ω C_{OUT1} = 13pF; Digital Inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}	ns max
Feedthrough Error ³	FT	- 1, 2, 3	15				Digital Inputs = V_{IL} ; V_{REF} = ± 10V; 100kHz Sinewave	± mV p-p max
Reference Input Resistance	R_{IN}	- 1, 2, 3	5 20	5 20	5 20			kΩ min kΩ max
Input High Voltage	V_{IH}	- 1, 2, 3	2.4	2.4	2.4			V min
Input Low Voltage	V_{IL}	- 1, 2, 3	0.8	0.8	0.8			V max
Input Leakage Current	I_{IN}	- 1, 2, 3	1	1	1		V_{IN} = 0V or V_{DD}	± μA max
Input Capacitance	C_{IN}	- 1, 2, 3	5					pF max
Output Capacitance Pin 1	C_{OUT1}	- 1, 2, 3	100				Digital Input = V_{IH}	pF max
Pin 2	C_{OUT2}	- 1, 2, 3	35				Digital Input = V_{IH}	pF max
Pin 1	C_{OUT1}	- 1, 2, 3	35				Digital Input = V_{IL}	pF max
Pin 2	C_{OUT2}	- 1, 2, 3	100				Digital Input = V_{IL}	pF max
Supply Current	I_{DD}	- 1, 2, 3	2	2	2		Digital Inputs = V_{IL} or V_{IH}	mA max

NOTES

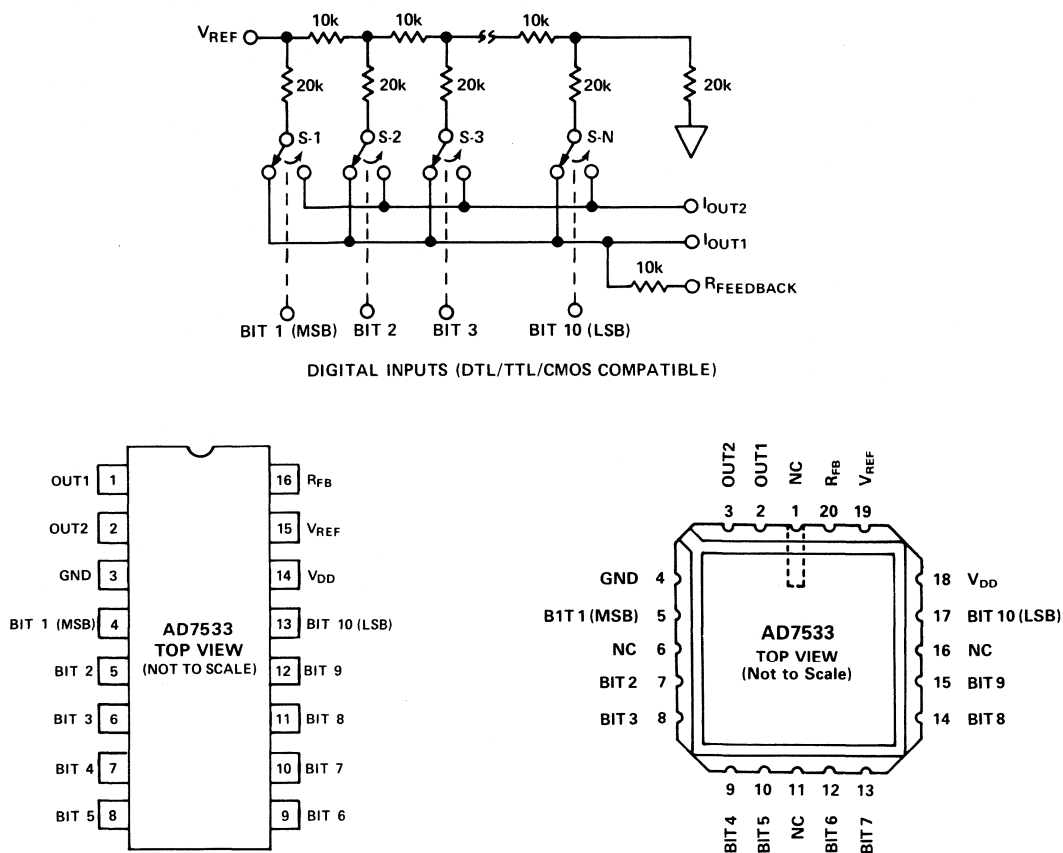
¹ V_{DD} = + 15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = + 10V unless otherwise stated.

²Measured using internal feedback resistor and includes effect of leakage current and gain TC.

³Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

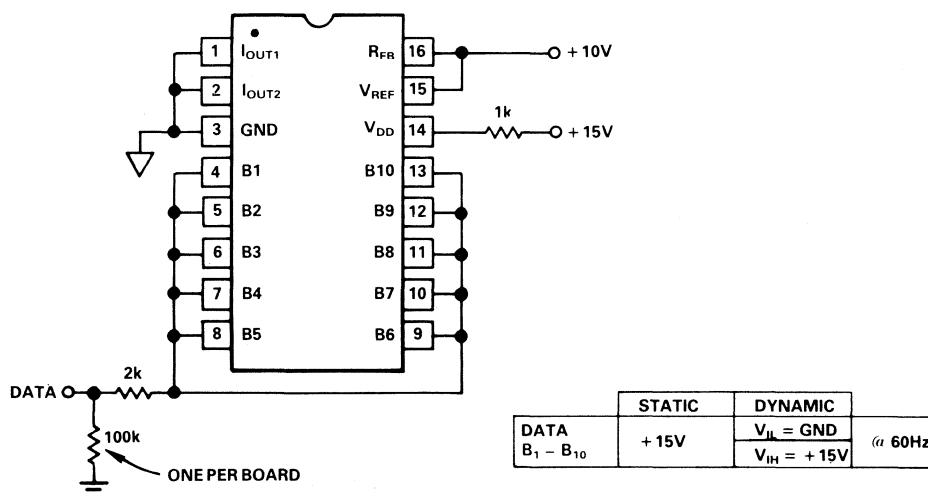


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 14-bit digital-to-analog converter. The device is configured to accept right-justified data in two bytes from an 8-bit data bus. A novel low-leakage configuration enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number
– 1	AD7534SQ/883B
– 2	AD7534TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-20

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} (Pin 19) to DGND	– 0.3V, + 17V
V_{SS} (Pin 20) to AGND	– 15V, + 0.3V
V_{REF} (Pin 1) to AGND	± 25V
V_{RFB} (Pin 2) to AGND	± 25V
Digital Input Voltage (Pins 7-18) to DGND	– 0.3V, V_{DD}
V_{PIN3} to DGND	– 0.3V, V_{DD}
AGND to DGND	– 0.3V, V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	– 55°C to + 125°C
Storage Temperature	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

AD7534 – SPECIFICATIONS

Test	Symbol	Device ²	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	14					Bits
Relative Accuracy	RA	-1 -2	± 2 ± 1	± 2 ± 2	± 2 ± 1	± 1		LSB max
Differential Nonlinearity	DNL	-1, 2	± 1	± 1	± 1	± 1	Guaranteed Monotonic to 14-Bits	LSB max
Gain Error ²	A _E	-1 -2	± 8 ± 4	± 8 ± 8	± 8 ± 4	± 4		LSB max
Gain Tempco	TC _{AE}	-1 -2	± 5 ± 2.5					ppm/°C max
Supply Rejection (Δ Gain/ Δ V _{DD})		-1, 2	± 0.02	± 0.01	± 0.02		Δ V _{DD} = $\pm 5\%$	% per % max
Output Leakage Current (Pin 3)	I _{OUT}	-1, 2 -1, 2	± 20 ± 150	± 5 ± 5	± 20 ± 150		V _{SS} = -300mV (DAC Register Loaded with All 0's) V _{SS} = 0V	nA max nA max
Output Current Settling Time @ 25°C	t _{SL}	-1, 2	1.5				To 0.003% of FSR. I _{OUT} Load = 100Ω, C _{EXT} = 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error ³	FT	-1, 2	10				V _{REF} = ± 10 V, 10kHz Sine Wave DAC Register Loaded with All 0's	mV p-p max
Input Resistance, Pin 1	R _{IN}	-1, 2	3.5 10	3.5 10	3.5 10		Typical Input Resistance = 6kΩ	kΩ min kΩ max
Input High Voltage	V _{IH}	-1, 2	2.4	2.4	2.4			V min
Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V max
Input Leakage Current	I _{IN}	-1, 2	± 10	± 1	± 10		V _{IN} = 0V or V _{DD}	μA max
Input Capacitance	C _{IN}	-1, 2	7					pF max
Analog Output Capacitance: (Pin 3)	C _{OUT}	-1, 2	260 130				DAC Register Loaded with All 1's DAC Register Loaded with All 0's	pF max
Address Valid to Write Setup Time	t _{AWS}	-1, 2	0					ns min
Address Valid to Write Hold Time	t _{AWH}	-1, 2	0					ns min
Data Setup Time	t _{DS}	-1, 2	180					ns min
Data Hold Time	t _{DH}	-1, 2	30					ns min
Chip Select to Write Setup Time	t _{CWS}	-1, 2	0					ns min
Chip Select to Write Hold Time	t _{CWH}	-1, 2	0					ns min
Write Pulse Width	t _{WR}	-1, 2	240					ns min
Power Supply Voltage Range	V _{DD}	-1, 2	11.4 15.75				Specs Guaranteed Over This Range	V min V max
	V _{SS}	-1, 2	-200 -500				Specs Guaranteed Over This Range	mV min mV max
Power Supply Current	I _{DD}	-1, 2	3 500	3 500	3 500		All Digital Inputs V _{IL} or V _{IH} All Digital Inputs 0 or V _{DD}	mA max μA max

NOTES

¹V_{DD} = +12V to 15V; V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = -300mV unless otherwise stated.

Specifications are guaranteed for a V_{DD} of +12V to +15V with a tolerance of $\pm 5\%$; testing is performed at 12V and 15V only. At V_{DD} = 5V, the device is fully functional with a slight degradation in performance.

²Measured using internal feedback resistor and includes effects of leakage current and gain T.C.

³Feedthrough can be further reduced by connecting the metal lid to ground.

Table I.

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 14-bit digital-to-analog converter for direct interfacing to both 8- and 16-bit microprocessor systems. A novel low-leakage configuration enables the AD7535 to exhibit excellent output leakage current characteristics over the specified temperature range.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number ¹
– 1	AD7535S(X)/883B
– 2	AD7535T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28	28-Contact LCC
Q	Q-28	28-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} (Pin 26) to DGND	– 0.3V, + 17V
V_{SS} (Pin 27) to AGND	– 15V, + 0.3V
V_{REFS} (Pin 1) to AGND	± 25V
V_{REFE} (Pin 2) to AGND	± 25V
V_{RFB} (Pin 3) to AGND	± 25V
Digital Input Voltage (Pins 8-25) to DGND	– 0.3V, V_{DD}
V_{PIN4} to DGND	– 0.3V, V_{DD}
AGND to DGND	– 0.3V, V_{DD}
Power Dissipation	
Up to + 75°C	1000mW
Derates above + 75°C	10mW/°C
Operating Temperature Range	– 55°C to + 125°C
Storage Temperature	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-28 and E-28
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-28 and E-28

AD7535 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	14					Bits
Relative Accuracy	RA	– 1	± 2	± 2	± 2			LSB max
		– 2	± 1	± 2	± 1	± 1		
Differential Nonlinearity	DNL	– 1, 2	± 1	± 1	± 1		Guaranteed Monotonic to 14-Bits	LSB max
Gain Error ²	A_E	– 1	± 8	± 8	± 8			LSB max
		– 2	± 4	± 8	± 4	± 4		
Gain Tempco	TC_{AE}	– 1	± 5					ppm/°C max
		– 2	± 2.5					
Supply Rejection ($\Delta\text{Gain}/\Delta V_{DD}$)	PSRR	– 1, 2	± 0.02	± 0.01	± 0.02		$\Delta V_{DD} = \pm 5\%$	% per % max
Output Leakage Current (Pin 4)	I_{OUT}	– 1, 2	± 20	± 5	± 20		$V_{SS} = -300\text{mV}$ (All Digital Inputs 0V)	nA max
			± 150	± 5	± 150		$V_{SS} = 0\text{V}$ (All Digital Inputs 0V)	
Output Current Settling Time (@ 25°C)	t_{SL}	– 1, 2	1.5				To 0.003% of FSR. I_{OUT} LOAD = 100 Ω , $C_{EXT} = 13\text{pF}$. DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error ³	FT	– 1, 2	10				$V_{REF} = \pm 10\text{V}$, 10kHz Sine Wave DAC Register Loaded with All 0's	mV p-p max
Reference Input Resistance (Pin 1)	R_{IN}	– 1, 2	3.5	3.5	3.5		Typical Input Resistance = 6k Ω	k Ω min
			10	10	10			k Ω max
Digital Input High Voltage	V_{IH}	– 1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	– 1, 2	0.8	0.8	0.8			V max
Input Leakage Current	I_{IN}	– 1, 2	± 10	± 1	± 10		$V_{IN} = 0\text{V}$ or V_{DD}	μA max
Input Capacitance	C_{IN}	– 1, 2	7					pF max
Analog Output Capacitance Pin 3	C_{OUT}	– 1, 2	260				DAC Register Loaded with All 1's	pF max
			130				DAC Register Loaded with All 0's	
$\overline{\text{CSMSB}}$ or $\overline{\text{CSLSB}}$ to $\overline{\text{WR}}$ Setup Time	t_{CWS}	– 1, 2	0					ns min
$\overline{\text{CSMSB}}$ or $\overline{\text{CSLSB}}$ to $\overline{\text{WR}}$ Hold Time	t_{CWH}	– 1, 2	0					ns min
$\overline{\text{LDAC}}$ Pulse Width	t_{LDAC}	– 1, 2	240					ns min
Write Pulse Width	t_{WR}	– 1, 2	240					ns min
Data Setup Time	t_{DS}	– 1, 2	180					ns min
Data Hold Time	t_{DH}	– 1, 2	30					ns min
Power Supply Voltage Range	V_{DD}	– 1, 2	11.4				Specs Guaranteed Over This Range	+ V min
			15.75					+ V max
	V_{SS}	– 1, 2	– 200					mV min
			– 300					mV max
Power Supply Current	I_{DD}	– 1, 2	4	4	4		All Digital Inputs V_{IL} or V_{IH}	mA max
			500	500	500		All Digital Inputs 0 or V_{DD}	μA max

NOTES

¹ $V_{DD} = +12\text{V}$ to $+15\text{V}$; $V_{REF} = +10\text{V}$, $V_{PIN3} = V_{PIN4} = 0\text{V}$, $V_{SS} = -300\text{mV}$ unless otherwise stated. Specifications are guaranteed for a V_{DD} of $+12\text{V}$ to $+15\text{V}$ with a tolerance of $\pm 5\%$, testing is performed at 12V and 15V only.

²Measured using internal feedback resistor and includes effects of leakage current and gain T.C.

³Feedthrough can be further reduced by connecting the metal lid to ground.

Table 1.

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 14-bit digital-to-analog converter for direct interfacing to both 8- and 16-bit microprocessor systems. The part is specified as a dedicated bipolar DAC since the resistors needed for 4-quadrant multiplication are contained on the chip. A novel low leakage configuration enables the AD7536 to exhibit excellent output leakage current characteristics over the specified temperature range.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number ¹
– 1	AD7536S(X)/883B
– 2	AD7536T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} (Pin 26) to DGND	– 0.3V, +17V
V_{SS} (Pin 27) to AGND	– 15V, +0.3V
V_{REF} (Pin 2) to AGND	±25V
V_{INV} (Pin 28) to AGND	±25V
R_{INT} (Pin 1) to AGND	±25V
R_{FB} (Pin 3) to AGND	±25V
Digital Input Voltage (Pins 8-25) to DGND	– 0.3V, V_{DD}
V_{PIN4} to DGND	– 0.3V, V_{DD}
AGND to DGND	– 0.3V, V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	1000mW
Derates above $+75^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	– 55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Storage Temperature Range	– 65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (Soldering 10sec)	+300 $^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-28 and E-28A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-28 and E-28A

AD7536 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	14				1LSB = $2V_{REF}/2^{14}$	Bits
Relative Accuracy	RA	– 1	± 2	± 2	± 2			LSB max
		– 2	± 1	± 2	± 1	± 1		
Differential Nonlinearity	DNL	– 1, 2	± 1	± 1	± 1		Guaranteed Monotonic to 14 Bits	LSB max
Gain Error ²	A _E	– 1	± 16	± 16	± 16			LSB max
Offset Error		– 2	± 8	± 16	± 8	± 8	Error due to Mismatch Between R _{FB} and Offset Resistors. It Also Includes Leakage Current to I _{OUT} and is Measured When DAC is Loaded with all 0's.	LSB max
		– 1, 2	± 4	± 4	± 4			
Gain Tempco		– 1, 2	± 5					ppm/°C max
Offset Tempco		– 1, 2	± 5					ppm/°C max
Supply Rejection (Δ Gain/ Δ V _{DD})		– 1, 2	± 0.02	± 0.02	± 0.02		$\Delta V_{DD} = V_{DD} \text{ max and } V_{DD} \text{ min}$	% per % max
Output Current Settling Time @ 25°C		– 1, 2	1.5				To 0.003% of FSR. I _{OUT} Load = 100Ω, C _{EXT} = 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error ³		– 1, 2	10				V _{REF} = $\pm 10V$, 10kHz Sine Wave DAC Register Loaded with 10 0000 0000 0000	mV p-p max
Reference Input Resistance (Pin 2)		– 1, 2	3	3	3		Typical Input Resistance = 6kΩ	kΩ max
			13	13	13			kΩ max
V _{INV} Input Resistance (Pin 28)		– 1, 2	2	2	2			kΩ min
			8	8	8			kΩ max
Digital Input High Voltage	V _{IH}	– 1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V max
Input Leakage Current	I _{IN}	– 1, 2	± 10	± 1	± 10		V _{IN} = 0V or V _{DD}	μA max
Input Capacitance	C _{IN}	– 1, 2	7					pF max
Analog Output Capacitance: (Pin 4)	C _{OUT}	– 1, 2	260				DAC Register Loaded with All 1's	pF max
			130				DAC Register Loaded with All 0's	
CSMSB or CSLSB to $\overline{WR}$ Setup Time ⁴		– 1, 2	0					ns min
CSMSB or CSLSB to $\overline{WR}$ Hold Time		– 1, 2	0					ns min
LDAC Pulse Width		– 1, 2	240					ns min
Write Pulse Width		– 1, 2	240					ns min
Data Setup Time	t _{DS}	– 1, 2	180					ns min
Data Hold Time	t _{DH}	– 1, 2	30					ns min
Power Supply Voltage Range	V _{DD}	– 1, 2	11.4				Specs Guaranteed Over This Range	+ V min
			15.75					+ V max
	V _{SS}	– 1, 2	– 300					V min
Power Supply Current	I _{DD}	– 1, 2	4	4	4		All Digital Inputs V _{IL} or V _{IH}	mA max
			500	500	500		All Digital Inputs 0 or V _{DD}	μA max

NOTES

¹V_{DD} = +11.4V to +15.75V; V_{REF} = +10V, V_{PIN5} = V_{PIN4} = 0V, V_{SS} = –300mV unless otherwise stated.

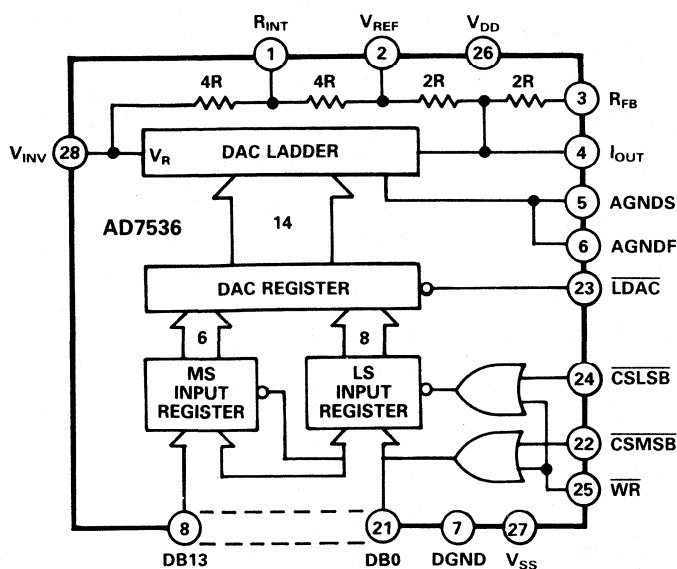
Specifications are guaranteed for a V_{DD} of +12V to +15V with a tolerance of $\pm 5\%$; testing is performed at 12V and 15V only. At V_{DD} = 5V, the device is fully functional with a slight degradation in performance.

²Measured using internal feedback resistor and includes effects of leakage current and gain T.C.

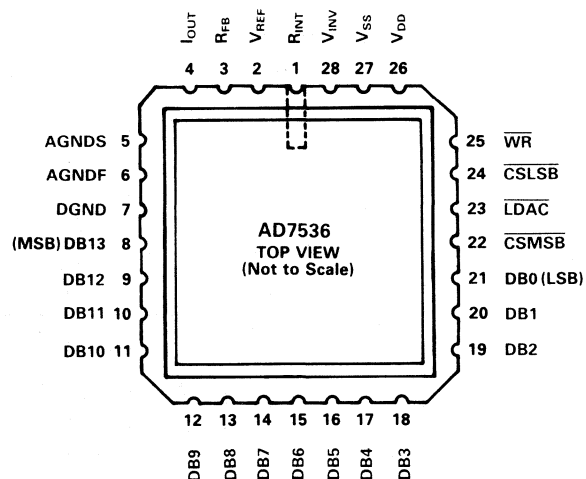
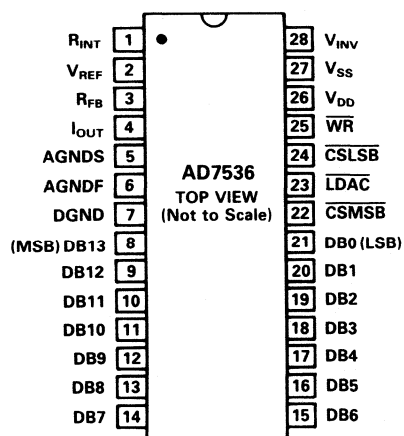
³Feedthrough can be further reduced by connecting the metal lid to ground.

⁴Refer to Timing Diagram.

Table 1.



E Package (LCC)



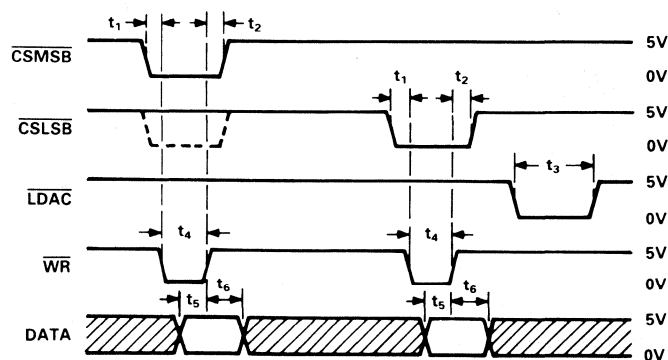
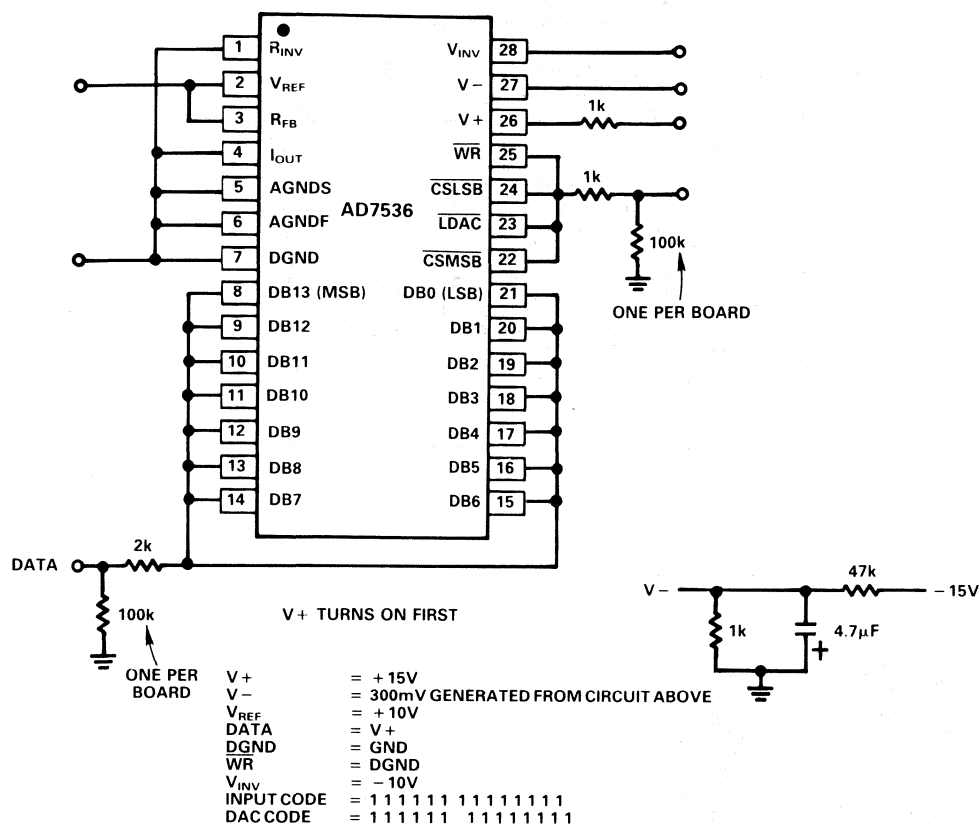
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

AD7536

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20\text{ns}$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF LDAC IS ACTIVATED PRIOR TO THE RISING EDGE OF WR, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER WR GOES HIGH.

AD7536 Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12-bit digital-to-analog converter. The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Each D/A converter has a 2-byte (8 + 4) loading structure. It is designed for right-justified format. The device is easily interfaced to any 8-bit microprocessor system.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7537S(X)/883B
-2	AD7537T(X)/883B
-3	AD7537U(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3" Width
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted, Pin numbers refer to DIP package)

V_{DD} (Pin 20) to DGND	-0.3V, +17V
V_{REFA} , V_{REFB} (Pins 4, 21) to AGNDA, AGNDB	$\pm 25\text{V}$
V_{RFBA} , V_{RFBB} (Pins 3, 22) to AGNDA, AGNDB	$\pm 25\text{V}$
Digital Input Voltage (Pins 5-19) to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
V_{PIN2} , V_{PIN23} to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
AGNDA, AGNDB to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-24 and E-28A

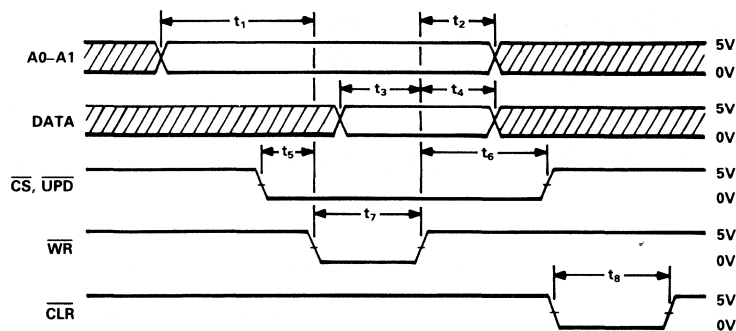
AD7537 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ /Comments	Units
Resolution	RES	– 1, 2, 3	12					Bits
Relative Accuracy	RA	– 1	1	1	1		$V_{DD} = 10.8V$	$\pm$ LSB max
		– 2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	– 1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 12 Bits from T_{min} to T_{max} . $V_{DD} = 10.8V$	$\pm$ LSB max
Gain Error	A_E	– 1	6	6	6		Measured Using R_{FA} and R_{FB} . Both DAC Registers Loaded with All 1s. $V_{DD} = 10.8V$.	$\pm$ LSB max
		– 2	3	6	3	3		
		– 3	2	6	2	2		
Gain Temperature Coefficient	dA_E/dT	– 1, 2, 3	5				Typical Value is 1ppm/°C	$\pm$ ppm/°C max
Output Leakage Current (Pin 2)	I_{OUTA}	– 1, 2, 3	250	10	250		DAC A Register Loaded with All 0s; $V_{DD} = 16.5V$	nA max
Output Leakage Current (Pin 23)	I_{OUTB}	– 1, 2, 3	250	10	250		DAC B Register Loaded with All 0s; $V_{DD} = 16.5V$	nA max
Reference Input Resistance (Pin 4, Pin 21)	R_I	– 1, 2, 3	9	9	9		Typical Input Resistance is 14k $V_{DD} = 10.8V$	k Ω min
			20	20	20			k Ω max
Reference Input Resistance Match V_{REFA}, V_{REFB}	RM_{IN}	– 1, 2	3	3	3		Typically $\pm 0.5\%$ $V_{DD} = 10.8V$	$\pm$ % max
		– 3	1	3	3	1		
Digital Input High Voltage	V_{IH}	– 1, 2, 3	2.4	2.4	2.4		$V_{DD} = 10.8V$ and 16.5V	V min
Digital Input Low Voltage	V_{IL}	– 1, 2, 3	0.8	0.8	0.8		$V_{DD} = 10.8V$ and 16.5V	V max
Digital Input Current	I_{IN}	– 1, 2, 3	10	1	10		$V_{IN} = V_{DD} = 16.5V$	μ A max
Digital Input Capacitance	C_I	– 1, 2, 3	10					pF max
Power Supply Voltage	V_{DD}	– 1, 2, 3	10.8					V min
			16.5					V max
Power Supply Current	I_{DD}	– 1, 2, 3	2	2	2		$V_{DD} = 16.5V$	mA max
Output Current Settling Time (@ 25°C)	t_{SL}	– 1, 2, 3	1.5				To 0.01% of Full-Scale Range. I_{OUT} Load = 100. $C_{EXT} = 13pF$. DAC Output Measured from Rising Edge of WR. Typical Value of Settling Time is 0.8 μ s.	μ s max
AC Feedthrough V_{REFA} to I_{OUTA} and V_{REFB} to I_{OUTB}	FT	– 1, 2, 3	65				$V_{REFA}, V_{REFB} = 20V$ p-p 10kHz Sine-Wave DAC Register Loaded with All 0s.	– dB max
Power Supply Rejection Ratio (Δ Gain/ ΔV_{DD})	PSRR	– 1, 2, 3	0.02	0.01	0.02		$\Delta V_{DD} = 12V \pm 5\%$	$\pm$ %/% max
Output Capacitance for DACA and DACB	C_{OUT}	– 1, 2, 3	70				DACA, DACB Loaded with All 0s.	pF max
			140				DACA, DACB Loaded with All 1s.	
Address Valid to Write Setup Time, t_1	t_{ANS}	– 1, 2, 3	30					ns min
Address Valid to Write Hold Time, t_2	t_{ANH}	– 1, 2, 3	25					ns min
Data Setup Time, t_3	t_{DS}	– 1, 2, 3	80					ns min
Data Hold Time, t_4	t_{DH}	– 1, 2, 3	25					ns min
Chip Select to Write Setup Time, t_5	t_{CWS}	– 1, 2, 3	0					ns min
Chip Select to Write Hold Time, t_6	t_{CWH}	– 1, 2, 3	0					ns min
Write Pulse Width, t_7	t_{WR}	– 1, 2, 3	100					ns min
Clear Pulse Width, t_8	t_{CL}	– 1, 2, 3	100					ns min

NOTES

¹ $V_{DD} = +12V$ to $+15V \pm 10\%$ except where otherwise stated; $V_{REFA} = V_{REFB} = 10V$; $V_{PIN2} = V_{PIN1} = 0V$; $V_{PIN23} = V_{PIN24} = 0V$. Output amplifiers are AD644.
Pin numbers refer to DIP Package.

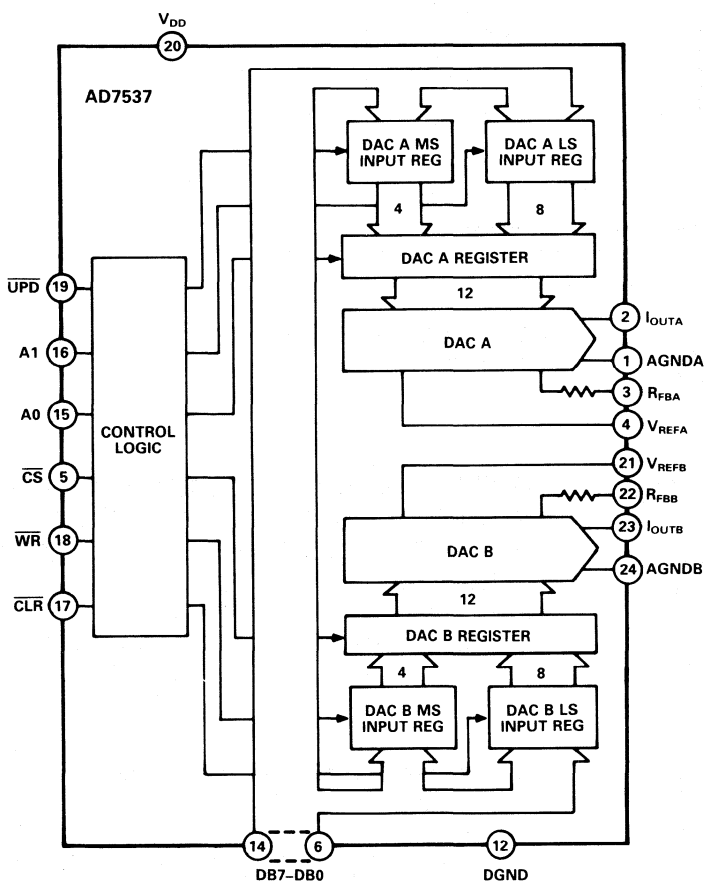
Table 1.



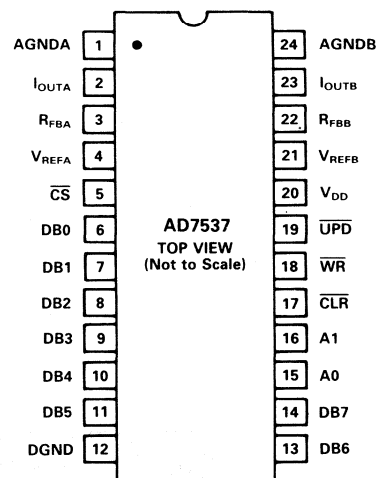
- NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20\text{ns}$.
 2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

Figure 1. Timing Diagram for AD7537

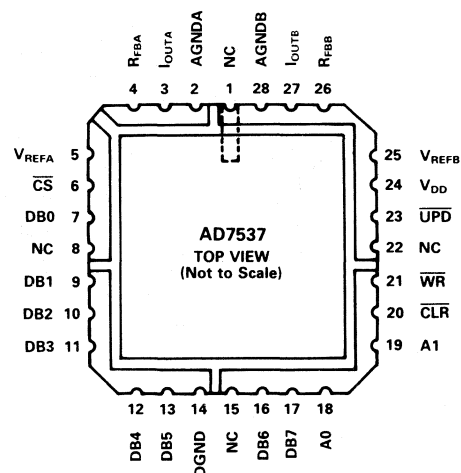
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

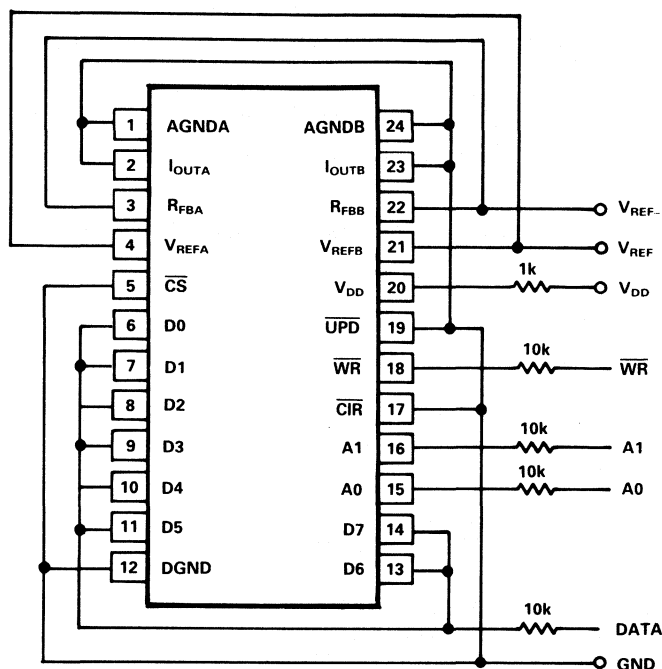


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

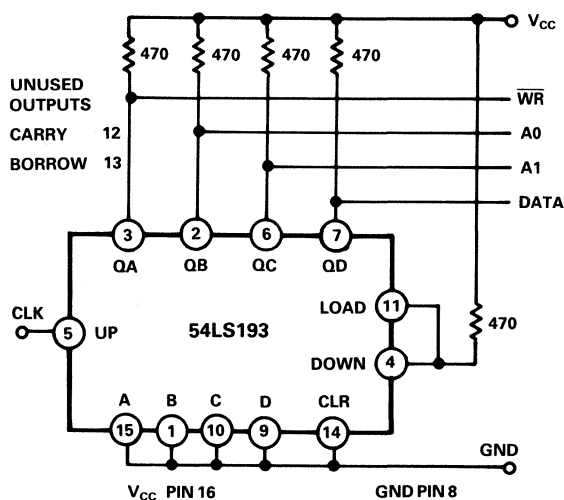
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



EXTERNAL INPUTS

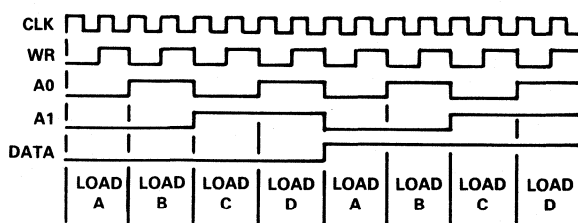
V_{REF-} -10V
 V_{REF} 10V
 V_{DD} 15V
 CLK
 GND

A0, A1, DATA AND $\overline{WR}$ ARE DERIVED FROM THE 54193 CONTROL CIRCUIT.



EXTERNAL INPUTS

V_{CC} 5V
 GND
 CLK
 ALL RESISTORS 10%



1. THERE ARE 6 CONNECTIONS TO EACH BOARD.
 $V_{DD} = 15V$ $V_{REF} = 10V$
 $V_{CC} = 5V$ $V_{REF-} = -10V$
 CLOCK GND
2. EACH AD7537 SOCKET HAS 5 RESISTORS ASSOCIATED WITH IT. 1k ON THE V_{DD} LINE, 10k ON THE CONTROL LINES $\overline{WR}$, A0, A1 AND 10k COMMON TO ALL DATA LINES.
3. UPD IS TIED LOW SO THE DAC REAR RANK LATCHES ARE TRANSPARENT.
4. THE DAC CODES ARE TOGGLED BETWEEN 0 AND FULL SCALE EVERY 4 CLOCK PULSES.
5. EACH BOARD HAS A 54193 4-BIT COUNTER CONTROLLING THE LOADING AND TOGGING OF DATA.
6. THIS BOARD IS FOR DYNAMIC BURN-IN ONLY.
7. RESISTOR TOLERANCE 10%.

5.0 Unipolar Binary Operation (2-Quadrant Multiplication)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table 2.

Operational amplifiers A1 and A2 can be in a single package (AD644) or separate packages (AD544, AD OP-27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high-speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7537, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

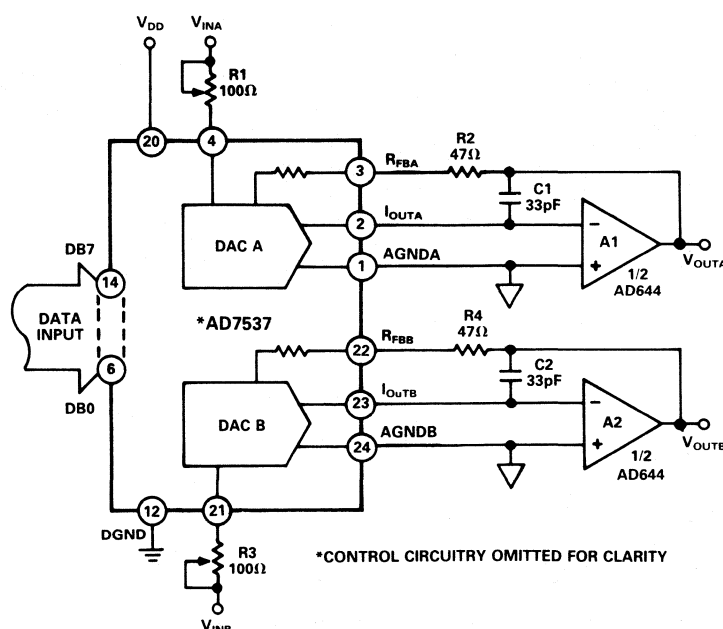


Figure 2. AD7537 Unipolar Binary Operation

Binary Number in DAC Register		Analog Output, V_{OUTA} or V_{OUTB}
MSB	LSB	
1111	1111 1111	$-V_{IN} \left(\frac{4095}{4096} \right)$
1000	0000 0000	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000 0001	$-V_{IN} \left(\frac{1}{4096} \right)$
0000	0000 0000	0V

Table 2. Unipolar Binary Code Table for Circuit of Figure 2

6.0 Bipolar Operation (4-Quadrant Multiplication)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table 3.

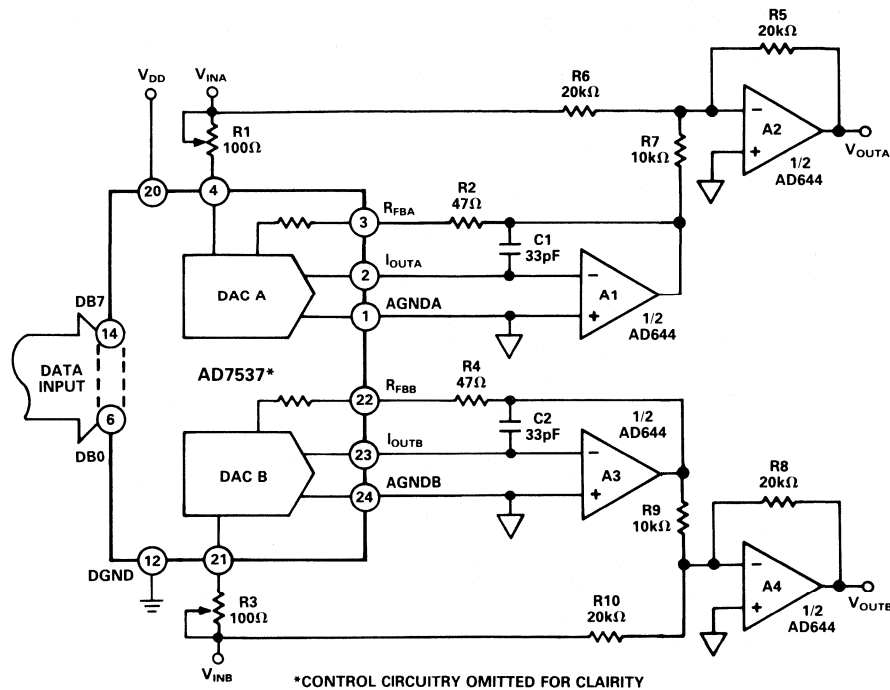


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register		Analog Output, V_{OUTA} or V_{OUTB}
MSB	LSB	
1111	1111 1111	$+V_{IN} \left(\frac{2047}{2048} \right)$
1000	0000 0001	$+V_{IN} \left(\frac{1}{2048} \right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{IN} \left(\frac{1}{2048} \right)$
0000	0000 0000	$-V_{IN} \left(\frac{2048}{2048} \right) = -V_{IN}$

Table 3. Bipolar Code Table for Offset Binary Circuit of Figure 3

1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	AD7541S(X)/883B
–2	AD7541T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} to GND	+17V
V_{REF} to GND	$\pm 25\text{V}$
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pin 1, Pin 2)	–0.3V to V_{DD}
Power Dissipation	
Up to $+50^\circ\text{C}$	1000mW
Derates above $+50^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-18 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-18 and E-20A

AD7541 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	12					Bits
Relative Accuracy	RA	– 1	1	1	1			± LSB max
		– 2	1/2	1	1/2	1/2		
Gain Error ²	AE	– 1, 2	16.7	12.5	16.7			± LSB max
Gain Tempco	TC _{AE}	– 1, 2	13					± ppm/°C max
Power Supply Rejection	PSRR	– 1, 2	0.02	0.01	0.02		V _{DD} = 14.5V to 15.5V	± % per % max
Output Leakage Current Pin 1	I _{OUT1}	– 1, 2	200	50	200		Digital Inputs = V _{IL} V _{REF} = + 10V	± nA max
Pin 2	I _{OUT2}	– 1, 2	200	50	200		Digital Inputs = V _{IH} V _{REF} = + 10V	± nA max
Output Current Settling Time		– 1, 2	1				To ± 1/2LSB, R _{OUT1} = 100Ω, C _{OUT1} = 13pF Digital Inputs = V _{IH} to V _{IL} or V _{IL} to V _{IH}	μs max
Feedthrough Error ³	FT	– 1, 2	1				V _{REF} = 20V p-p at 10kHz	mV p-p max
Reference Input Resistance	R _{IN}	– 1, 2	5	5	5			kΩ min
		– 1, 2	20	20	20			kΩ max
Digital Input High Voltage	V _{IH}	– 1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	– 1, 2	1	1	1		V _{IN} = 0V or 15V	± μA max
Digital Input Capacitance	C _{IN}	– 1, 2	8					pF max
Output Capacitance Pin 1	C _{OUT1}	– 1, 2	200				Digital Inputs = V _{IH}	pF max
Pin 2	C _{OUT2}	– 1, 2	60				Digital Inputs = V _{IH}	pF max
Pin 1	C _{OUT1}	– 1, 2	60				Digital Inputs = V _{IL}	pF max
Pin 2	C _{OUT2}	– 1, 2	200				Digital Inputs = V _{IL}	pF max
Supply current from V _{DD}	I _{DD}	– 1, 2	2	2	2		Digital Inputs = V _{IH} or V _{IL}	mA max

NOTES

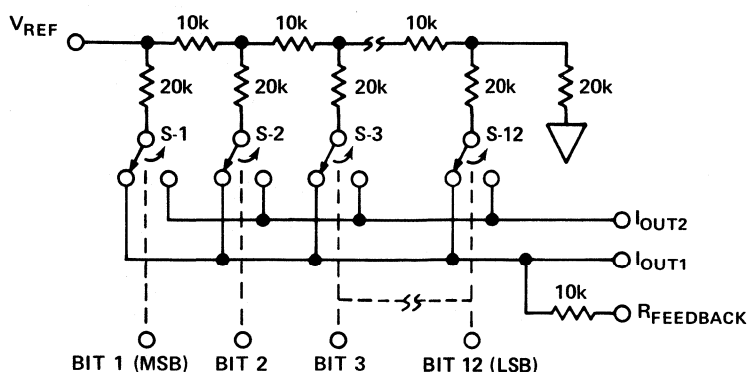
¹V_{DD} = + 15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = + 10V unless otherwise stated.

²Measured using internal feedback resistor and includes effect of leakage current and gain TC.

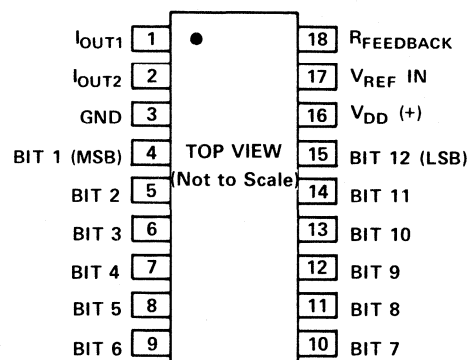
³Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

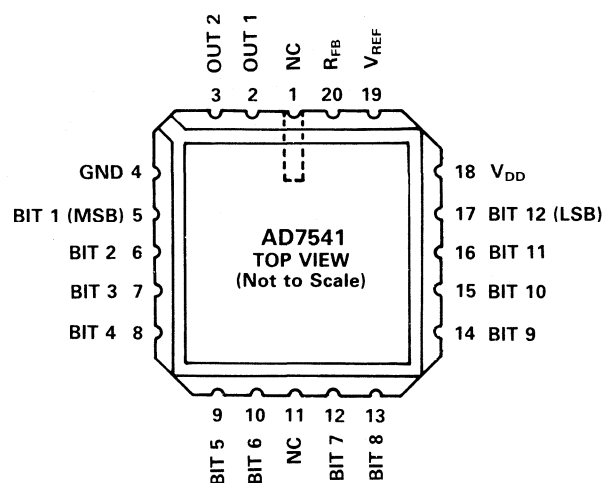
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)

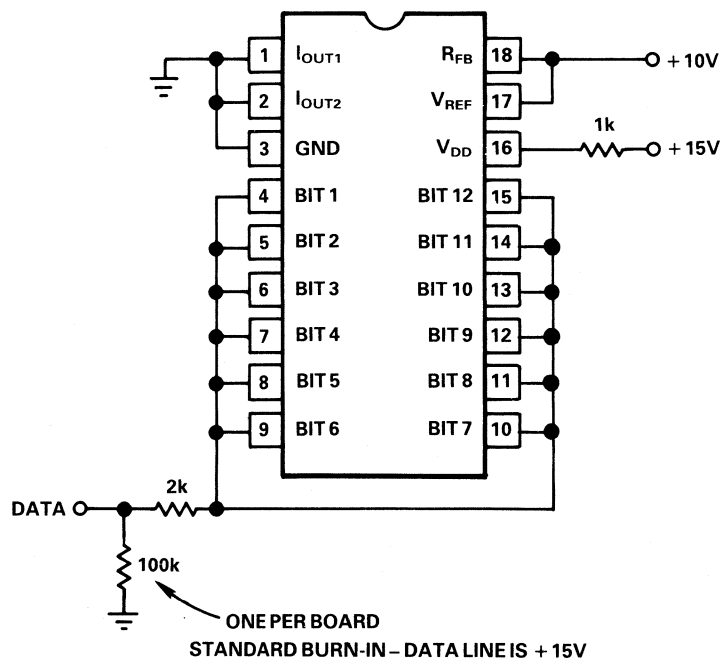


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter. The AD7541A is a direct replacement for the industry standard AD7541, offering improved performance in the areas of latch-up, lower gain error and gain temperature coefficient.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7541AS(X)/883B
-2	AD7541AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} (Pin 16) to GND	+17V
V_{REF} (Pin 17) to GND	$\pm 25\text{V}$
V_{RFB} (Pin 18) to GND	$\pm 25\text{V}$
Digital Input Voltage (Pin 4–Pin 15) to GND	$-0.3\text{V}, V_{DD}$
V_{PIN1}, V_{PIN2} to GND	-0.3V to V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-18 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-18 and E-20A

AD7541A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +125°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	–1, 2	12					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits, T_{min} to T_{max}	± LSB
		–2	1/2	1	1/2	1/2		
Gain Error ²	AE	–1	8	6	8			± LSB max
		–2	5	6	5	3		
Gain Tempco	TC _{AE}	–1, 2	5					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2	0.02	0.01	0.02		$\Delta V_{DD} = \pm 5\%$	± % per % max
Output Leakage Current Pin 1 Pin 2	I _{OUT1}	–1, 2	200	5	200		Digital Inputs = 0V	± nA max
	I _{OUT2}	–1, 2	200	5	200		Digital Inputs = V_{DD}	± nA max
Output Current Settling Time		–1, 2	0.6				To ± 1/2LSB, $R_{OUT1} = 100\Omega$, $C_{OUT1} = 13pF$ Digital Inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}	µs typ
Feedthrough Error ³	FT	–1, 2	1				$V_{REF} = \pm 10V$ 10kHz Sinewave $T_A = +25^\circ C$	mV p-p typ
Reference Input Resistance	R _{IN}	–1, 2	7	7	7			kΩ min
		–1, 2	18	18	18			kΩ max
Digital Input High Voltage	V _{IH}	–1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	–1, 2	1	1	1		$V_{IN} = 0V$ or V_{DD}	± µA max
Digital Input Capacitance	C _{IN}	–1, 2	8					pF max
Output Capacitance Pin 1 Pin 2 Pin 1 Pin 2	C _{OUT1}	–1, 2	200				Digital Inputs = V_{IH}	pF max
	C _{OUT2}	–1, 2	70				Digital Inputs = V_{IH}	pF max
	C _{OUT1}	–1, 2	70				Digital Inputs = V_{IL}	pF max
	C _{OUT2}	–1, 2	200				Digital Inputs = V_{IL}	pF max
Supply Current from V_{DD}	I _{DD}	–1, 2	2	2	2		Digital Inputs = V_{IH} or V_{IL}	mA max
			500	100	500		Digital Inputs = 0V or V_{DD}	µA max

NOTES

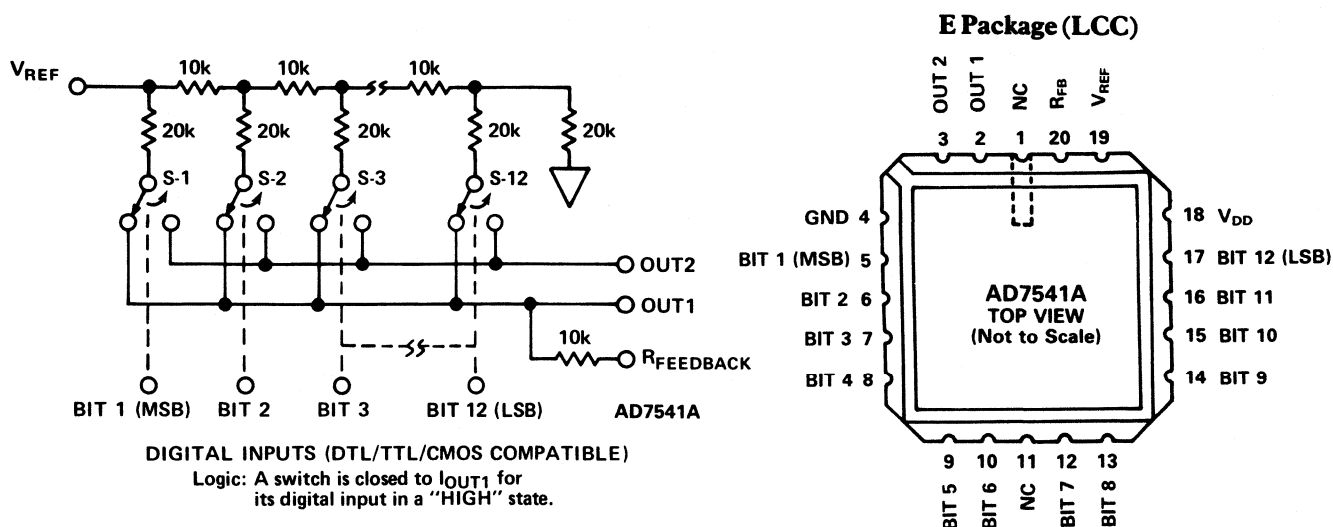
¹ $V_{DD} = +15V$; $V_{OUT1} = V_{OUT2} = 0V$; $V_{REF} = +10V$ unless otherwise stated.

²Measured using internal feedback resistor and includes effect of leakage current and gain TC.

³Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

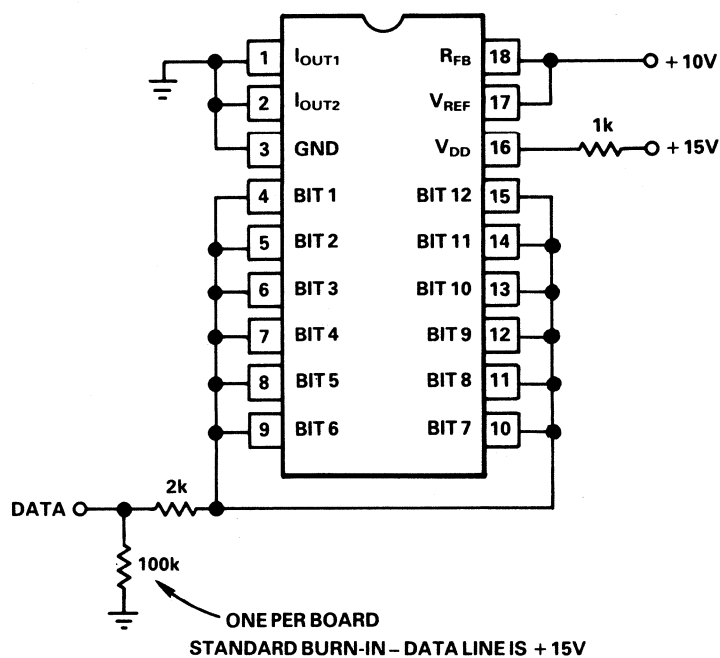


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12-bit multiplying digital-to-analog converter with three 4-bit data registers and a 12-bit DAC register on-chip. It interfaces directly with 4- or 8-bit microprocessors.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7542S(X)/883B
-2	AD7542T(X)/883B
-3	AD7542GT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND (Pins 4-11, 13)	-0.3V, +15V
V_{PIN1} , V_{PIN2} to AGND	-0.3V, +15V
V_{REF} to AGND	$\pm 25\text{V}$
V_{RFB} to AGND	$\pm 25\text{V}$
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

AD7542 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	- 1, 2, 3	12					Bits
Relative Accuracy	RA	- 1	1	1	1			± LSB max
		- 2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	- 1	2	2	2		Monotonic to 11 Bit from T_{min} to T_{max}	± LSB max
		- 2, 3	1	2	1	1	Monotonic to 12 Bit from T_{min} to T_{max}	± LSB max
Gain Error ²	AE	- 1, 2	14.5	12.3	14.5			± LSB max
		- 3	2	12.3	2	1		
Gain Tempco	TC _{AE}	- 1, 2, 3	5					± ppm/°C max
Supply Rejection (Δ Gain/ Δ V _{DD})	PSRR	- 1, 2, 3	0.01	0.005	0.01		Δ V _{DD} = ± 5%	± % per % max
Output Leakage Current I _{OUT1} (Pin 4)	I _{OUT1}	- 1, 2, 3	200	10	200		DAC Registers Loads with All 0's	± nA max
I _{OUT2} (Pin 5)	I _{OUT2}	- 1, 2, 3	200	10	200		DAC Register Loads with All 1's	± nA max
Output Current Settling Time	t _{SL}	- 1, 2, 3	2				To ± 1/2LSB R _{OUT1} = 100Ω, C _{OUT1} = 13pF, DAC. Output Measured from Trailing Edge of WR.	μs max
Feedthrough Error ³	FTE	- 1, 2, 3	2.5				V _{REF} = 10V, 10kHz Sinewave	mV p-p max
Reference Input Resistance (Pin 15)	R _{IN}	- 1, 2, 3	8	8	8			kΩ min
			25	25	25			kΩ max
Digital Input High Voltage	V _{IH}	- 1, 2, 3	3.0	3.0	3.0			V min
Digital Input Low Voltage	V _{IL}	- 1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	- 1, 2, 3	1	1	1		V _{IN} = 0V or V _{DD}	± μA max
Digital Input Capacitance	C _{IN}	- 1, 2, 3	8					pF max
Output Capacitance C _{OUT1} (Pin 1)	C _{OUT1}	- 1, 2, 3	260				Digital Inputs = V _{IH} . DAC Register Loaded with 1111 1111 1111	pF max
C _{OUT2} (Pin 2)	C _{OUT2}	- 1, 2, 3	75				Digital Inputs = V _{IH} . DAC Register Loaded with 1111 1111 1111	pF max
C _{OUT1} (Pin 1)	C _{OUT1}	- 1, 2, 3	75				Digital Inputs = V _{IL} . DAC Register Loaded with 0000 0000 0000	pF max
C _{OUT2} (Pin 2)	C _{OUT2}	- 1, 2, 3	260				Digital Inputs = V _{IL} . DAC Register Loaded with 0000 0000 0000	pF max
Write Pulse Width ⁴	t _{WR}	- 1, 2, 3	220					ns min
Address-to-Write Hold Time ⁴	t _{AWH}	- 1, 2, 3	80					ns min
Chip Select-to-Write Hold Time ⁴	t _{CWH}	- 1, 2, 3	100					ns min
Minimum CLEAR Pulse Width ⁴	t _{CLR}	- 1, 2, 3	300					ns min
Chip Select-to-WRITE Setup Time ⁴	t _{CWS}	- 1, 2, 3	130				Byte Loading	ns min
Address Valid to WRITE Setup Time ⁴	t _{AWS}	- 1, 2, 3	180				Byte Loading	ns min
Data Setup Time ⁴	t _{DS}	- 1, 2, 3	150					ns min
Data Hold Time ⁴	t _{DH}	- 1, 2, 3	65					ns min
Chip Select to WRITE Setup Time ⁴	t _{CWS}	- 1, 2, 3	150				DAC Loading	ns min
Address Valid to WRITE Setup Time ⁴	t _{AWS}	- 1, 2, 3	240				DAC Loading	ns min
Power Requirements	I _{DD}	- 1, 2, 3	2.5	2.5	2.5		Digital Inputs V _{IH} or V _{IL}	mA max

NOTES

¹V_{DD} = + 5V; V_{OUT1} = V_{OUT2} = 0V, V_{REF} = + 10V unless otherwise stated.

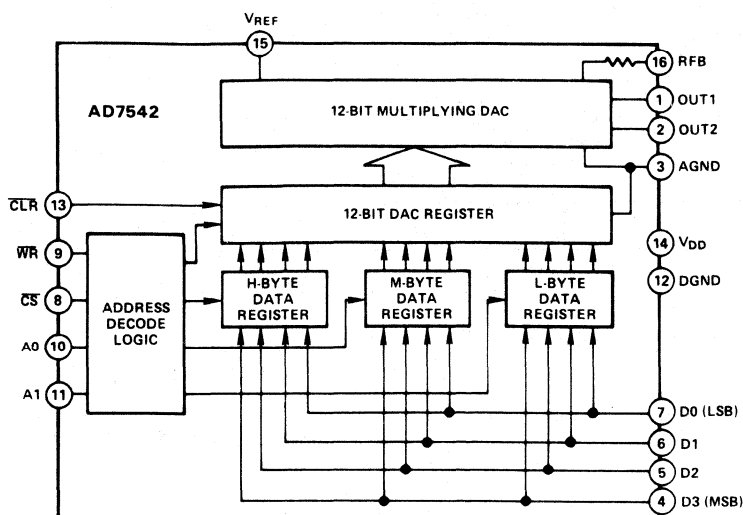
²Measured using internal feedback resistor and includes the effect of 5ppm max gain TC.

³Feedthrough can be further reduced by connecting the metal lid to ground.

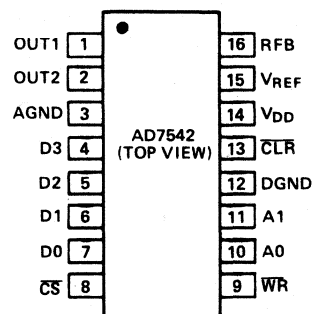
⁴Timing per Figure 1.

Table 1.

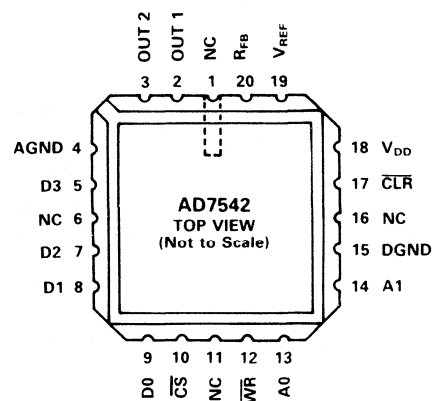
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package



E Package

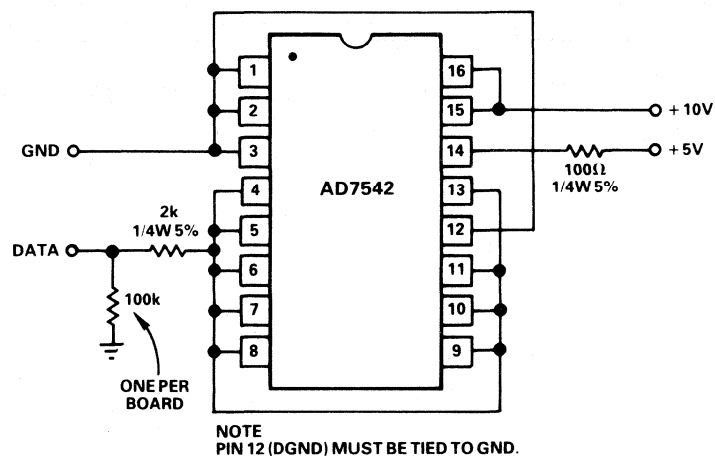


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



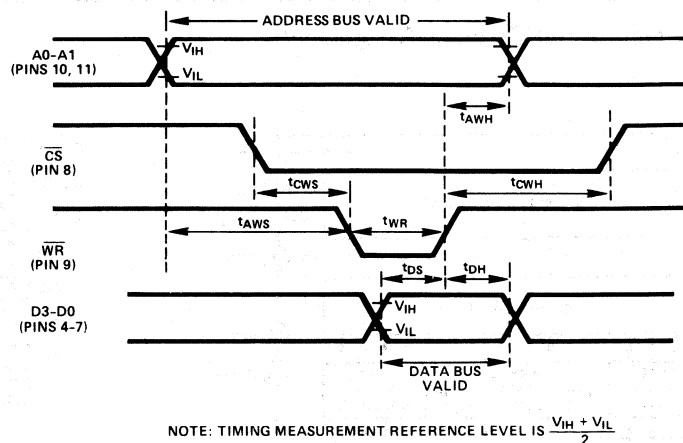


Figure 1. Timing Diagram

AD7542 Control Inputs					AD7542 Operation	
A ₁	A ₀	$\overline{\text{CS}}$	$\overline{\text{WR}}$	$\overline{\text{CLR}}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0		1	Load LOW Byte ⁵ Data Register On Edge As Shown	Load Applicable Data Register With Data At D ₀ – D ₃
0	1	0		1	Load MIDDLE Byte ⁵ Data Register On Edge As Shown	
1	0	0		1	Load HIGH Byte ⁵ Data Register On Edge As Shown	
1	1	0		1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers ⁶	

NOTES:

¹ 1 indicates logic HIGH

² 0 indicates logic LOW

³ X indicates don't care

⁴  indicates LOW to HIGH transition

⁵MSB → XXXX XXXX XXXX ← LSB
 high middle low
 byte byte byte

⁶ These control signals are level triggered.

Table 2. Truth Table



CMOS Serial Input 12-Bit DAC

AD7543

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12-bit multiplying digital-to-analog converter designed for serial interface applications.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7543S(X)/883B
-2	AD7543T(X)/883B
-3	AD7543GT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND (Pins 4-11, 13)	-0.3V, +15V
V_{PIN1} , V_{PIN2} to AGND	-0.3V, +15V
V_{REF} to AGND	$\pm 25\text{V}$
V_{RFB} to AGND	$\pm 25\text{V}$
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

AD7543 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2, 3	12					Bits
Relative Accuracy	RA	– 1	1	1	1			± LSB max
		– 2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	– 1	2	2	2		Monotonic to 11 Bit from T_{min} to T_{max}	± LSB max
		– 2, 3	1	2	1	1	Monotonic to 12 Bit from T_{min} to T_{max}	
Gain Error ²	AE	– 1, 2	14.5	12.3	14.5			± LSB max
		– 3	2	12.3	2	1		
Gain Tempco	TC _{AE}	– 1, 2, 3	5					± ppm/°C max
Supply Rejection (Δ Gain/ Δ V _{DD})	PSRR	– 1, 2, 3	0.01	0.005	0.01		Δ V _{DD} = ± 5%	± % per % max
Output Leakage Current I _{OUT1} (Pin 4)	I _{OUT1}	– 1, 2, 3	200	± 10	200		DAC Registers Loads with All 0's	± nA max
I _{OUT2} (Pin 5)	I _{OUT2}	– 1, 2, 3	200	± 10	200		DAC Register Loads with All 1's	
Output Current Settling Time	t _{SL}	– 1, 2, 3	2				To ± 1/2LSB R _{OUT1} = 100Ω, C _{OUT1} = 13pF DAC. Output Measured from Falling Edge of LD1 and LD2.	µs max
Feedthrough Error ³	FTE	– 1, 2, 3	2.5				V _{REF} = 10V, 10kHz Sinewave	mV p-p max
Reference Input Resistance (Pin 15)	R _{IN}	– 1, 2, 3	8	8	8			kΩ min
			25	25	25			kΩ max
Digital Input High Voltage	V _{IH}	– 1, 2, 3	3.0	3.0	3.0			V min
Digital Input Low Voltage	V _{IL}	– 1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	– 1, 2, 3	1	1	1		V _{IN} = 0V or V _{DD}	± µA max
Digital Input Capacitance	C _{IN}	– 1, 2, 3	8					pF max
Output Capacitance C _{OUT1} (Pin 1)	C _{OUT1}	– 1, 2, 3	260				Digital Inputs = V _{IH} . DAC Register Loaded with 1111 1111 1111	pF max
C _{OUT2} (Pin 2)	C _{OUT2}	– 1, 2, 3	75				Digital Inputs = V _{IH} . DAC Register Loaded with 1111 1111 1111	pF max
C _{OUT1} (Pin 1)	C _{OUT1}	– 1, 2, 3	75				Digital Inputs = V _{IL} . DAC Register Loaded with 0000 0000 0000	pF max
C _{OUT2} (Pin 2)	C _{OUT2}	– 1, 2, 3	260				Digital Inputs = V _{IL} . DAC Register Loaded with 0000 0000 0000	pF max
Serial Input to Strobe Setup Time ⁴	t _{DS1}	– 1, 2, 3	100				STB1 Used as a Strobe	ns min
	t _{DS4}	– 1, 2, 3	0				STB4 Used as a Strobe	
	t _{DS3}	– 1, 2, 3	0				STB3 Used as a Strobe	
	t _{DS2}	– 1, 2, 3	40				STB2 Used as a Strobe	
Serial Input to Strobe Hold Time ⁴	t _{DH1}	– 1, 2, 3	70				STB1 Used as a Strobe	ns min
	t _{DH4}	– 1, 2, 3	250				STB4 Used as a Strobe	
	t _{DH3}	– 1, 2, 3	250				STB3 Used as a Strobe	
	t _{DH2}	– 1, 2, 3	200				STB2 Used as a Strobe	
	t _{SR1}	– 1, 2, 3	160				SR1 Data Pulse Width ⁴	
	t _{STB1}	– 1, 2, 3	160				STB1 Pulse Width ⁴	
	t _{STB4}	– 1, 2, 3	230				STB4 Pulse Width ⁴	
	t _{STB3}	– 1, 2, 3	230				STB3 Pulse Width ⁴	
	t _{STB2}	– 1, 2, 3	180				STB2 Pulse Width ⁴	
	t _{LD1} , t _{LD2}	– 1, 2, 3	300				Min Time Between Strobing LSB into Register A and Loading Register B ⁴	
	t _{ASB}	– 1, 2, 3	80				Min Time Between Strobing LSB into Register A and Loading Register B ⁴	
	t _{CLR}	– 1, 2, 3	400				CLK Pulse Width ⁴	

NOTES

¹V_{DD} = +5V; V_{OUT1} = V_{OUT2} = 0V, V_{REF} = +10V unless otherwise stated.

²Measured using internal feedback resistor and includes the effect of 5ppm max gain TC.

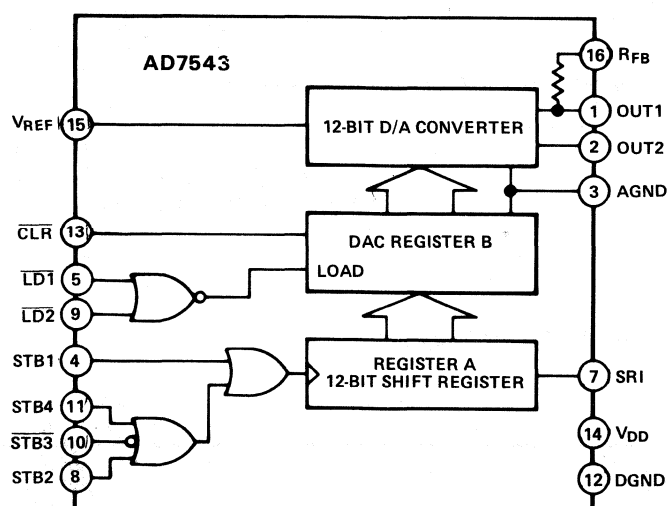
³Feedthrough can be further reduced by connecting the metal lid to ground.

⁴Timing per Figure 1.

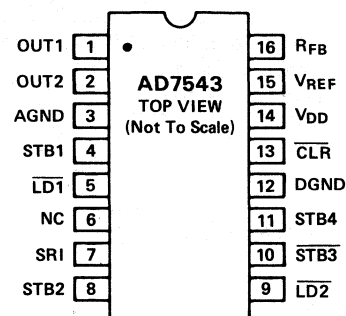
Table 1.

REV. C

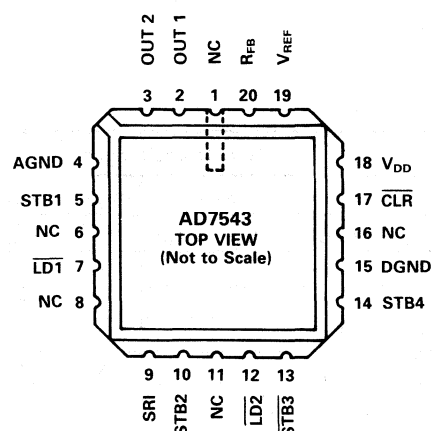
3.2.1 Functional Block Diagram and Terminal Assignments.



DIP (Q) Package



LCC (E) Package

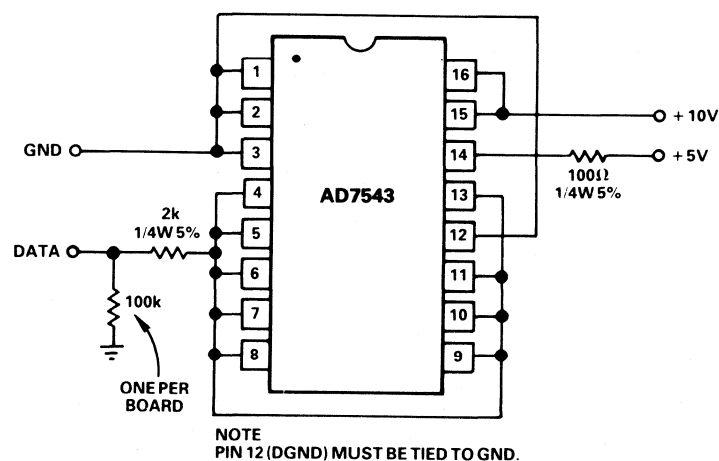


3.2.4 Microcircuit Technology Group.

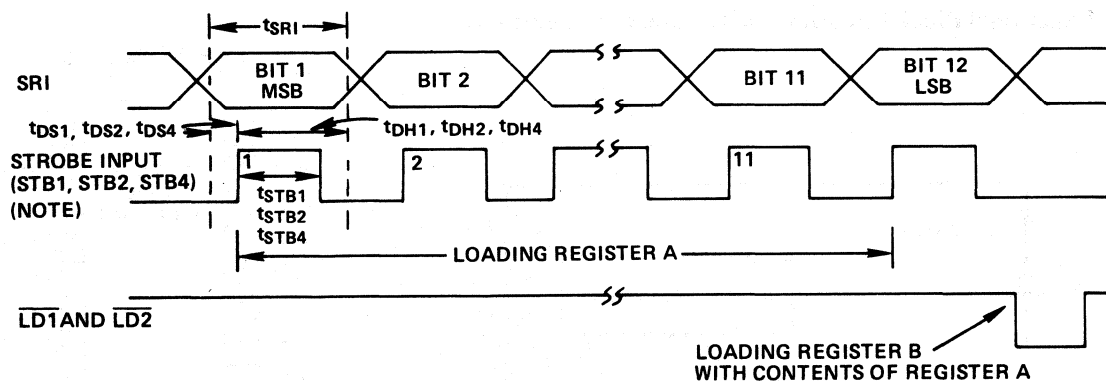
This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7543



NOTE:
STROBE WAVEFORM IS INVERTED IF
STB3 IS USED TO STROBE SERIAL DATA
BITS INTO REGISTER A.

Figure 1. Timing Diagram

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0		X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1		0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0		0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:

1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown is positive edge is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table 2. Truth Table

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit systems. The AD7545 can be used with any supply voltage from +5V to +15V.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7545S(X)/883B
-2	AD7545T(X)/883B
-3	AD7545U(X)/883B
-4	AD7545GU(X)/883B

NOTE:

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V _{REF} to GND	−0.3, +17V
Digital Input Voltage to DGND	−0.3V to V _{DD}
V _{RFB} , V _{REF} to DGND	±25V
V _{PIN1} to DGND	−0.3V to V _{DD}
AGND to DGND	−0.3V, V _{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-20 and E-20A
 θ_{JA} = 120°C/W for Q-20 and E-20A

AD7545 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	- 1, 2, 3, 4	12					Bits
Relative Accuracy	RA	- 1	2	2	2			$\pm$ LSB max
		- 2	1	2	1	1		
		- 3, 4	1/2	2	1/2	1/2		
Differential Nonlinearity	DNL	- 1	4	4	4		10-Bit Monotonic T_{min} to T_{max}	$\pm$ LSB max
		- 2, 3, 4	1	4	1	1	12-Bit Monotonic T_{min} to T_{max}	
Gain Error ²	AE	- 1	25	25	25		DAC Register Loaded with 1111 1111 1111.	$\pm$ LSB max
		- 2	15	25	15	15		
		- 3	10	25	10	10		
		- 4	7	25	7	6		
Gain Tempco	TC _{AE}	- 1, 2, 3, 4	10					$\pm$ ppm/ $^{\circ}$ C max
Power Supply Rejection	PSRR	- 1, 2, 3, 4	0.02	0.01	0.02		$\Delta V_{DD} = \pm 5\%$	$\pm$ %/% max
Output Leakage Current Pin 1	OUT1	- 1, 2, 3, 4	200	10	200		DB0-DB11 = 0V; $\overline{WR}, \overline{CS} = 0V$	$\pm$ nA max
Output Current Settling Time	t _{SL}	- 1, 2, 3, 4	2				To $\pm 1/2$ LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS} = 0V$. $\overline{CS} = 0V$.	μ s max
Feedthrough Error ³	FT	- 1, 2, 3, 4	10				$V_{REF} = \pm 10V$, 10kHz Sinewave	mV p-p max
Reference Input Resistance Pin 19 to Ground	R _{IN}	- 1, 2, 3, 4	7	7	7			k Ω min
			25	25	25			k Ω max
Digital Input High Voltage	V _{IH}	- 1, 2, 3, 4	13.5	13.5	13.5			V min
Digital Input Low Voltage	V _{IL}	- 1, 2, 3, 4	1.5	1.5	1.5			V max
Digital Input Leakage Current	I _{IN}	- 1, 2, 3, 4	10	1	10		$V_{IN} = 0V$ or V_{DD}	$\pm$ μ A max
Digital Input Capacitance DB0-DB11 $\overline{WR}, \overline{CS}$	C _{IN}	- 1, 2, 3, 4	5				$V_{IN} = 0$	pF max
			20					
Output Capacitance	C _{OUT1}	- 1, 2, 3, 4	70				DB0-DB11 = 0V, $\overline{WR}, \overline{CS} = 0V$	pF max
			200				DB0-DB11 = V_{DD} , $\overline{WR}, \overline{CS} = 0V$	
Chip Select to Write Setup Time ⁴	t _{CS}	- 1, 2, 3, 4	200					ns min
Chip Select to Write Hold Time ⁴	t _{CH}	- 1, 2, 3, 4	0					ns min
Write Pulse Width ⁴	t _{WR}	- 1, 2, 3, 4	240				$t_{CS} \geq t_{WR}, t_{CH} \geq 0$	ns min
Data Setup Time ⁴	t _{DS}	- 1, 2, 3, 4	120					ns min
Data Hold Time ⁴	t _{DH}	- 1, 2, 3, 4	30					ns min
Supply Current from V_{DD}	I _{DD}	- 1, 2, 3, 4	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max
			500	100	500		All Digital Inputs 0 or V_{DD} .	μ A max

NOTES

¹ $V_{OUT1} = 0V$; $V_{REF} = +10V$, AGND = DGND unless otherwise stated.

²Measured using internal feedback resistor and includes effect of 5ppm max gain TC.

³Feedthrough error can be reduced by connecting the metal lid to ground.

⁴Timing per Figure 1.

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Resolution	RES	-1, 2, 3, 4	12					Bits
Relative Accuracy	RA	-1	2	2	2			$\pm$ LSB max
		-2	1	2	1	1		
		-3, 4	1/2	2	1/2	1/2		
Differential Nonlinearity	DNL	-1	4	4	4		10-Bit Monotonic T_{min} to T_{max}	$\pm$ LSB max
		-2, 3, 4	1	4	1	1	12-Bit Monotonic T_{min} to T_{max}	
Gain Error ²	AE	-1	20	20	20		DAC Register Loaded with 1111 1111 1111.	$\pm$ LSB max
		-2	10	20	10	10		
		-3	6	20	6	5		
		-4	2	20	2	1		
Gain Tempco	TC_{AE}	-1, 2, 3, 4	5					$\pm$ ppm/ $^{\circ}C$ max
Power Supply Rejection	PSRR	-1, 2, 3, 4	0.03	0.015	0.03		$\Delta V_{DD} = \pm 5\%$	$\pm$ %/% max
Output Leakage Current Pin 1	OUT1	-1, 2, 3, 4	200	10	200		$\overline{DB0}-\overline{DB11} = 0V$; $\overline{WR}, \overline{CS} = 0V$	$\pm$ nA max
Output Current Settling Time	t_{SL}	-1, 2, 3, 4	2				To $\pm 1/2$ LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS} = 0V$.	μs max
Feedthrough Error ³	FT	-1, 2, 3, 4	10				$V_{REF} = \pm 10V$, 10kHz Sinewave	mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2, 3, 4	7	7	7			k Ω min
			25	25	25			k Ω max
Digital Input High Voltage	V_{IH}	-1, 2, 3, 4	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2, 3, 4	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2, 3, 4	10	1	10		$V_{IN} = 0V$ or V_{DD}	$\pm$ μA max
Digital Input Capacitance $\overline{DB0}-\overline{DB11}$ $\overline{WR}, \overline{CS}$	C_{IN}	-1, 2, 3, 4	5				$V_{IN} = 0$	pF max
		-1, 2, 3, 4	20				$V_{IN} = 0$	pF max
Output Capacitance	C_{OUT1}	-1, 2, 3, 4	70				$\overline{DB0}-\overline{DB11} = 0V$, $\overline{WR}, \overline{CS} = 0V$	pF max
			200				$\overline{DB0}-\overline{DB11} = V_{DD}$, $\overline{WR}, \overline{CS} = 0V$	
Chip Select to Write Setup Time ⁴	t_{CS}	-1, 2, 3, 4	380					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1, 2, 3, 4	0					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2, 3, 4	400				$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns min
Data Setup Time ⁴	t_{DS}	-1, 2, 3, 4	210					ns min
Data Hold Time ⁴	t_{DH}	-1, 2, 3, 4	30					ns min
Supply Current from V_{DD}	I_{DD}	-1, 2, 3, 4	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max
			500	100	500		All Digital Inputs 0 or V_{DD} .	μA max

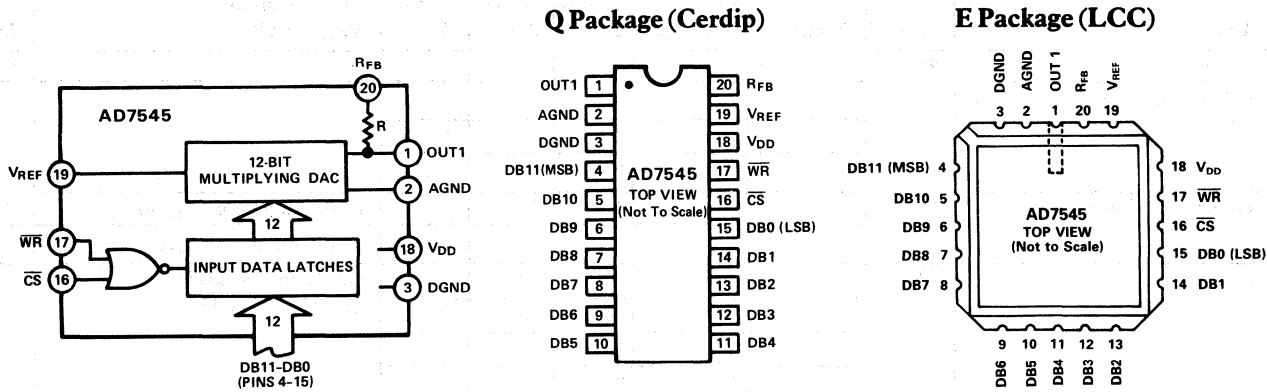
NOTES

¹ $V_{OUT1} = 0V$; $V_{REF} = +10V$, AGND = DGND unless otherwise stated.²Measured using internal feedback resistor and includes effect of 5ppm max gain TC.³Feedthrough error can be reduced by connecting the metal lid to ground.⁴Timing per Figure 1.

Table 2.

AD7545

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

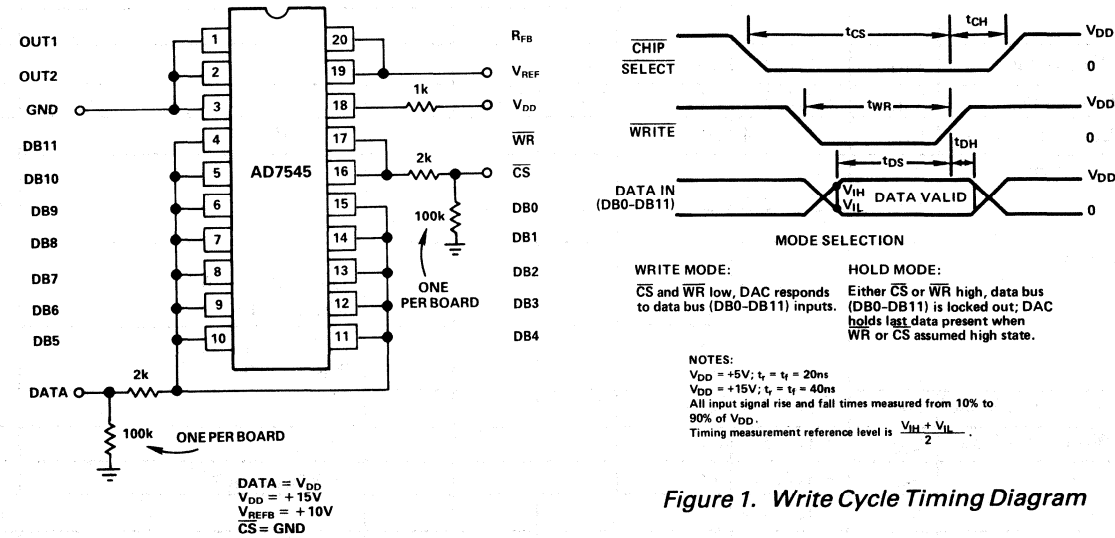


Figure 1. Write Cycle Timing Diagram

MODE SELECTION	
WRITE MODE: CS and WR low, DAC responds to data bus (DB0-DB11) inputs.	HOLD MODE: Either CS or WR high, data bus (DB0-DB11) is locked out; DAC holds last data present when WR or CS assumed high state.

NOTES:
 $V_{DD} = +5V$; $t_r = t_f = 20ns$
 $V_{DD} = +15V$; $t_r = t_f = 40ns$
All input signal rise and fall times measured from 10% to 90% of V_{DD} .
Timing measurement reference level is $V_{IH} + V_{IL} / 2$.

Table 3. Write Mode Selection

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to 12- and 16-bit microprocessor based systems. The AD7545A is an improved version of the AD7545 and will operate with any supply voltage from +5 V to +15 V.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number ¹
-1	AD7545AT(X)/883B
-2	AD7545AU(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	 -0.3 V, +17 V
Digital Input Voltage to DGND	 -0.3 V, $V_{DD} + 0.3$ V
V_{RFB} , V_{REF} to DGND	 +25 V
V_{PIN1} to DGND	 -0.3 V, $V_{DD} + 0.3$ V
AGND to DGND	 -0.3 V, $V_{DD} + 0.3$ V
Power Dissipation to $+75^\circ\text{C}$	 450 mW
Derates above $+75^\circ\text{C}$ by	 6 mW/ $^\circ\text{C}$
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$
Storage Temperature	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	 $+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-20 and E-20A

AD7545A – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}/T_{max}	Sub Group 1	Sub Group 2, 3	Test Conditions/Comments $V_{DD} = +5\text{ V}$	Units
Resolution	RES	–1, 2	12				Bits
Relative Accuracy	RA	–1, 2	1/2	1/2	1/2		±LSB max
Differential Nonlinearity	DNL	–1, 2	1	1	1	12-Bit Monotonic T_{min} to T_{max}	±LSB max
Gain Error ²	A_E	–1	4	3	4	DAC Register Loaded with 1111 1111 1111	±LSB max
		–2	2	1	2		
Gain Tempco	TC_{AE}	–1, 2	5				±ppm/°C max
Power Supply Rejection	PSRR	–1, 2	0.004	0.002	0.004	$V_{DD} = \pm 5\%$	±%/ % max
Output Leakage Current	OUT1	–1, 2	200	10	200	$DB0-DB11 = 0\text{ V}$; $\overline{WR}, \overline{CS} = 0\text{ V}$	±nA max
Output Current Settling Time	t_{SL}	–1, 2	1			To +1/2 LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS} = 0\text{ V}$	µs max
Feedthrough Error	FT	–1, 2	10				mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	–1, 2	10	10	10		k min
			20	20	20		k max
Digital Input High Voltage	V_{IH}	–1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{IL}	–1, 2	0.8	0.8	0.8		V max
Digital Input Leakage Current	I_{IN}	–1, 2	10	1	10	$V_{IN} = 0\text{ V}$ or V_{DD}	±µA max
Digital Input Capacitance	C_{IN}	–1, 2	8			$DB0-DB11$; $\overline{WR}, \overline{CS}$	pF max
			15				
Output Capacitance	C_{OUT1}	–1, 2	70			$DB0-DB11 = 0\text{ V}$, $\overline{WR}, \overline{CS} = 0\text{ V}$	pF max
			150			$DB0-DB11 = V_{DD}$; $\overline{WR}, \overline{CS} = 0\text{ V}$	
Chip Select to Write Setup Time ³	t_{CS}	–1, 2	170			$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns min
Chip Select to Write Hold Time ³	t_{CH}	–1, 2	0				
Write Pulse Width ³	t_{WR}	–1, 2	170				
Data Setup Time ³	t_{DS}	–1, 2	150				
Data Hold Time ³	t_{DH}	–1, 2	5				
Supply Current from V_{DD}	I_{DD}	–1, 2	2	2	2	All Digital Inputs V_{IL} or V_{IH}	mA max
			100	100	100	All Digital Inputs 0 or V_{DD}	µA max

NOTES

¹ $V_{OUT1} = 0\text{ V}$, $V_{REF} = +10\text{ V}$, AGND = DGND unless otherwise stated.

²Measured using internal feedback resistor.

³Timing per Figure 1.

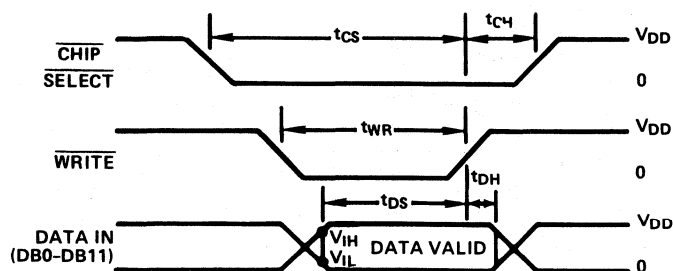
Table 1.

Test	Symbol	Device	Design Limit T_{min}/T_{max}	Sub Group 1	Sub Group 2, 3	Test Conditions/Comments $V_{DD} = +15\text{ V}$	Units
Resolution	RES	-1, 2	12				Bits
Relative Accuracy	RA	-1, 2	1/2	1/2	1/2		$\pm\text{LSB max}$
Differential Nonlinearity	DNL	-1, 2	1	1	1	12-Bit Monotonic T_{min} to T_{max}	$\pm\text{LSB max}$
Gain Error ²	A_E	-1	4	3	4	DAC Register Loaded with 1111 1111 1111	$\pm\text{LSB max}$
		-2	2	1	2		
Gain Tempco	TC_{AE}	-1, 2	5				$\pm\text{ppm}/^\circ\text{C max}$
Power Supply Rejection	PSRR	-1, 2	0.004	0.002	0.004	$V_{DD} = \pm 5\%$	$\pm\%/ \% \text{ max}$
Output Leakage Current	OUT1	-1, 2	200	10	200	DB0-DB11 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V	$\pm\text{nA max}$
Output Current Settling Time	t_{SL}	-1, 2	1			To +1/2 LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$.	$\mu\text{s max}$
Feedthrough Error	FT	-1, 2	10				mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2	10	10	10		k min
			20	20	20		k max
Digital Input High Voltage	V_{IH}	-1, 2	13.5	13.5	13.5		V min
Digital Input Low Voltage	V_{IL}	-1, 2	1.5	1.5	1.5		V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10	$V_{IN} = 0\text{ V or }V_{DD}$	$\pm\mu\text{A max}$
Digital Input Capacitance	C_{IN}	-1, 2	8			DB0-DB11; $\overline{WR}$, $\overline{CS}$	pF max
Output Capacitance	C_{OUT1}	-1, 2	70			DB0-DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0 V	pF max
			150			DB0-DB11 = V_{DD} ; $\overline{WR}$, $\overline{CS}$ = 0 V	
Chip Select to Write Setup Time ³	t_{CS}	-1, 2	95			$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns min
Chip Select to Write Hold Time ³	t_{CH}	-1, 2	0				
Write Pulse Width ³	t_{WR}	-1, 2	95				
Data Setup Time ³	t_{DS}	-1, 2	80				
Data Hold Time ³	t_{DH}	-1, 2	5				
Supply Current from V_{DD}	I_{DD}	-1, 2	2	2	2	All Digital Inputs V_{IL} or V_{IH}	mA max
			100	100	100	All Digital Inputs 0 or V_{DD}	$\mu\text{A max}$

NOTES

¹ $V_{OUT1} = 0\text{ V}$, $V_{REF} = +10\text{ V}$, AGND = DGND unless otherwise stated.²Measured using internal feedback resistor.³Timing per Figure 1.

Table 2.



MODE SELECTION

WRITE MODE:

 $\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.

HOLD MODE:

Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

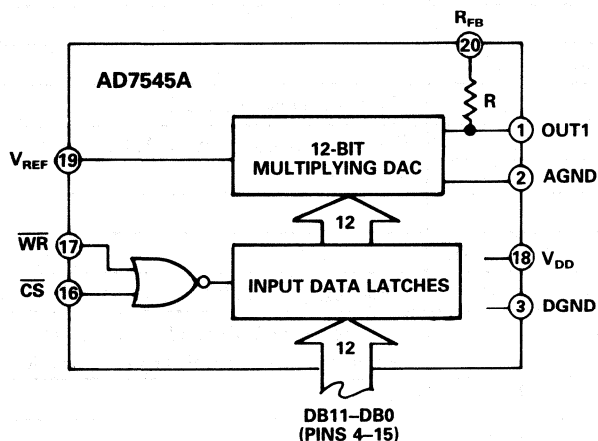
NOTES:

 $V_{DD} = +5\text{ V}$; $t_r = t_f = 20\text{ ns}$ $V_{DD} = +15\text{ V}$; $t_r = t_f = 40\text{ ns}$ All input signal rise and fall times measured from 10% to 90% of V_{DD} .Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

Figure 1. Write Cycle Timing Diagram

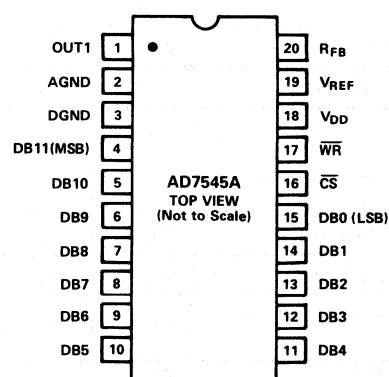
AD7545A

3.2.1 Functional Block Diagram and Terminal Assignments.

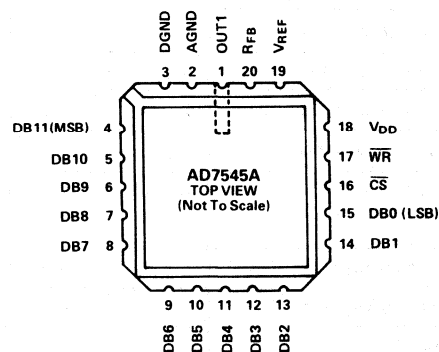


Pin Assignments

Cerdip (Q)



LCC (E)

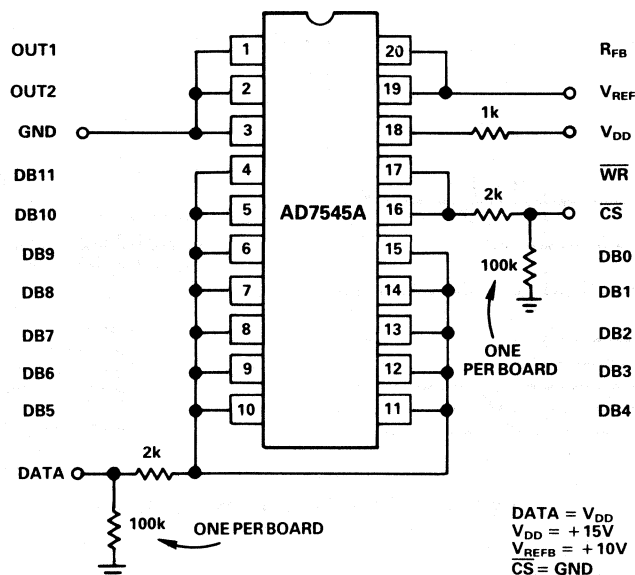


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).



1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12-bit digital-to-analog converter. The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Each D/A converter is preceded by a 12-bit data latch for direct interfacing to 12- and 16-bit microprocessor.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7547S(X)/883B
-2	AD7547T(X)/883B
-3	AD7547U(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3" Width
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted, Pin numbers refer to DIP package)

V_{DD} (Pin 21) to DGND	−0.3V, +17V
V_{REFA} , V_{REFB} (Pins 4, 22) to AGND	±25V
V_{RFBA} , V_{RFBB} (Pins 3, 23) to AGND	±25V
Digital Input Voltage (Pins 5–20) to DGND	−0.3V, $V_{DD} + 0.3V$
V_{PIN2} , V_{PIN24} to DGND	−0.3V, $V_{DD} + 0.3V$
AGND to DGND	−0.3V, $V_{DD} + 0.3V$
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-24 and E-28A

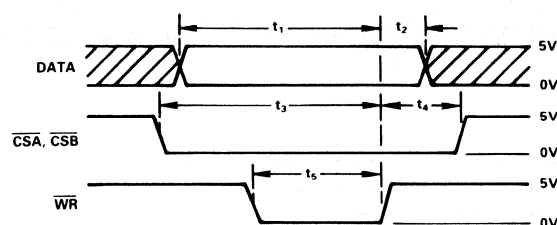
AD7547 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ /Comments	Units
Resolution	RES	– 1, 2, 3	12					Bits
Relative Accuracy	RA	– 1	1	1	1		$V_{DD} = 10.8V$ and $16.5V$	$\pm$ LSB max
		– 2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	– 1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 12 Bits from T_{min} to T_{max} . $V_{DD} = 10.8V$ and $16.5V$.	$\pm$ LSB max
Gain Error	A_E	– 1	6	6	6		Measured Using R_{FA} and R_{FB} . Both DAC Registers Loaded with All 1s. $V_{DD} = 10.8V$.	$\pm$ LSB max
		– 2	3	6	3	3		
		– 3	2	6	2	2		
Gain Temperature Coefficient	dA_E/dT	– 1, 2, 3	5				Typical Value is 1ppm/°C	$\pm$ ppm/°C max
Output Leakage Current (Pin 2)	I_{OUTA}	– 1, 2, 3	250	10	250		DAC A Register Loaded with All 0s; $V_{DD} = 16.5V$	nA max
Output Leakage Current (Pin 24)	I_{OUTB}	– 1, 2, 3	250	10	250		DAC B Register Loaded with All 0s; $V_{DD} = 16.5V$	nA max
Reference Input Resistance (Pin 4, Pin 22)	R_I	– 1, 2, 3	9	9	9		Typical Input Resistance is 14k $V_{DD} = 10.8V$	k Ω min
			20	20	20			k Ω max
Reference Input Resistance Match V_{REFA}, V_{REFB}	RM_{IN}	– 1, 2	3	3	3		Typically $\pm 0.5\%$ $V_{DD} = 10.8V$	$\pm$ % max
		– 3	1	3	1	1		
Digital Input High Voltage	V_{IH}	– 1, 2, 3	2.4	2.4	2.4		$V_{DD} = 10.8V$ and $16.5V$	V min
Digital Input Low Voltage	V_{IL}	– 1, 2, 3	0.8	0.8	0.8		$V_{DD} = 10.8V$ and $16.5V$	V max
Digital Input Current	I_{IN}	– 1, 2, 3	10	1	10		$V_{IN} = V_{DD} = 16.5V$	μ A max
Digital Input Capacitance	C_I	– 1, 2, 3	10					pF max
Power Supply Voltage	V_{DD}	– 1, 2, 3	10.8					V min
			16.5					V max
Power Supply Current	I_{DD}	– 1, 2, 3	2	2	2		$V_{DD} = 16.5V$	mA max
Output Current Settling Time @ 25°C	t_{SL}	– 1, 2, 3	1.5				To 0.01% of Full-Scale Range. I_{OUT} Load = 100. $C_{EXT} = 13pF$. DAC Output Measured from Rising Edge of WR. Typical Value of Settling Time is 0.8 μ s.	μ s max
AC Feedthrough V_{REFA} to I_{OUTA} and V_{REFB} to I_{OUTB}	FT	– 1, 2, 3	65				$V_{REFA}, V_{REFB} = 20V$ p-p 10kHz Sine-Wave DAC Register Loaded with All 0s.	– dB max
Power Supply Rejection Ratio (Δ Gain/ ΔV_{DD})	PSRR	– 1, 2, 3	0.02	0.01	0.02		$\Delta V_{DD} = V_{DD} \text{ max} - V_{DD} \text{ min}$; $V_{DD} = 10.8V$	$\pm$ %/% max
Output Capacitance for DACA and DACB	C_{OUT}	– 1, 2, 3	70				DACA, DACB Loaded with All 0s.	pF max
			140				DACA, DACB Loaded with All 1s.	
Data Setup Time, t_1	t_{DS}	– 1, 2, 3	80					ns min
Data Hold Time, t_2	t_{DH}	– 1, 2, 3	25					ns min
Chip Select to Write Setup Time, t_3	t_{CWS}	– 1, 2, 3	100					ns min
Chip Select to Write Hold Time, t_4	t_{CWH}	– 1, 2, 3	0					ns min
Write Pulse Width, t_5	t_{WR}	– 1, 2, 3	100					ns min

NOTES

¹ $V_{DD} = +12V$ to $+15V \pm 10\%$ except where otherwise stated; $V_{REFA} = V_{REFB} = 10V$; $V_{PIN2} = V_{PIN24} = V_{PIN1} = 0V$. Output amplifiers are AD644.
Pin numbers refer to DIP Package.

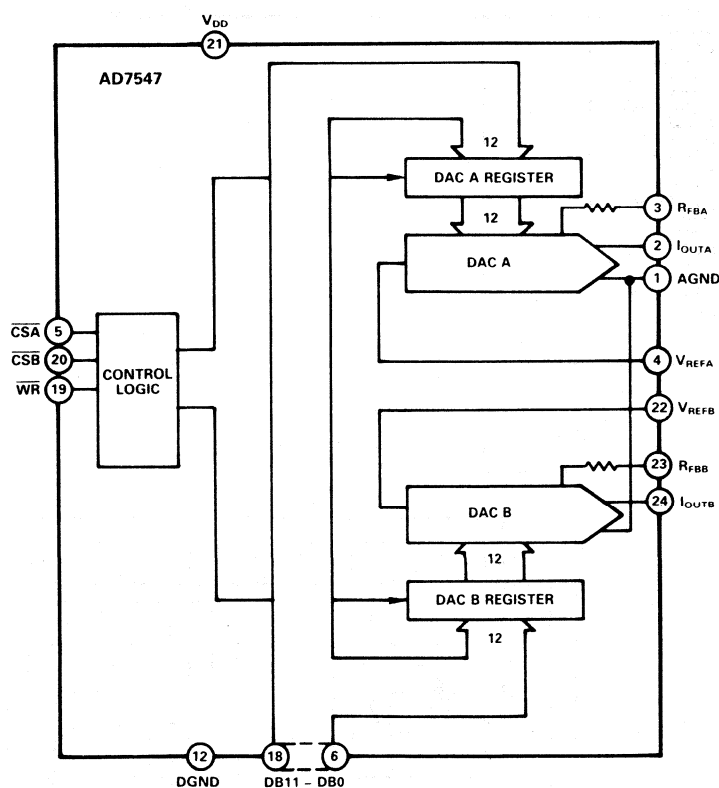
Table 1.



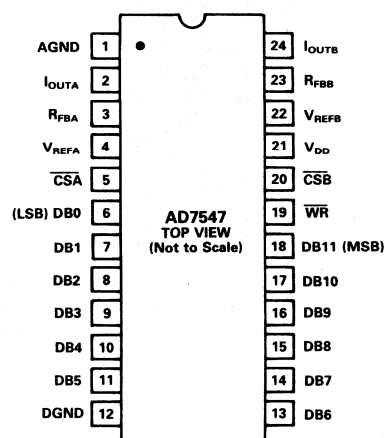
- NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20\text{ns}$.
 2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

Figure 1. Timing Diagram for AD7547

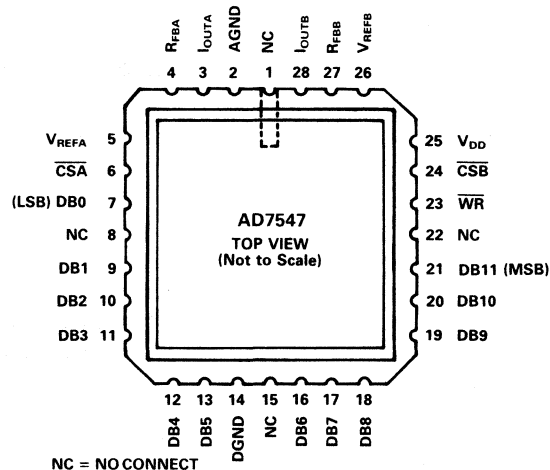
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)



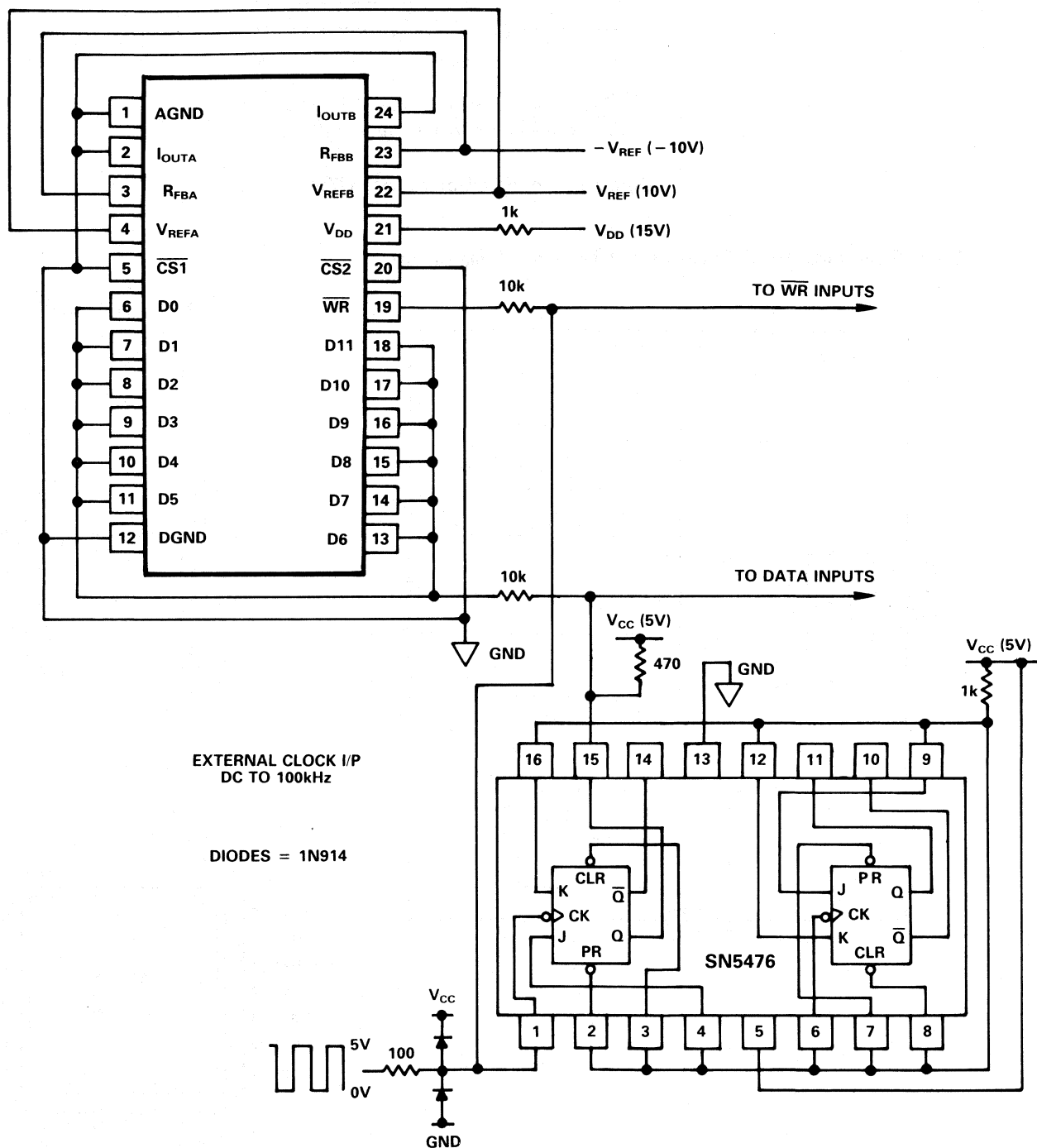
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

AD7547

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Unipolar Binary Operation (2-Quadrant Multiplication)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table 2.

Operational amplifiers A1 and A2 can be in a single package (AD644) or separate packages (AD544, AD OP-27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high-speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7547, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

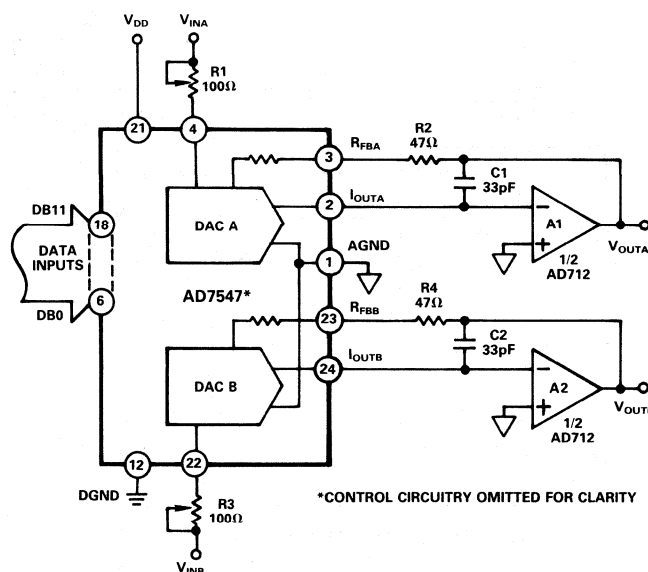


Figure 2. AD7547 Unipolar Binary Operation

Binary Number in DAC Register		Analog Output, V_{OUTA} or V_{OUTB}
MSB	LSB	
1111	1111 1111	$-V_{IN} \left(\frac{4095}{4096} \right)$
1000	0000 0000	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000 0001	$-V_{IN} \left(\frac{1}{4096} \right)$
0000	0000 0000	0V

Table 2. Unipolar Binary Code Table for Circuit of Figure 2

6.0 Bipolar Operation (4-Quadrant Multiplication)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table 3.

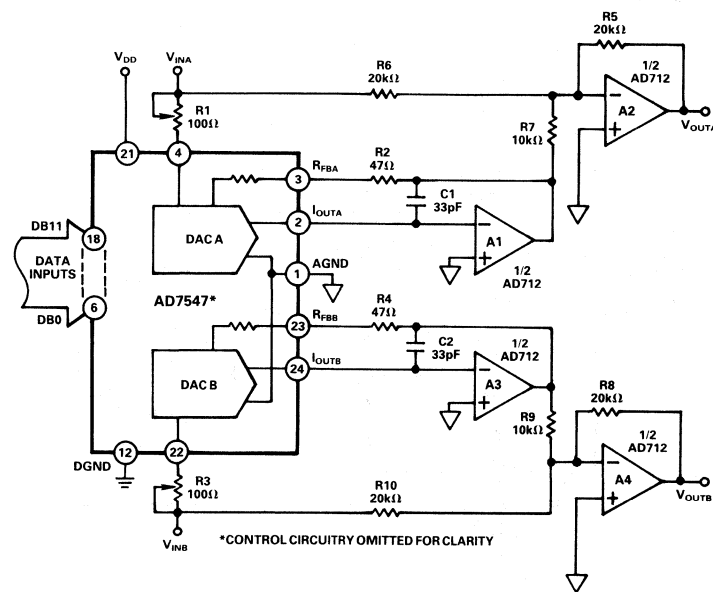


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register		Analog Output, V_{OUTA} or V_{OUTB}
MSB	LSB	
1111	1111 1111	$+V_{IN} \left(\frac{2047}{2048} \right)$
1000	0000 0001	$+V_{IN} \left(\frac{1}{2048} \right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{IN} \left(\frac{1}{2048} \right)$
0000	0000 0000	$-V_{IN} \left(\frac{2048}{2048} \right) = -V_{IN}$

Table 3. Bipolar Code Table for Offset Binary Circuit of Figure 3

1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter for use with 8-bit bus microprocessors. Data is loaded in two bytes, 8 + 4 (high/low byte), to input holding registers. The complete word is then transferred into the DAC register to update the DAC.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7548S(X)/883B
-2	AD7548T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} (Pin 18) to DGND	+17V
V_{REF} (Pin 19) to AGND	$\pm 25\text{V}$
V_{RFB} (Pin 20) to AGND	$\pm 25\text{V}$
Digital Input Voltage (Pins 4–17) to DGND	-0.3V to V_{DD}
V_{PIN1} to DGND	-0.3V , V_{DD}
AGND to DGND	-0.3V , V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-20 and E-20A

AD7548 — SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	-1, 2	12					Bits
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits Over Temperature.	± LSB max
		-2	1/2	1	1/2	1/2		
Gain Error ²	A_E	-1	6	6	6			± LSB max
		-2	3	6	3	3		
Gain Tempco	dA_E/dT	-1, 2	5					± ppm/°C max
Power Supply Rejection	PSRR	-1, 2	0.02				$\Delta V_{DD} = \pm 5\%$	± %/% max
Output Leakage Current Pin 1	I_{OUT}	-1, 2	150	5	150		DAC Register Loaded with All 0's.	± nA max
Output Current Settling Time	t_{SL}	-1, 2	2				To ± 1/2LSB of Full Scale Range. I_{OUT} Load = 100Ω and 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error ³	FTE	-1, 2	10				$V_{REF} = \pm 5V$, 10kHz Sinewave. DAC Register Loaded with All 0's.	mV p-p max
Reference Input Resistance Pin 15	R_I	-1, 2	7	7	7			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10		$V_{IN} = 0V$ or V_{DD} .	± μA max
Digital Input Capacitance	C_I	-1, 2	7					pF max
Output Capacitance Pin 1	C_O	-1, 2	200				DAC Register Loaded with All 1's.	pF max
			100				DAC Register Loaded with All 0's.	
Supply Current from V_{DD}	I_{DD}	-1, 2	3	3	3		All Digital Inputs V_{IL} or V_{IH} .	mA max
			1	1	1		All Digital Inputs 0 or V_{DD} .	mA max
Data Valid Setup Time ⁴	t_{DS}	-1, 2	230					ns min
Data Valid Hold Time ⁴	t_{DH}	-1, 2	50					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$ ⁴ to $\overline{WR}$ Setup Time	t_{CWS}	-1, 2	50					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$ ⁴ to $\overline{WR}$ Hold Time	t_{CWH} ⁴	-1, 2	25					ns min
$\overline{LDAC}$ to $\overline{WR}$ Setup Time ⁴	t_{LWS}	-1, 2	50					ns min
$\overline{LDAC}$ to $\overline{WR}$ Hold Time ⁴	t_{LWH}	-1, 2	25					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2	240					ns min

NOTES

¹ $V_{PIN1} = V_{PIN2} = 0V$, $V_{REF} = +10V$, unless otherwise noted.

²Measured using internal R_{FB} and includes effect of leakage current and gain TC.

³Feedthrough error can be reduced by connecting the metal lid to DGND.

⁴Timing per Figure 1.

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Resolution	RES	-1, 2	12					Bits
Relative Accuracy	RA	-1	1	1	1			$\pm$ LSB max
		-2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits Over Temperature.	$\pm$ LSB max
		-2	1/2	1	1/2	1/2		
Gain Error ²	A_E	-1	6	6	6			$\pm$ LSB max
		-2	3	6	3	3		
Gain Tempco	dA_E/dT	-1, 2	5					$\pm$ ppm/ $^{\circ}C$ max
Power Supply Rejection	PSRR	-1, 2	0.02				$\Delta V_{DD} = \pm 5\%$.	$\pm$ %/% max
Output Leakage Current Pin 1	I_{OUT}	-1, 2	150	5	150		DAC Register Loaded with All 0's.	$\pm$ nA max
Output Current Settling Time	t_{SL}	-1, 2	2				To $\pm 1/2$ LSB of Full Scale Range. I_{OUT} Load = 100 Ω and 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error ³	FTE	-1, 2	10				$V_{REF} = \pm 5V$, 10kHz Sinewave. DAC Register Loaded with All 0's.	mV p-p max
Reference Input Resistance Pin 15	R_I	-1, 2	7	7	7			k Ω min
			20	20	20			k Ω max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10		$V_{IN} = 0V$ or V_{DD} .	$\pm$ μA max
Digital Input Capacitance	C_I	-1, 2	7					pF max
Output Capacitance Pin 1	C_O	-1, 2	200				DAC Register Loaded with All 1's.	pF max
			100				DAC Register Loaded with All 0's.	
Supply Current from V_{DD}	I_{DD}	-1, 2	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max
			300	300	300		All Digital Inputs 0 or V_{DD} .	μA max
Data Valid Setup Time ⁴	t_{DS}	-1, 2	290					ns min
Data Valid Hold Time ⁴	t_{DH}	-1, 2	70					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$ ⁴ to $\overline{WR}$ Setup Time	t_{CWS}	-1, 2	50					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$ ⁴ to $\overline{WR}$ Hold Time	t_{CWH}	-1, 2	25					ns min
$\overline{LDAC}$ to $\overline{WR}$ Setup Time ⁴	t_{LWS}	-1, 2	50					ns min
$\overline{LDAC}$ to $\overline{WR}$ Hold Time ⁴	t_{LWH}	-1, 2	25					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2	320					ns min

NOTES

¹ $V_{PIN1} = V_{PIN2} = 0V$; $V_{REF} = +10V$, unless otherwise stated.

²Measured using internal R_{FB} and includes effect of leakage current and gain TC.

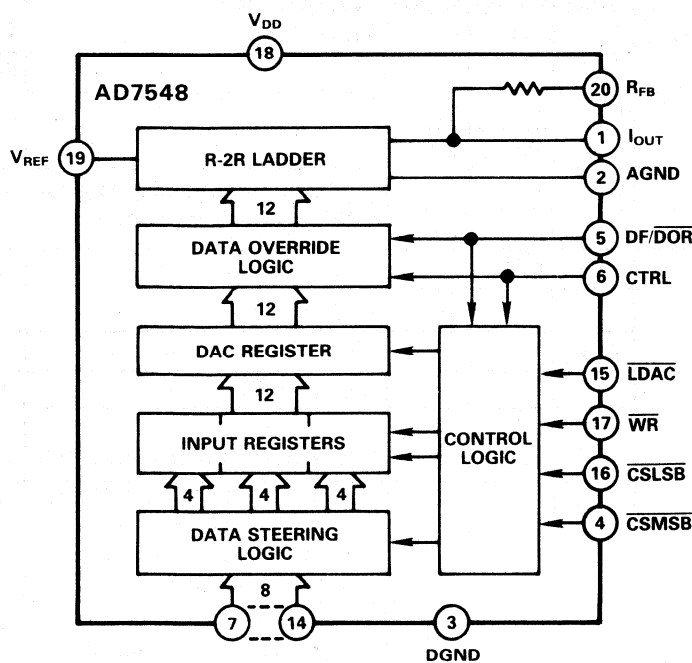
³Feedthrough error can be reduced by connecting the metal lid to DGND.

⁴Timing per Figure 1.

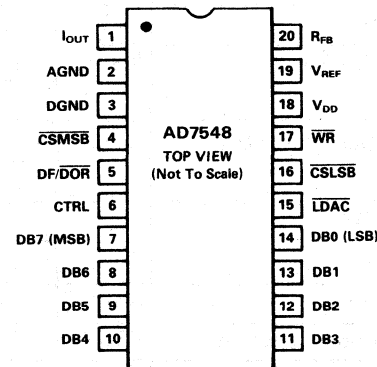
Table 2.

AD7548

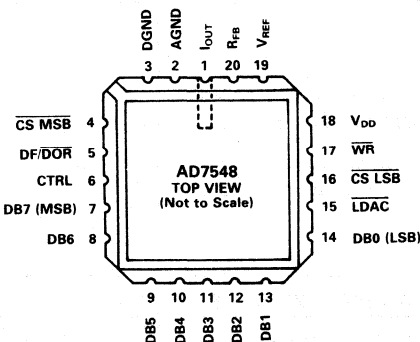
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package



E Package

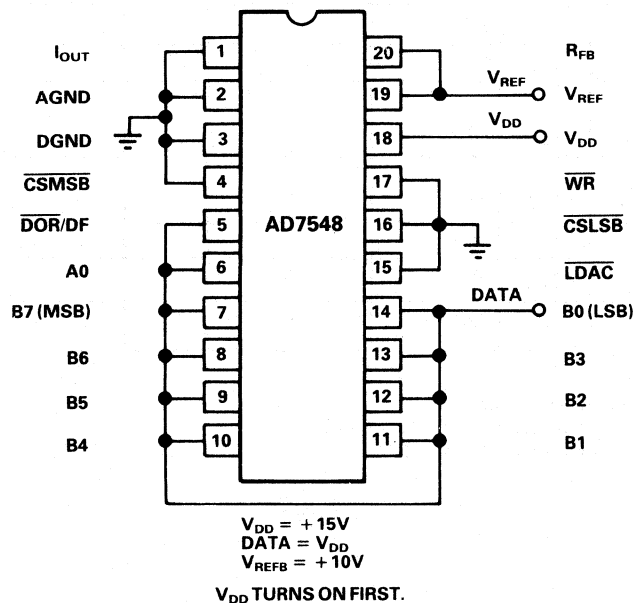


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

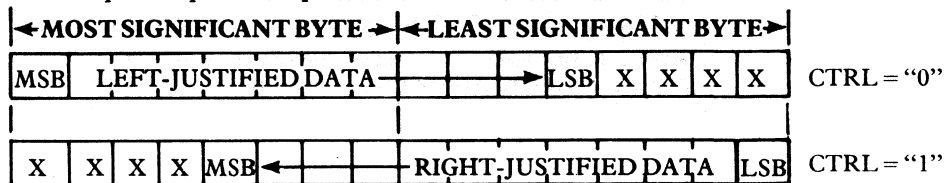


PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	I _{OUT}	DAC current OUT bus. Normally terminated at virtual ground of output amplifier.
2	AGND	Analog Ground.
3	DGND	Digital Ground.
4	CSMSB	Chip Select Most Significant (MS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
5	DF/ $\overline{DOR}$	Data Format/Data Override. When this input is LOW, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/ $\overline{DOR}$ HIGH, CTRL selects either a left or right justified input data format. For normal operation, DF/ $\overline{DOR}$ is held HIGH.

DF/ $\overline{DOR}$	CTRL	FUNCTION
0	0	DAC register contents overridden by all 0's
0	1	DAC register contents overridden by all 1's
1	0	Left-justified input data selected
1	1	Right-justified input data selected

6 CTRL Control Input. See pin 5 description.



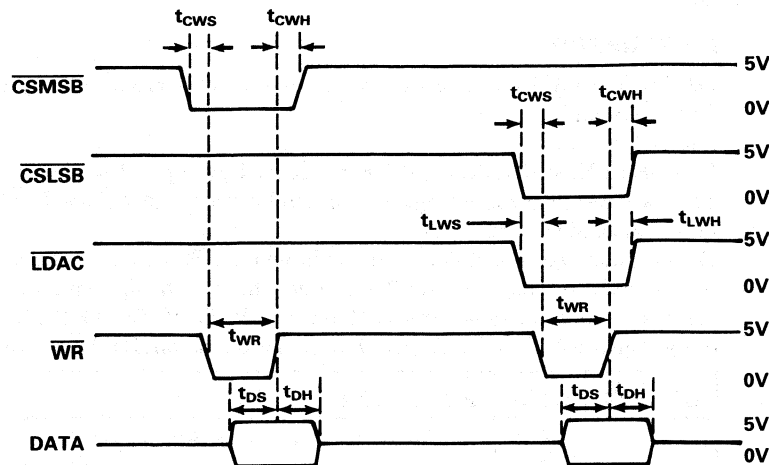
X = Don't care states.

7	DB7	Data Bit 7. Most Significant Bit (MSB).
8	DB6	Data Bit 6.
9	DB5	Data Bit 5.
10	DB4	Data Bit 4.
11	DB3	Data Bit 3.
12	DB2	Data Bit 2.
13	DB1	Data Bit 1.
14	DB0	Data Bit 0. Least Significant Bit (LSB).
15	$\overline{LDAC}$	Load DAC Input, active LOW. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus.
16	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
17	$\overline{WR}$	WRITE Input. This active low signal, in combination with others is used in loading external data into the AD7548 input register and in transferring data from the input register to the DAC register.

$\overline{WR}$	CSMSB	CSLSB	$\overline{LDAC}$	FUNCTION
0	1	0	1	Load LS Byte to Input Register.
0	1	0	0	Load LS Byte to Input Register and DAC Register.
0	0	1	1	Load MS Byte to Input Register.
0	0	1	0	Load MS Byte to Input Register and DAC Register.
0	1	1	0	Load Input Register to DAC Register.
1	X	X	X	No Data Transfer

18	V _{DD}	+5V to +15V Supply Input.
19	V _{REF}	Reference Voltage Input.
20	R _{FB}	Feedback Resistor. Used for normal D/A conversion.

Table 3.



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V.
 $t_r = t_f = 20\text{ns}$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{\text{IH}} + V_{\text{IL}}}{2}$.
3. $\overline{\text{CSMSB}}$ (PIN 4) AND $\overline{\text{CSLSB}}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/DOR = +5V.
FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/DOR = +5V.

Figure 1. Control Input Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a dual 12-bit monolithic, CMOS, current output digital-to-analog converter. Both DACs provide four quadrant multiplication capabilities with a separate reference input and feedback resistor for each DAC. The DACs are each loaded in three 4-bit nibbles.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD7549S(X)/883B
– 2	AD7549T(X)/883B

NOTE

¹See Paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin DIP
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} (Pin 20) to DGND	– 0.3V, + 17V
V_{REFA} , V_{REFB} (Pins 19, 13) to AGND	$\pm 25\text{V}$
V_{RFBA} , V_{RFBB} (Pins 18, 14) to AGND	$\pm 25\text{V}$
Digital Input Voltage (Pins 1-11) to DGND	– 0.3V, V_{DD}
V_{PIN15} , V_{PIN17} , to DGND	– 0.3V, V_{DD}
AGND to DGND	– 0.3V, V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-20 and E-20A

AD7549 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	12					Bits
Relative Accuracy	RA	– 1 – 2	± 1 $\pm 1/2$	± 1 ± 1	± 1 $\pm 1/2$	$\pm 1/2$		LSB max
Differential Nonlinearity	DNL	– 1, 2	± 1	± 1	± 1		Guaranteed Monotonic to 12-Bits	LSB max
Gain Error ²	A _E	– 1 – 2	± 6 ± 3	± 6 ± 6	± 6 ± 3	± 3		LSB max
Gain Tempco	TC _{AE}	– 1, 2	± 5					ppm/°C max
Supply Rejection (Δ Gain/ Δ V _{DD})	PSRR	– 1, 2	± 0.02	± 0.01	± 0.02		Δ V _{DD} = $\pm 5\%$ Full Scale Outputs	% per % max
Output Leakage Current (Pin 17)	I _{OUTA}	– 1, 2	250	20	250		DAC A Register Loaded with All 0's	nA max
(Pin 15)	I _{OUTB}	– 1, 2	250	20	250		DAC B Register Loaded with All 0's	nA max
Output Current Settling Time (@ 25°C)	t _{SL}	– 1, 2	1.5				To 0.01% of FSR. I _{OUT} Load = 100 Ω , C _{EXT} = 13pF. DAC Output Measured from Falling Edge of WR. Typical Value of Settling Time is 0.8 μ s.	μ s max
Feedthrough Error ³ V _{REFA} to I _{OUTA} V _{REFB} to I _{OUTB}	FT	– 1, 2	– 65 – 65				V _{REFA} , V _{REFB} = ± 20 V p-p, 10kHz Sine Wave. DAC Register Loaded with All 0's	dB max
Reference Input Resistance (Pin 19, Pin 13)	R _{IN}	– 1, 2 – 1, 2	7 18	7 18	7 18			k Ω min k Ω max
Reference Input Resistance Match V _{REFA} /V _{REFB}	RM _{IN}	– 1 – 2	± 3 ± 2	± 3 ± 3	± 3 ± 2	± 2		% max
Digital Input High Voltage	V _{IH}	– 1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V max
Input Leakage Current	I _{IN}	– 1, 2	± 10	± 1	± 10		V _{IN} = V _{DD}	μ A max
Input Capacitance	C _{IN}	– 1, 2	7					pF max
Analog Output Capacitance	C _{OUTA} C _{OUTB}	– 1, 2	80 80				DAC A, DAC B Loaded with All 0's	pF max
	C _{OUTA} C _{OUTB}	– 1, 2	160 160				DAC A, DAC B Loaded with All 1's	pF max
Address Valid to Write Setup Time	t _{AWS}	– 1, 2	110					ns min
Address Valid to Write Hold Time	t _{AWH}	– 1, 2	0					ns min
Data Setup Time	t _{DS}	– 1, 2	240					ns min
Data Hold Time	t _{DH}	– 1, 2	0					ns min
Chip Select or Update to Write Setup Time	t _{CWS}	– 1, 2	20					ns min
Chip Select or Update to Write Hold Time	t _{CWH}	– 1, 2	0					ns min
Write Pulse Width	t _{WR}	– 1, 2	250					ns min
Clear Pulse Width	t _{CLR}	– 1, 2	250					ns min
Power Requirements	I _{DD}	– 1, 2	5	5	5			mA max

NOTES

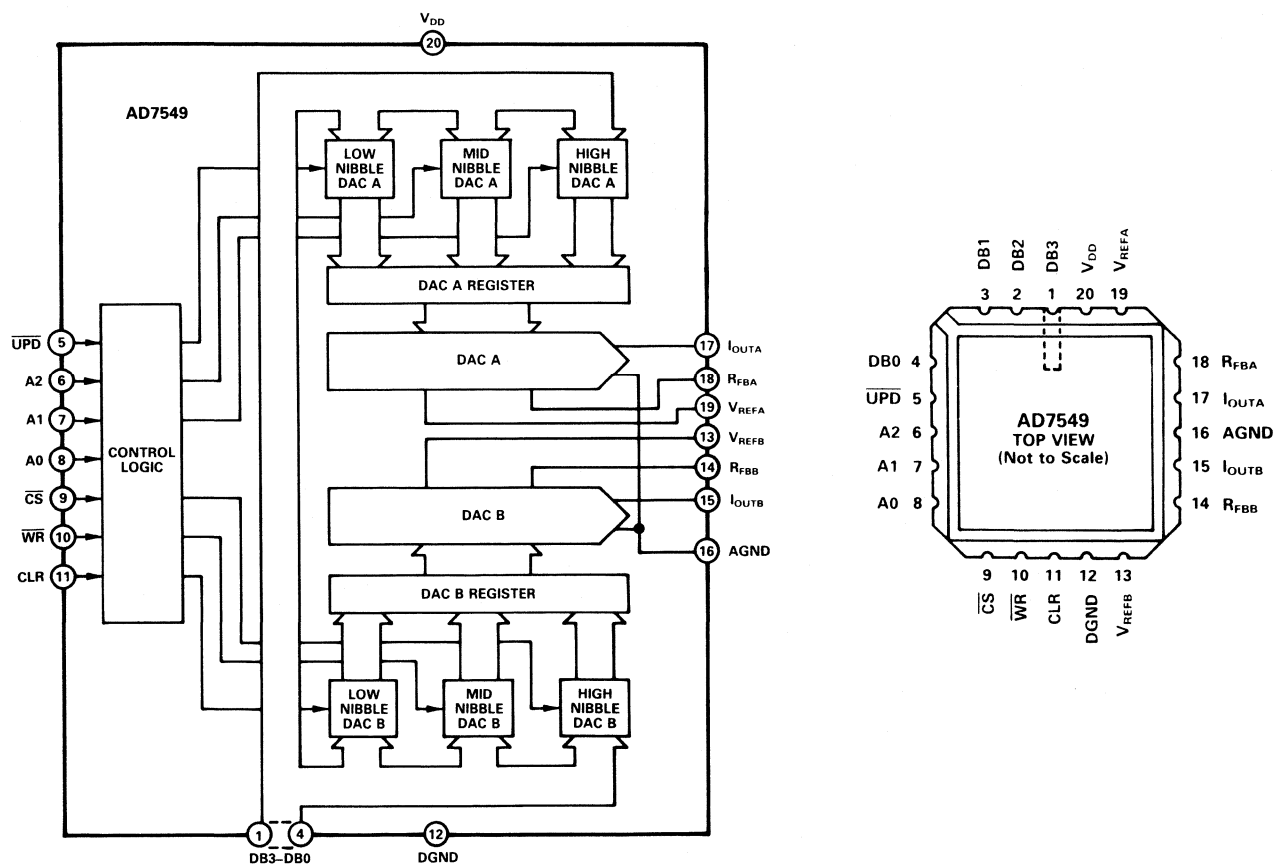
¹V_{DD} = +15V; V_{REFA} = V_{REFB} = +10V, V_{PIN15} = V_{PIN17} = V_{PIN16} = 0V unless otherwise stated.
Specifications are guaranteed for a V_{DD} of +15V with a tolerance of $\pm 5\%$, testing is performed at 15V only, except where stated otherwise.

²Measured using internal feedback resistor and includes effects of leakage current and gain T.C.

³Feedthrough can be further reduced by connecting the metal lid to ground.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

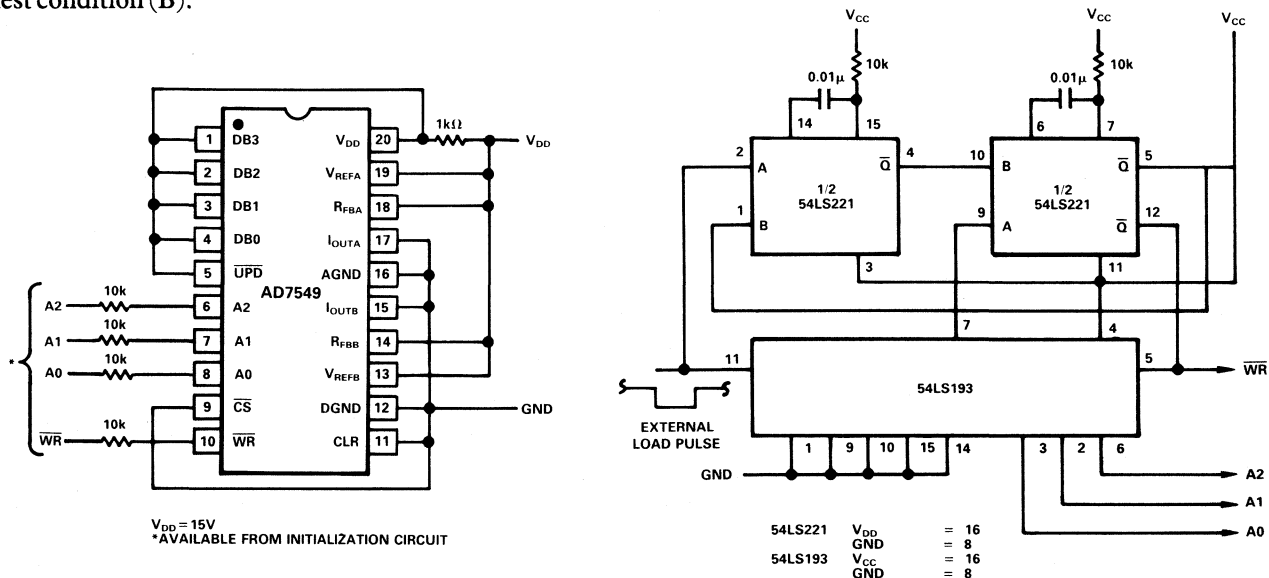


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



INITIALIZATION CIRCUIT

REV. B

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8-bit input/output port. This consists of an 8-bit sampling analog-to-digital converter, an 8-bit digital-to-analog converter with output amplifier, and a common reference and 8-bit parallel data bus.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number
-1	AD7569S(X)/883B
-2	AD7569T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V_{DD} to AGND (DAC or ADC)	-0.3 V, +7 V
V_{DD} to DGND	-0.3 V, +7 V
V_{DD} to V_{SS}	-0.3 V, +14 V
AGND (DAC or ADC) to DGND	-0.3 V, $V_{DD} + 0.3$ V
AGND (DAC) to AGND (ADC)	± 5 V
Logic Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
CLK Input Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
V_{OUT} to AGND (DAC)	$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V
V_{IN} to AGND (ADC)	$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V
Power Dissipation (to $+75^\circ\text{C}$)	450 mW
Derates above $+75^\circ\text{C}$	6 mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-24 and E-28A

AD7569 – SPECIFICATIONS

DAC								
Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ /Comments	Units
Resolution	RES	-1, 2	8				Minimum Resolution for Which No Missing Codes Are Guaranteed.	Bits
Total Unadjusted Error	TUE	-1, 2	3					±LSB typ
Relative Accuracy	INL	-1	1	1	1			±LSB max
		-2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	1	1	1			±LSB max
		-2	3/4	1	3/4	3/4		
Unipolar Offset Error		-1	2.5	2	2.5			±LSB max
		-2	2	2	2	1.5		
Bipolar Zero Offset Error		-1	2.5	2	2.5			±LSB max
		-2	2	2	2	1.5		
Full Scale Error ²		-1	4	2	4			LSB max
		-2	3	2	3	1		
Δ Full Scale/ ΔV_{DD}		-1, 2		1/2			$V_{OUT} = 2.5 \text{ V}; \Delta V_{DD} = \pm 5\%$	±LSB max
Δ Full Scale/ ΔV_{SS}		-1, 2		1/2			$V_{OUT} = -2.5 \text{ V}; \Delta V_{SS} = \pm 5\%$	±LSB max
Signal to Noise Ratio	SNR	-1, 2	46	46	46		$V_{OUT} = 20 \text{ kHz Sine};$ $f_{SAMPLING} = 400 \text{ kHz}$	dB min
Total Harmonic Distortion	THD	-1, 2	48	48	48		$V_{OUT} = 20 \text{ kHz Sine};$ $f_{SAMPLING} = 400 \text{ kHz}$	dB max
Intermodulation Distortion	IMD	-1, 2	55				$f_a = 18.4 \text{ kHz}; f_b = 14.5 \text{ kHz}$ $f_{SAMPLING} = 400 \text{ kHz}$	dB typ
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Unipolar Analog Output Voltage		-1, 2	0 to +1.25/2.5					
Bipolar Analog Output Voltage		-1, 2	±1.25/±2.5					
Input Leakage Current	I_{IN}	-1, 2	10	10	10		$V_{IN} = 0 \text{ to } V_{DD}$	±μA max
Input Capacitance	C_{IN}	-1, 2	10					pF max
Supply Current from V_{DD}	I_{DD}	-1, 2	13	13	13			mA max
Supply Current from V_{SS}	I_{SS}	-1, 2	4	4	4			mA max

NOTES

¹ $V_{DD} = +5 \text{ V} \pm 5\%$, $V_{SS} = \text{RANGE} = \text{AGND}_{DAC} = \text{AGND}_{ADC} = \text{DGND} = 0 \text{ V}$, $f_{CLK} = 5 \text{ MHz}$

²Includes internal voltage reference error and is calculated after offset error has been adjusted out.

Table 1.

ADC								
Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ /Comments	Units
Resolution	RES	-1, 2	8				Minimum Resolution for Which No Missing Codes Are Guaranteed.	Bits
Total Unadjusted Error	TUE	-1, 2	4					±LSB typ
Relative Accuracy	INL	-1	1	1	1			±LSB max
		-2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	1	1	1			±LSB max
		-2	3/4	1	3/4	3/4		
Unipolar Offset Error		-1	3	2	3			±LSB max
		-2	2.5	2	2.5	1.5		
Bipolar Zero Offset Error		-1	4	3	4			±LSB max
		-2	3.5	3	3.5	2.5		
Full Scale Error ²		-1, 2	-7.5	-7.5	-7.5			LSB max
			+2	+2	+2			
Δ Full Scale/ ΔV_{DD}		-1, 2		0.5			$V_{IN} = +2.5 \text{ V}; \Delta V_{DD} = \pm 5\%$	±LSB max
Δ Full Scale/ ΔV_{SS}		-1, 2		0.5			$V_{IN} = -2.5 \text{ V}; \Delta V_{SS} = \pm 5\%$	±LSB max
Signal-to-Noise Ratio	SNR	-1	44	44	44	44	$V_{IN} = 100 \text{ kHz Sine};$ $f_{SAMPLING} = 400 \text{ kHz}$	dB min
		-2	45	44	45	44		
Total Harmonic Distortion	THD	-1, 2	48	48	48		$V_{IN} = 100 \text{ kHz Sine};$ $f_{SAMPLING} = 400 \text{ kHz}$	dB max
Intermodulation Distortion	IMD	-1, 2	60				$f_a = 99 \text{ kHz}; f_b = 96.7 \text{ kHz}$ $f_{SAMPLING} = 400 \text{ kHz}$	dB typ
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Unipolar Analog Input Voltage	V_{INV}	-1, 2	0 to 1.25/+2.5				$V_{DD} = +5 \text{ V}; V_{SS} = 0 \text{ V}$	V
Bipolar Analog Input Voltage	V_{INB}	-1, 2	±1.25/±2.5				$V_{DD} = +5 \text{ V}; V_{SS} = -5 \text{ V}$	V
Input Current	I_{IN}	-1, 2	300	300	300			±μA max
Input Capacitance	C_{IN}	-1, 2	10					pF max
Input Leakage Current	I_{IL}	-1, 2	10	10	10			±μA max
CLK Input Current (High Level)	I_{INH}	-1, 2	40	40	40		$V_{IN} = V_{DD}$	μA max
CLK Input Current (Low Level)	I_{INL}	-1, 2	-1.6	-1.6	-1.6		$V_{IN} = 0 \text{ V}$	mA max
Digital Output Low Voltage	V_{OL}	-1, 2	0.4	0.4	0.4			V max
Digital Output High Voltage	V_{OH}	-1, 2	4.0	4.0	4.0			V min
Floating State Leakage Current	I_{OUT}	-1, 2	10	10	10			±μA max

Table 2. (Continued on next page)

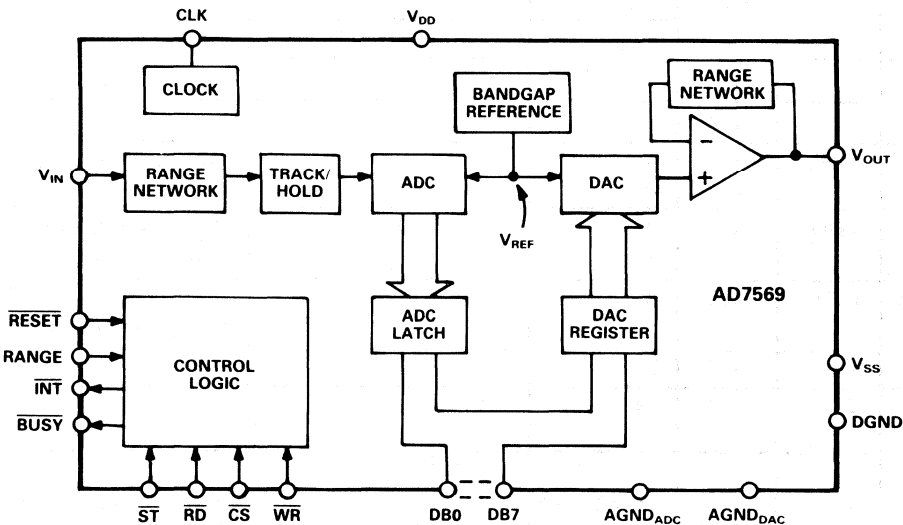
AD7569

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ /Comments	Units
Floating State Output Capacitance	C_{OUT}	-1, 2	10					pF max
Conversion Time (External Clock)	t_{CONV}	-1, 2	2.0	2.0	2.0		$f_{CLK} = 5.0\text{ MHz}$	$\mu\text{s max}$

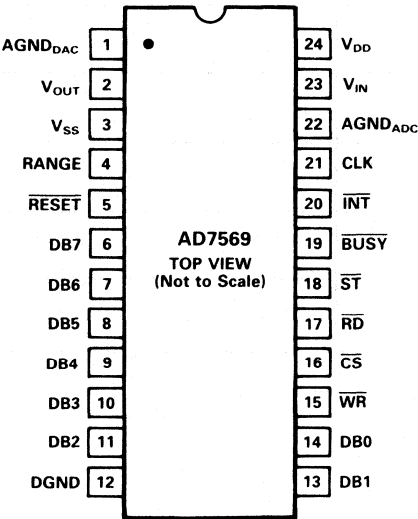
NOTES
¹ $V_{DD} = +5\text{ V} \pm 5\%$, $V_{SS} = \text{RANGE} = \text{AGND}_{DAC} = \text{AGND}_{ADC} = \text{DGND} = 0\text{ V}$, $f_{CLK} = 5\text{ MHz}$
²Includes internal voltage reference error and is calculated after offset error has been adjusted out.

Table 2.

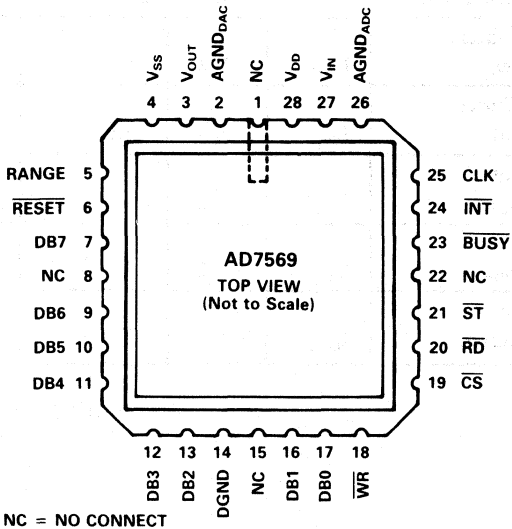
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)



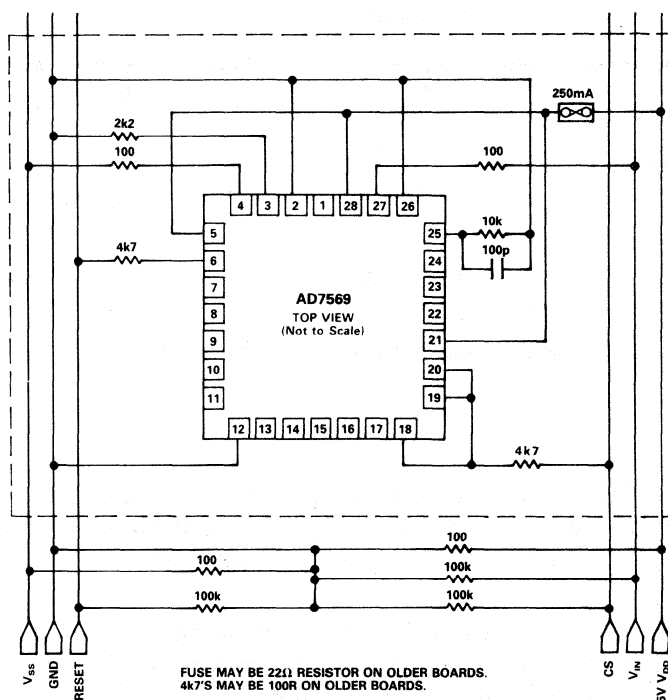
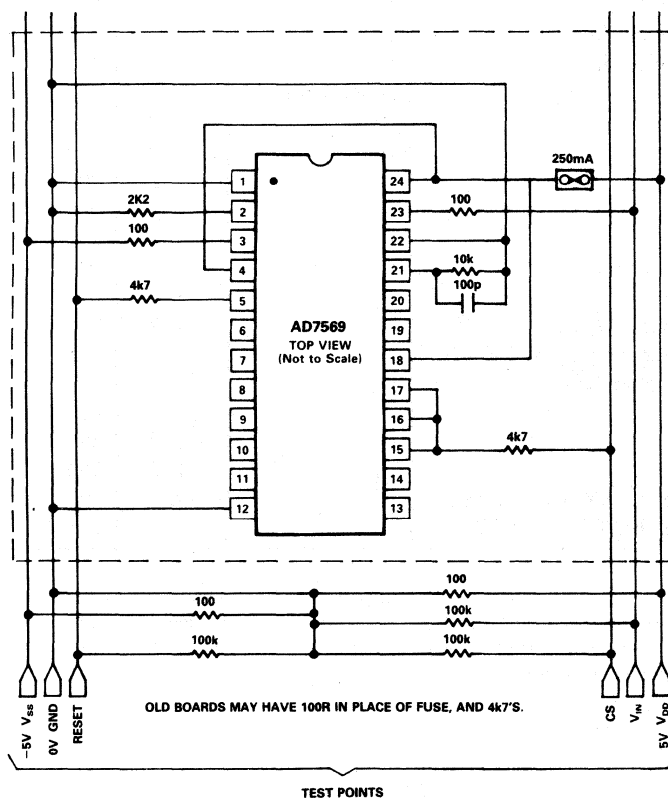
NC = NO CONNECT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7569 TIMING¹

Test	Symbol	Device	Design Limit T_{min} to T_{max}	Units
$\overline{WR}$ Pulse Width	DAC Timing t_1	-1, 2	90	ns min
$\overline{CS}$, $\overline{A/B}$ to $\overline{WRS}$ Setup Time	t_2	-1, 2	0	ns min
$\overline{CS}$, $\overline{A/B}$ to $\overline{WR}$ Hold Time	t_3	-1, 2	0	ns min
Data Valid to $\overline{WR}$ Setup Time	t_4	-1, 2	80	ns min
Data Valid to $\overline{WR}$ Hold Time	t_5	-1, 2	10	ns min
$\overline{ST}$ Pulse Width	ADC Timing t_6	-1, 2	50	ns min
$\overline{ST}$ to $\overline{BUSY}$ Delay	t_7	-1, 2	150	ns max
$\overline{BUSY}$ to $\overline{INT}$ Delay	t_8	-1, 2	30	ns max
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_9	-1, 2	0	ns min
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{10}	-1, 2	0	ns min
$\overline{RD}$ Pulse Width. Determined by t_{13} .	t_{11}	-1, 2	90	ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{12}	-1, 2	0	ns min
Data Access Time after $\overline{RD}$; $C_L = 20$ pF	t_{13}^2	-1, 2	90	ns max
Data Access Time after $\overline{RD}$; $C_L = 100$ pF			135	ns max
Bus Relinquish Time after $\overline{RD}$	t_{14}^3	-1, 2	10	ns min
			85	ns max
$\overline{RD}$ to $\overline{INT}$ Delay	t_{15}	-1, 2	85	ns max
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_{16}	-1, 2	160	ns max
Data Valid Time after $\overline{BUSY}$; $C_L = 20$ pF	t_{17}^2	-1, 2	90	ns max
Data Valid Time after $\overline{BUSY}$; $C_L = 100$ pF			135	ns max

NOTES

¹All input control signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

² t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

³ t_{14} is defined as the time required for the data line to change 0.5 V when loaded with the circuit of Figure 2.

Specifications subject to change without notice.

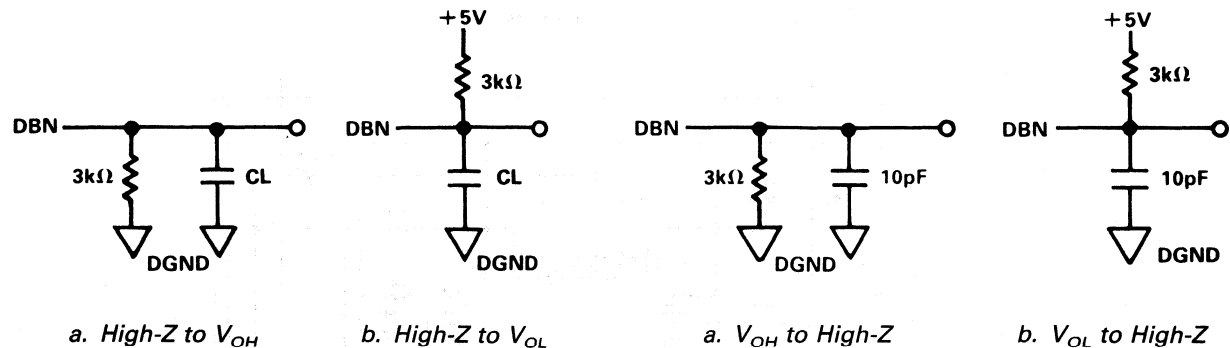


Figure 1. Load Circuits for Data Access Time Test

Figure 2. Load Circuits for Bus Relinquish Time Test

6.0 Digital Section.

The data pins on the AD7569 provide a connection between the external bus and both the DAC data inputs and ADC data outputs. The threshold levels of all digital inputs and outputs are compatible with either TTL or 5 V CMOS levels. Internal input protection of all digital pins is achieved by on-chip distributed diodes.

The data format is straight binary when the part is used in single supply ($V_{SS} = 0$ V). However, when a V_{SS} of -5 V is applied, the data format becomes 2s complement. This data format applies to the digital inputs of the DAC and the digital outputs of the ADC.

6.1 ADC Section.

The analog-to-digital converter on the AD7569 uses the successive approximation technique to achieve a fast conversion time of 2 μ s and provide an 8-bit parallel digital output. The reference for the ADC is provided by the on-chip bandgap reference.

Conversion start is controlled by $\overline{ST}$ or by $\overline{CS}$ and $\overline{RD}$. Once a conversion has been started another conversion start should not be attempted until the conversion in progress is completed. Exercising the $\overline{RESET}$ input does not affect conversion; the $\overline{RESET}$ input resets the $\overline{INT}$ line high which is useful in interrupt-driven systems where a READ has not been performed at the end of the previous conversion. The $\overline{INT}$ line does not have to be cleared at the end of conversion. The ADC will continued to convert correctly but the function of the $\overline{INT}$ line will be affected.

Figure 3 shows the operating waveforms for a conversion cycle. The analog input voltage, V_{IN} , is held 50 ns typical after the falling edge of $\overline{ST}$ or ($\overline{CS}$ & $\overline{RD}$). The MSB decision is made approximately 50 ns after the second falling edge of the input CLK following a conversion start. If t_1 in Figure 3 is greater than 50 ns, then the falling edge of the input CLK will be seen as the first falling clock edge. If t_1 is less than 50 ns, the first falling clock edge of the conversion will not occur until one clock cycle later. The succeeding bit decisions are made approximately 50 ns after a CLK edge until conversion is complete. At the end of conversion, the SAR contents are transferred to the output latch and the SAR is reset in readiness for a new conversion. A single conversion lasts for 8 input clock cycles.

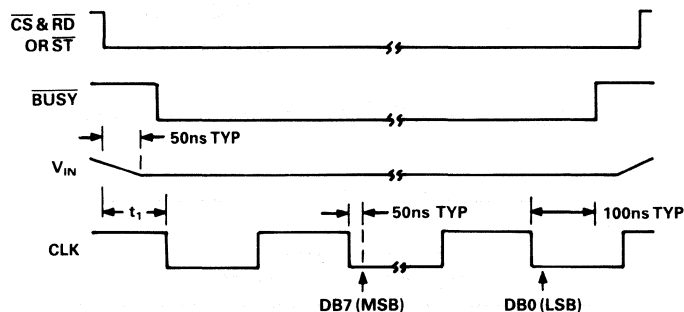


Figure 3. Operating Waveforms Using External Clock

6.2 Digital Interface.

DAC Timing and Control – AD7569

Table 3 shows the truth table for DAC operation for the AD7569. The part contains an 8-bit DAC register which is loaded from the data bus under control of $\overline{CS}$ and $\overline{WR}$. The data contained in the DAC register determines the analog output from the DAC. The $\overline{WR}$ input is an edge-triggered input and data is transferred into the DAC register on the rising edge of $\overline{WR}$. Holding $\overline{CS}$ and $\overline{WR}$ low does not make the DAC register transparent.

$\overline{CS}$	$\overline{WR}$	$\overline{RESET}$	DAC Function
H	H	H	DAC Register Unaffected
L	L	H	DAC Register Unaffected
L	$\uparrow$	H	DAC Register Updated
$\uparrow$	L	H	DAC Register Updated
X	X	L	DAC Register Loaded with All Zeros

L = Low State H = High State X = Don't Care

Table 3. AD7569 DAC Truth Table

The contents of the DAC register are reset to all 0s by an active low pulse on the $\overline{\text{RESET}}$ line and for the unipolar output ranges the output remains at 0 V after $\overline{\text{RESET}}$ returns high. For the bipolar output ranges a low pulse on $\overline{\text{RESET}}$ causes the output to go to negative full scale. In unipolar applications the $\overline{\text{RESET}}$ line can be used to ensure power-up to 0 V on the AD7569 DAC output and is also useful when used as a zero override in system calibration cycles. If the $\overline{\text{RESET}}$ input is connected to the system $\overline{\text{RESET}}$ line, then the DAC output resets to 0 V when the entire system is reset. Figure 4 shows the input control logic for the AD7569 DAC and the write cycle timing diagram is shown in Figure 5.

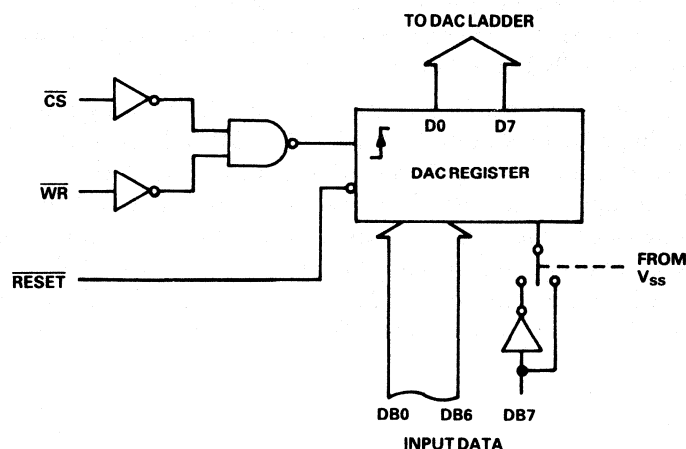
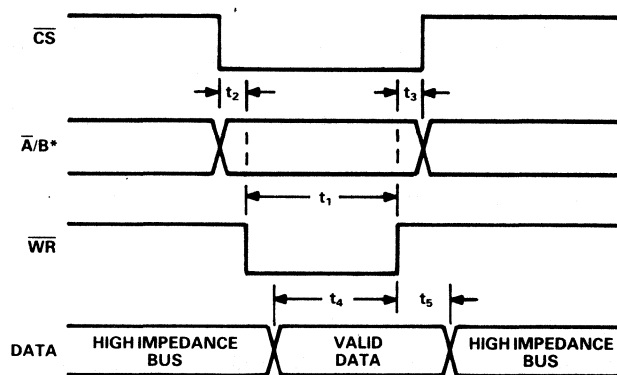


Figure 4. AD7569 DAC Input Control Logic



NOTES

1. ALL INPUT RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V,
 $t_R = t_F = 5\text{ns}$

2. TIMING MEASUREMENT REFERENCE LEVEL IS

$$\frac{V_{\text{INH}} + V_{\text{INL}}}{2}$$

Figure 5. AD7569 Write Cycle Timing Diagram

6.3 ADC Timing and Control.

The ADC on the AD7569 is capable of two basic operating modes. In the first mode the $\overline{\text{ST}}$ line is used to start conversion and drive the track-and-hold into hold mode. At the end of conversion the track-and-hold returns to its tracking mode. The second mode is achieved by hard-wiring the $\overline{\text{ST}}$ line high. In this case, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ start conversion and the microprocessor is driven into a WAIT state for the duration of conversion by $\overline{\text{BUSY}}$.

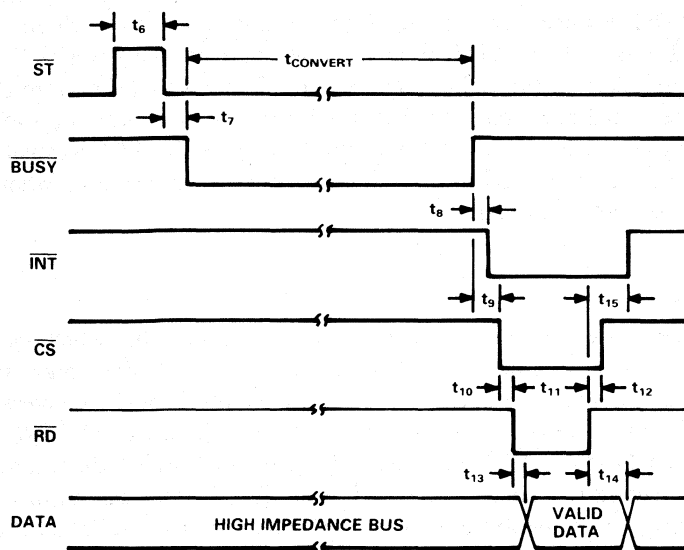


Figure 6. ADC Mode 1 Interface Timing

6.4 Mode 1 Interface.

The timing diagram for the first mode is shown in Figure 6. It can be used in digital signal processing and other applications where precise sampling in time is required. In these applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases the $\overline{ST}$ line is driven by a timer or some precise clock source.

The falling edge of the $\overline{ST}$ pulse starts conversion and drives the AD7569 track-and-hold amplifier into its hold mode. $\overline{BUSY}$ stays low for the duration of conversion and returns high at the end of conversion and the track-and-hold amplifier reverts to its tracking mode on this rising edge of $\overline{BUSY}$. The $\overline{INT}$ line can be used to interrupt the microprocessor. A READ to the AD7569 address accesses the data and the $\overline{INT}$ line is reset on the rising edge of $\overline{CS}$ and $\overline{RD}$. Alternatively the $\overline{INT}$ can be used to trigger a pulse which drives the $\overline{CS}$ and $\overline{RD}$ and places the data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. The $\overline{ST}$ input should not be high when $\overline{RD}$ is brought low otherwise the part will not operate correctly in this mode.

It is important, especially in systems where the conversion start ($\overline{ST}$ pulse) is asynchronous to the microprocessor, that a READ does not occur during a conversion. Trying to read data from the device during a conversion can cause errors to the conversion in progress. Also, pulsing the $\overline{ST}$ line a second time before conversion end should be avoided since it too can cause errors in the conversion result. In applications where precise sampling is not critical the $\overline{ST}$ pulse can be generated from a microprocessor $\overline{WR}$ or $\overline{RD}$ line gated with a decoded address (different to AD7569 $\overline{CS}$ address).

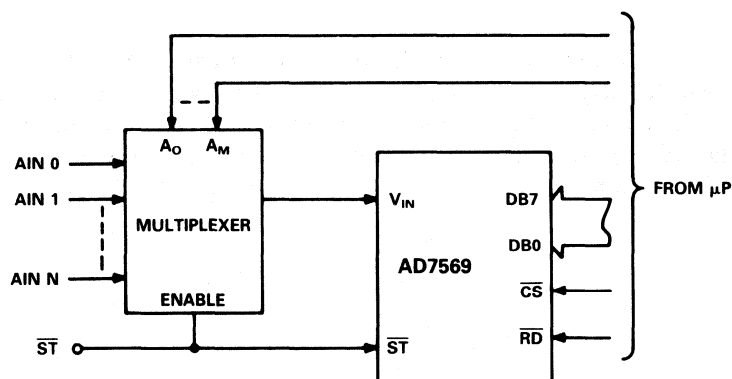


Figure 7. Multichannel Inputs

This interface mode is also useful in applications where a number of input channels are required to be converted by the ADC. Figure 7 shows the circuit configuration for such an application. The signal which drives the $\overline{ST}$ input of the AD7569 is also used to drive the ENABLE input of the multiplexer. The multiplexer is enabled on the rising edge of the $\overline{ST}$ pulse while the input signal is held on the falling edge. Therefore, the signal must have settled to within 8 bits over the duration of the $\overline{ST}$ pulse. The settling time, including t_{ON} (ENABLE) of the multiplexer plus the T/H acquisition time (typically 200 ns), thus determines the width of the $\overline{ST}$ pulse. This is suited to applications where a number of input channels need to be successively sampled or scanned.

6.5 Mode 2 Interface.

The second interface mode is intended for use with microprocessors which can be forced into a WAIT state for at least 2 μ s. The $\overline{ST}$ line of the AD7569 must be hard-wired high to achieve this mode. The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7569 address, bringing $\overline{CS}$ and $\overline{RD}$ low. $\overline{BUSY}$ and $\overline{RD}$ low. $\overline{BUSY}$ subsequently goes low (forcing the microprocessor READY or WAIT input low), placing the microprocessor into a WAIT state. The input signal is held on the falling edge of $\overline{RD}$ (assuming $\overline{CS}$ is already low or is co-incident with $\overline{RD}$). When the conversion is complete ($\overline{BUSY}$ goes high), the processor completes the memory READ and acquires the newly converted data. While conversion is in progress, the ADC places old data (from the previous conversion) on the data bus. The timing diagram for this interface is shown in Figure 8.

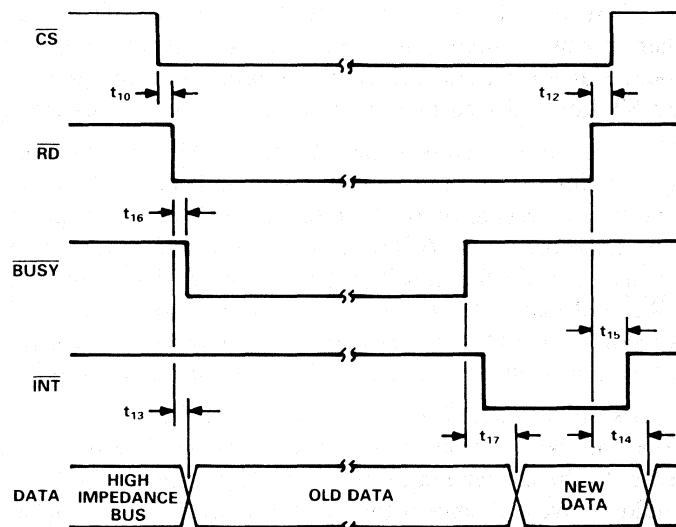


Figure 8. ADC Mode 2 Interface Timing

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion. The fast conversion time of the ADC ensures that for many microprocessors, the processor is not placed in a WAIT state for an excessive amount of time.

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS successive approximation 12-bit analog-to-digital converter with an on chip buried Zener reference and converting in 5 or 12 μ s.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification are as follows:

Device	Part Number
-1	AD7572S(X)05/883B and AD7572S(X)12/883B
-2	AD7572T(X)05/883B and AD7572T(X)12/883B
-3	AD7572U(X)05/883B and AD7572U(X)12/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to DGND	 -0.3 V, +7 V
V_{SS} to DGND	 +0.3 V, -17 V
AGND to DGND	 -0.3 V, $V_{DD} + 0.3$ V
AIN to AGND	 -15 V, +15 V
Digital Input Voltage to DGND	 -0.3 V, $V_{DD} + 0.3$ V
Digital Output Voltage to DGND	 -0.3 V, $V_{DD} + 0.3$ V
Power Dissipation (to $+75^\circ\text{C}$)	 1000 mW
Derates above $+75^\circ\text{C}$	 10 mW/ $^\circ\text{C}$
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$
Storage Temperature	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	 $+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-24 and E-28A

AD7572 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2, 3	12				Minimum Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	-1, 2	1	1	1			±LSB max
		-3	3/4	1	3/4	1/2		
Differential Nonlinearity	DNL	-1, 2, 3	1	1	1			±LSB max
Offset Error	OE	-1	6	4	6			±LSB max
		-2	5	4	5	3		
		-3	4	4	4			
Full-Scale Error ²	FSE	-1		15				±LSB max
		-2, 3		15		10		
Full-Scale Temp Co ³	FSTC	-1	45		45			±ppm/°C max
		-2, 3	25		25			
Analog Input Current		-1, 2, 3	3.5	3.5	3.5			mA max
V _{REF} Output	V _{REF}	-1, 2, 3		-5.25			±1%	V max
V _{REF} Temp Co	REFTC	-1	40		40			±ppm/°C max
		-2, 3	20		20			
Output Current Sink Capability		-1, 2, 3	550	550	550		External Load Should Not Change During Conversion	μA max
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input High Voltage	V _{IM}	-1, 2, 3	2.4	2.4	2.4			V min
Input Capacitance	C _{IN}	-1, 2, 3	10					pF max
Input Current 1	I _{IN1}	-1, 2, 3	10	10	10		$\overline{CS}$, $\overline{RD}$, HBEN	±μA max
Input Current 2	I _{IN2}	-1, 2, 3	20	20	20		CLKIN	±μA max
Digital Output Low Voltage	V _{OL}	-1, 2, 3	0.4	0.4	0.4		I _{SINK} = 1.6 mA	V max
Digital Output High Voltage	V _{OH}	-1, 2, 3	4.0	4.0	4.0		I _{SOURCE} = 200 μA	V min
Floating State Leakage Current	I _{OUT}	-1, 2, 3	10	10	10			±μA max
Floating State Output Capacitance	C _{OUT}	-1, 2, 3	15					pF max
Supply Current from V _{DD}	I _{DD}	-1, 2, 3	7	7	7			mA max
Supply Current from V _{SS}	I _{SS}	-1, 2, 3	-12	-12	-12			mA max
Conversion Time ⁴ Synchronous Clock	t _{CONV}	-1, 2, 3	5	5	5		f _{CLK} = 2.5 MHz	μs max
			12.5	12.5	12.5	12.5	f _{CLK} = 1 MHz	
Conversion Time ⁴ Asynchronous Clock	t _{CONV}	-1, 2, 3	4.8	4.8	4.8		f _{CLK} = 2.5 MHz	μs min
			5.2	5.2	5.2			μs max
Conversion Time ⁴ Asynchronous Clock	t _{CONV}	-1, 2, 3	12	12	12		f _{CLK} = 1 MHz	μs min
			13	13	13			μs max

NOTES

¹V_{DD} = +5 V ± 5%, V_{SS} = -15 V ± 5%.

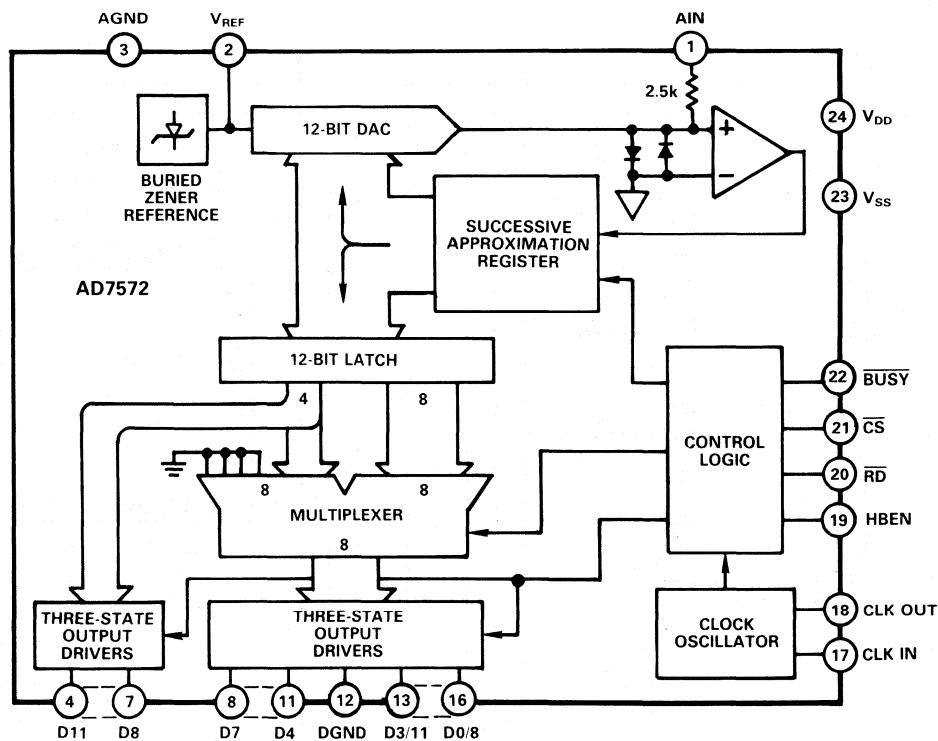
²Includes Internal V_{REF} Error.

³Includes Internal V_{REF} Drift.

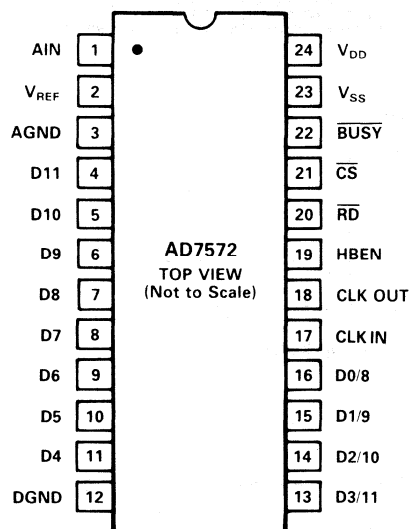
⁴Order either AD7572YX05/883B or AD7572YX12/883B.

Table 1.

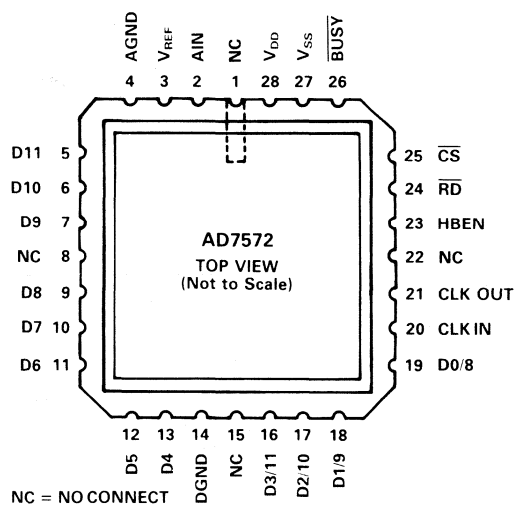
3.2.1 Functional Block Diagram and Terminal Assignments.



**Q Package
(DIP)**



**E Package
(LCC)**



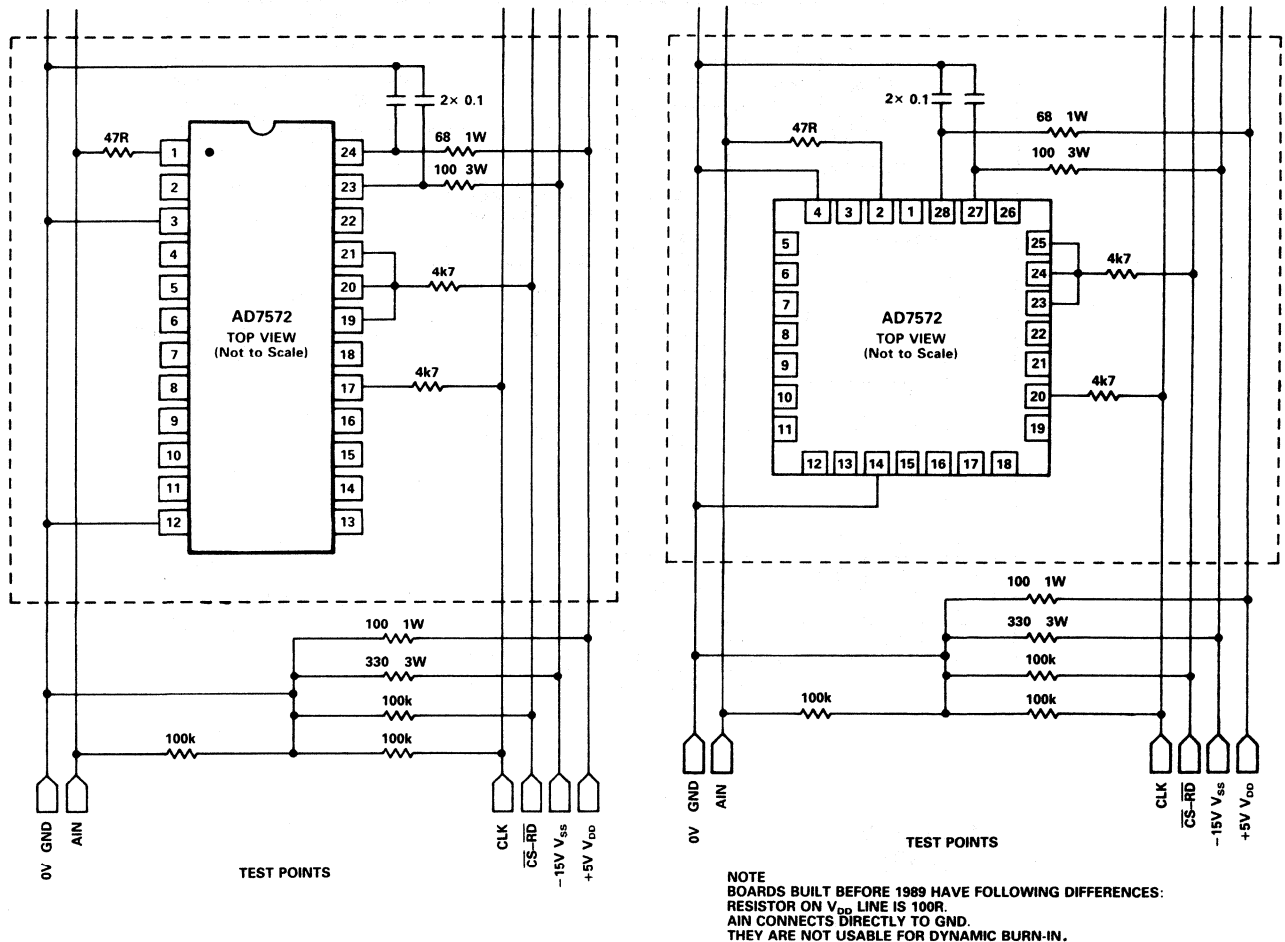
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by Technology Group (81).

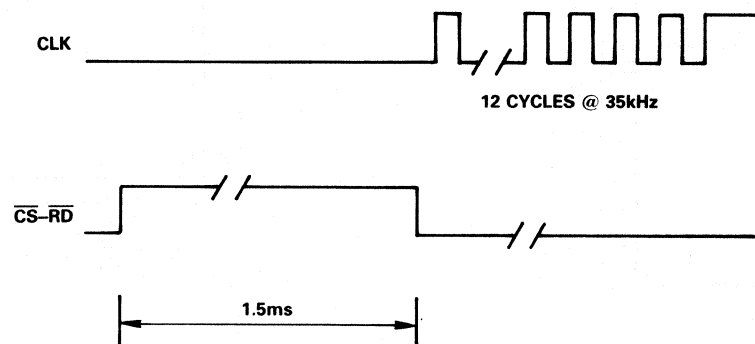
AD7572

4.2.1 Life Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7572 Edge Connections



Static Burn-in Initialization

AD7572 TIMING¹

Test	Symbol	Device	Design Limit T _{min} to T _{max}	Units
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time	t_1	-1, 2, 3	0	ns min
$\overline{\text{RD}}$ to BUSY Propagation Delay	t_2	-1, 2, 3	270	ns max
Data Access Time after $\overline{\text{RD}}$, $C_L = 20$ pF	t_3^2	-1, 2, 3	120	ns max
Data Access Time after $\overline{\text{RD}}$, $C_L = 100$ pF			170	ns max
$\overline{\text{RD}}$ Pulse Width	t_4	-1, 2, 3	t_3	ns min
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	t_5	-1, 2, 3	0	ns min
Data Setup Time after BUSY	t_6^2	-1, 2, 3	100	ns max
Bus Relinquish Time	t_7^3	-1, 2, 3	20	ns min
			90	ns max
HBEN to $\overline{\text{RD}}$ Setup Time	t_8	-1, 2, 3	0	ns min
HBEN to $\overline{\text{RD}}$ Hold Time	t_9	-1, 2, 3	0	ns min
Delay Between Successive Read Operations	t_{10}	-1, 2, 3	200	ns min

NOTES

¹All input control signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

² t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

³ t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

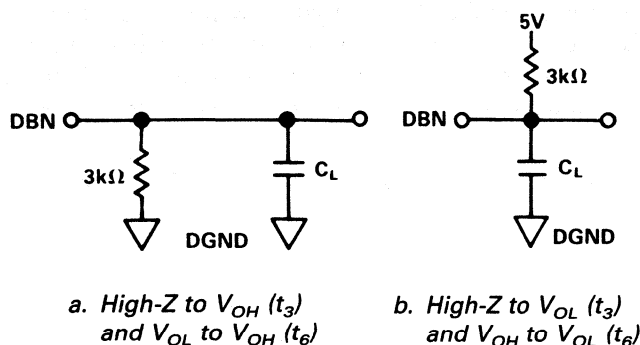


Figure 1. Load Circuits for Access Time

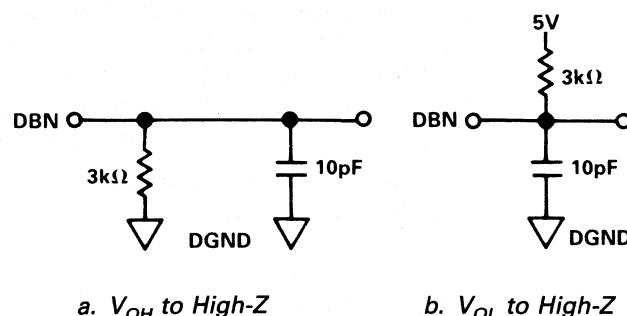


Figure 2. Load Circuits for Output Float Delay

6.0 Converter Details.

Conversion start is controlled by the $\overline{\text{CS}}$, $\overline{\text{RD}}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit voltage mode DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 3, the AIN input connects to the comparator input via 2.5 kΩ. The DAC which has a similar 2.5 kΩ output impedance connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 80 ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 80 ns after a CLK IN edge until conversion is finished. At the end of conversion, the DAC output current balances the AIN input current. The SAR contents (12-bit data word) which represent the AIN input signal is loaded into a 12-bit latch.

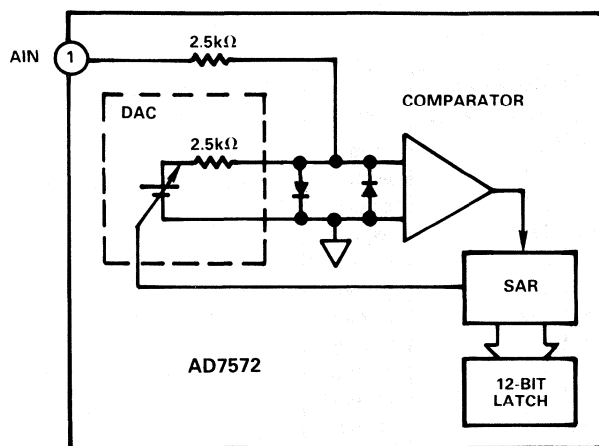


Figure 3. AD7572 AIN Input

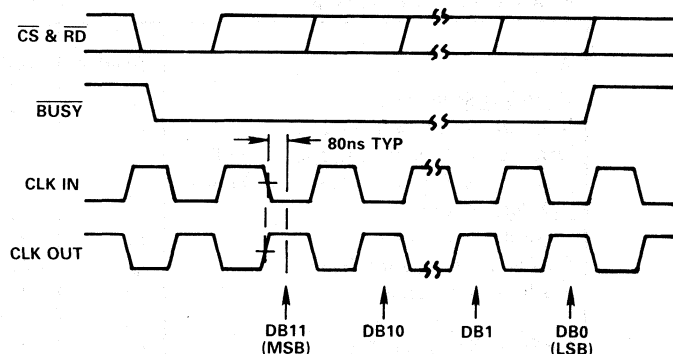


Figure 4. Operating Waveforms Using an External Clock Source for CLK IN

6.1 Driving the Analog Input.

During conversion, the AIN input current is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 2.5 MHz when CLK IN = 2.5 MHz). The analog input voltage must remain fixed during this period and as a result must be driven from an op amp or sample hold with a low output impedance. The output impedance of an op amp is equal to the open loop output impedance divided by the loop gain at the frequency of interest.

Suitable devices capable of driving the AD7572 AIN input are the AD OP-27 and AD711 op amps or the AD585 sample hold.

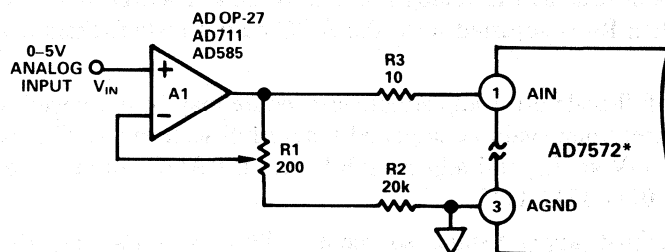
6.2 Control Inputs Synchronization.

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach ensures a fixed 5 μ s conversion time for the AD7572XX 05 and 12.5 μ s for the AD7572XX12: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT.

6.3 Unipolar Offset and Full-Scale Error Adjustment.

In applications where absolute accuracy is important, then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 5 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving AIN (i.e., A1 in Figure 5.). For zero offset error apply 0.61 mV (i.e., 1/2 LSB) at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817 V (i.e., FS $-3/2$ LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.



* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 5. Unipolar 0 to +5 V Operation with Gain Error Adjust

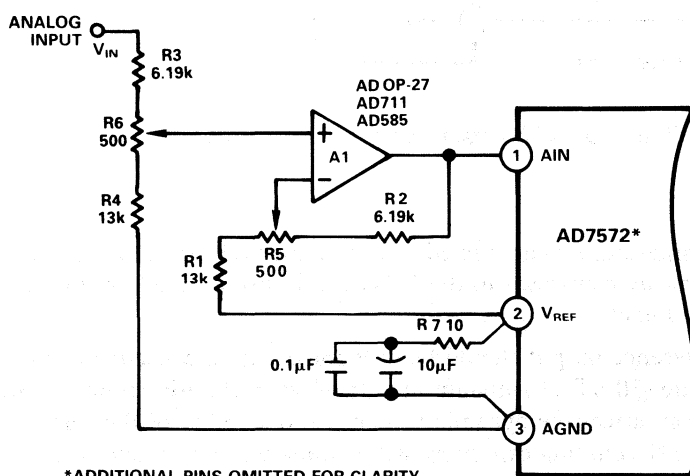
6.4 Bipolar Operation.

Figures 6 and 7 show how bipolar operation can be achieved with the AD7572. Both circuits use an op amp to offset the analog signal (V_{IN}) by 2.5 V. Alternatively, the op amp (A1) can be replaced by a sample hold as shown in Figure 24. The op amp transfer functions are given below:

Figure 10: $A_{IN} = (V_{IN} + 2.5)$ volts

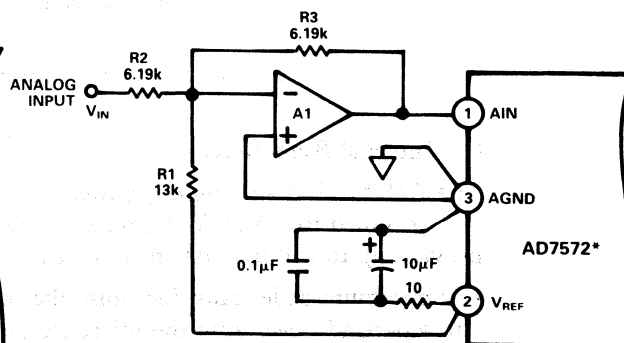
Figure 12: $A_{IN} = (-V_{IN} + 2.5)$ volts

Both circuits have an analog input range of ± 2.5 V and an LSB size of 1.22 mV. The output codes are offset binary for Figure 6 and complimentary offset binary for Figure 7.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 6. AD7572 Bipolar Operation – Output Code is Offset Binary



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 7. AD7572 Bipolar Operation – Output Code is Complimentary Offset Binary

Signal ranges other than ± 2.5 V are easily accommodated using different values of R3 and R4 for Figure 6, and a different R2 value for Figure 7. These resistors should be chosen such that the voltage range at AIN covers the full dynamic range (i.e., 0 V to 5 V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

In measurement applications where absolute accuracy is required, offset and full-scale error can be adjusted to zero as in Figure 8.

6.5 Bipolar Offset and Full-Scale Error Adjustment.

The bipolar circuit of Figure 6 can be adjusted for offset and full-scale errors, by including two potentiometers R5 and R6, as shown in Figure 8. Offset must be adjusted before full-scale error. This is achieved by applying an analog input of 0.61 mV (1/2 LSB) at V_{IN} and adjusting R5 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

AD7572

For full-scale error adjustment, the analog input must be at 2.49817 volts (i.e., $FS/2 - 3/2$ LSBs or last transition point). Then R6 is adjusted until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

A similar offset and full-scale error adjustment procedure may be employed for Figure 7 by making R1 and R2 variable. Offset must again be adjusted before full scale error. This is achieved by applying an analog input of 0.61 mV at V_{IN} and adjusting R1 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

For full-scale error adjust, apply a signal source of 2.49817 V at V_{IN} and adjust R2 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

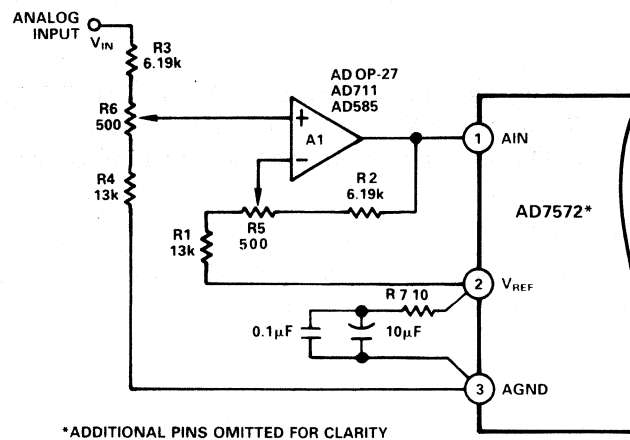


Figure 8. AD7572 Bipolar Operation with Offset and Gain Error Adjust

6.6 Internal Reference.

The AD7572 has an on-chip, buffered, temperature-compensated, buried Zener reference, which is factory trimmed to $-5.25 \text{ V} \pm 1\%$. It is internally connected to the DAC and is also available at Pin 2 to provide up to 550 μA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10 μF of tantalum in parallel with 100 nF ceramic). However, large values of decoupling capacitor can affect the dynamic response and stability of the reference amplifier. A 10 Ω resistor in series with the decoupling capacitors will eliminate this problem without adversely affecting the filtering effect of the capacitors. A simplified schematic of the reference with its recommended decoupling components is shown in Figure 9.

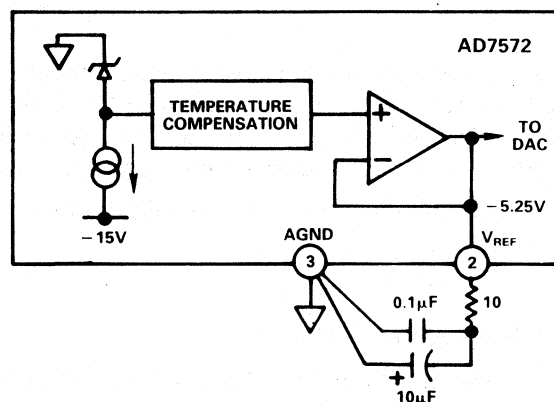


Figure 9. AD7572 Internal -5.25 V Reference

1.1 Scope.

This specification covers the detail requirements for an 8-bit microprocessor compatible monolithic CMOS analog-to-digital converter which uses the successive-approximations technique to provide a conversion time of 15μs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7574S(X)/883B
-2	AD7574T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-18	18-Pin Side-Brazed Ceramic
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V _{DD} to AGND	0V, +7V
V _{DD} to DGND	0V, +7V
Clock Input Voltage (Pin AGND) to DGND	-0.3V, V _{DD}
Digital Input Voltage (Pin 15-16) to DGND	-0.3V, +15V
Digital Output Voltage (Pin 6-14) to DGND	-0.3V to V _{DD}
Clock Input Voltage (Pin 17) to DGND	-0.3V to V _{DD}
V _{REF} (Pin 1)	±20V
V _{BOFS} (Pin 3)	±20V
V _{AIN} (Pin 4)	±20V
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for D-18, Q-18 and E-20A
 θ_{JA} = 120°C/W for D-18, Q-18 and E-20A

AD7574 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	8					Bits
Relative Accuracy	RA	– 1	3/4	3/4	3/4		Measured Using External Clock Frequency of 500kHz	± LSB max
		– 2	1/2	3/4	1/2	1/2		
Differential Nonlinearity	DNL	– 1	7/8	7/8	7/8		Measured Using External Clock Frequency of 500kHz	± LSB max
		– 2	3/4	7/8	3/4	3/4		
Gain Error	AE	– 1	6.5	5	6.5		Gain Error is Measured After Calibrating Out Offset Error.	± LSB max
		– 2	4.5	5	4.5	3		
Offset Error	V_{OS}	– 1	80	60	80			± mV max
		– 2	50	60	50	30		
Resistance Mismatch between BOFS (Pin 3) and A_{IN} (Pin 4)	RM	– 1, 2	1.5	1.5	1.5			± % max
Input Resistance @ V_{REF} (Pin 2) @ BOFS (Pin 3) @ A_{IN} (Pin 4)	R_{IN}	– 1, 2	5	5	5			k Ω min
			15	15	15			k Ω max
		– 1, 2	10	10	10			k Ω min
			30	30	30			k Ω max
		– 1, 2	10	10	10			k Ω min
			30	30	30			k Ω max
Digital Input High Level	V_{IH}	– 1, 2	3.0	3.0	3.0		$\overline{RD}$ (Pin 15), $\overline{CS}$ (Pin 16)	V min
Digital Input Low Level	V_{IL}	– 1, 2	0.8	0.8	0.8			V max
Digital Input Current	I_{IN}	– 1, 2	10	1	10		$V_{IN} = 0V$ or V_{DD}	± μA max
Digital Input Capacitance	C_{IN}	– 1, 2	5					pF max
Clock Input High Level	V_{IH}	– 1, 2	3.0	3.0	3.0			V min
Clock Input Low Level	V_{IL}	– 1, 2	0.4	0.4	0.4			V max
Clock Input High Current	I_{IH}	– 1, 2	2	2	2			± mA max
Clock Input Low Current	I_{IL}	– 1, 2	10	1	10			± μA max
Digital Output High Level	V_{OH}	– 1, 2	4	4	4		$I_{SOURCE} = 40\mu A$	V min
Digital Output Low Level	V_{OL}	– 1, 2	0.8	0.4	0.8		$I_{SINK} = 1.6mA$	V max
Floating State Leakage Current (DB7–DB0)	I_{LKG}	– 1, 2	10	1	10		$V_{OUT} = 0V$ or V_{DD}	± μA max
Floating State Output Capacitance (DB7–DB0)	C_{OUT}	– 1, 2	7					pF max
Supply Current from V_{DD}	I_{DD}	– 1, 2	5	5	5		$A_{IN} = 0V$, $\overline{BUSY}$ and $\overline{RD}$ High	mA max
$\overline{CS}$ Pulse Width	t_{CS}	– 1, 2	150					ns min
$\overline{RD}$ to $\overline{CS}$ Setup Time	$t_{W_{SCS}}$	– 1, 2	0					ns min
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	t_{CBPD}	– 1, 2	180				$\overline{BUSY}$ Load = 20pF	ns max
			200				$\overline{BUSY}$ Load = 100pF	ns max
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}	– 1, 2	0					ns min
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}	– 1, 2	0					ns min
Data Valid Access Time	t_{RAD}	– 1, 2	400				DB0–DB7 Load = 100pF	ns max
Data Valid Hold Time	t_{RHD}	– 1, 2	80				Note 2	ns min
			180				Note 2	ns max
		– 1, 2	80				Note 3	ns min
			180				Note 3	ns max

Table 1. (Continued on next page)

REV. B

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHS}	- 1, 2	500					ns max
Reset Time Requirement	t_{RESET}	- 1, 2	3.0					μs min
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_{WBPD}	- 1, 2	2.0				$\overline{BUSY}$ Load = 20pF	μs max
Conversion Time	$t_{CONVERT}$	- 1, 2	15				With External Clock of 500kHz	μs max

NOTES

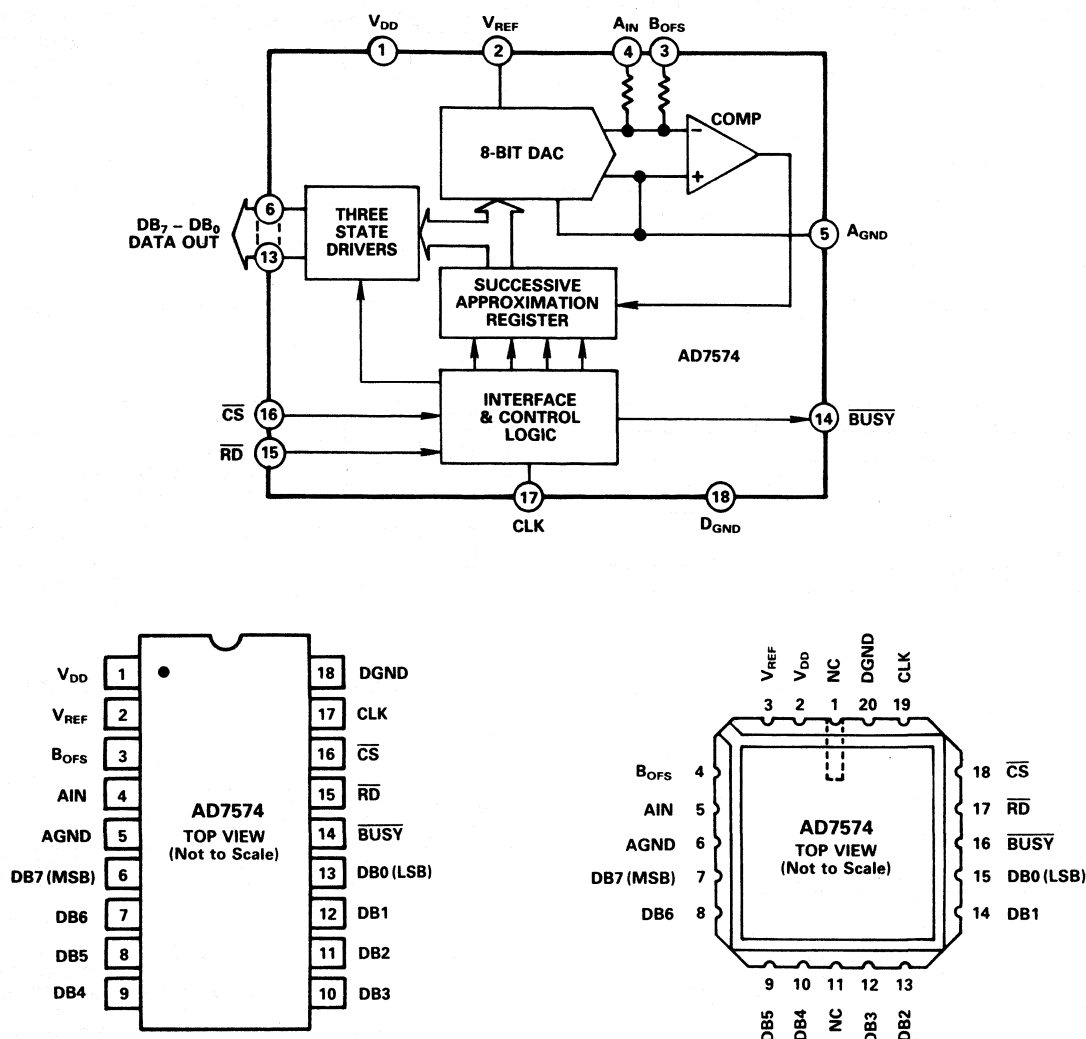
¹ $V_{DD} = +5V$; $V_{REF} = -10V$, Unipolar Configuration, $R_{CLK} = 180$, $C_{CLK} = 100pF$ unless otherwise stated.

²Static RAM interface mode.

³ROM interface mode.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

AD7574

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

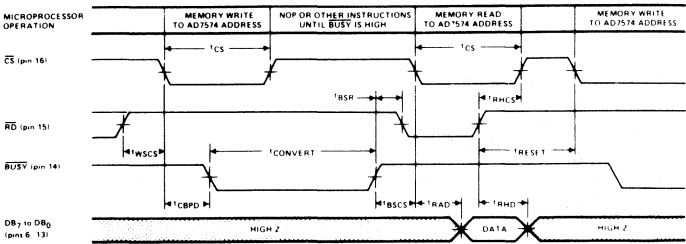
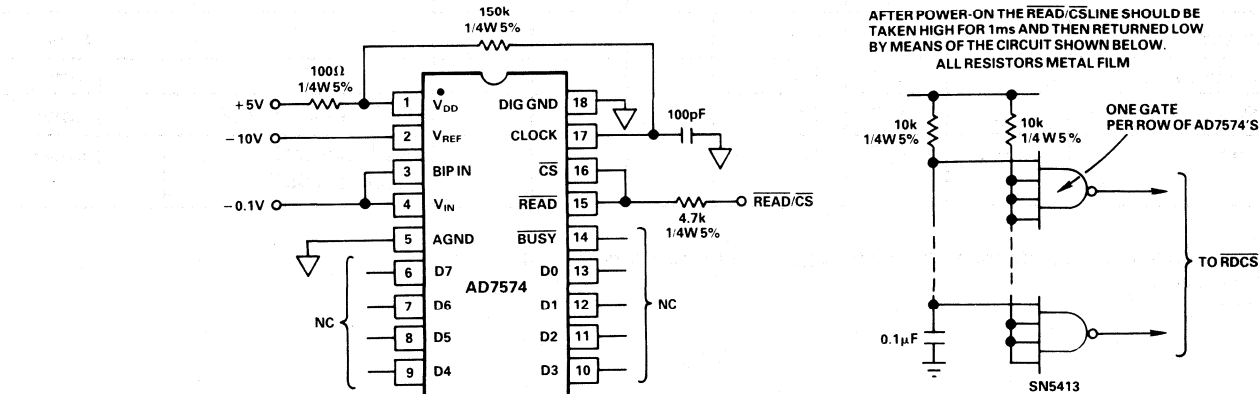


Figure 1. Static RAM Mode Timing Diagram

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
CS	RD	BUSY	DB ₇ -DB ₀	
L	H	H	HIGH Z	WRITE CYCLE (START CONVERT) READ CYCLE (DATA READ) RESET CONVERTER
L	L	H	HIGH Z → DATA	
L	L	H	DATA → HIGH Z	
H	X ¹	X	HIGH Z	NOT SELECTED NO EFFECT CONVERTER BUSY NO EFFECT CONVERTER BUSY NOT ALLOWED, CAUSES INCORRECT CONVERSION
L	H	L	HIGH Z	
L	L	L	HIGH Z	
L	L	L	HIGH Z	

NOTE
¹If RD goes LOW to HIGH when CS is LOW, the ADC is internally reset, RD has no effect while CS is HIGH.

Table II. Truth Table, Static RAM Mode

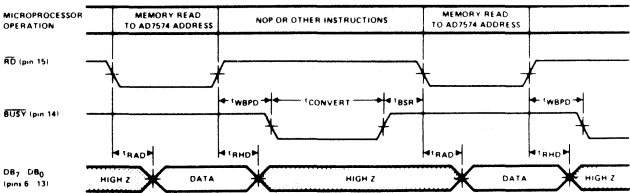


Figure 2. ROM Mode Timing Diagram (CS Held LOW)

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
CS	RD	BUSY	DB ₇ -DB ₀	
L	H	H	HIGH Z → DATA	DATA READ RESET AND START NEW CONVERSION
L	L	H	DATA → HIGH Z	
L	L	L	HIGH Z	NO EFFECT, CONVERTER BUSY NOT ALLOWED, CAUSES INCORRECT CONVERSION
L	L	L	HIGH Z	

Table III. Truth Table, ROM Mode

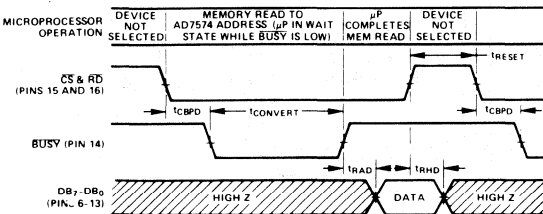


Figure 3. Slow Memory Mode Timing Diagram (CS and RD Tied Together)

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
CS & RD		BUSY	DB ₇ -DB ₀	
H		H	HIGH Z	NOT SELECTED START CONVERSION CONVERSION IN PROGRESS μP IN WAIT STATE
L		H → L	HIGH Z	
L		L	HIGH Z	
L		┐	HIGH → DATA	CONVERSION COMPLETE, μP READS DATA CONVERTER RESET AND DESELECTED NOT SELECTED
┐		H	DATA → HIGH Z	
H		H	HIGH Z	

Table IV. Truth Table, Slow Memory Mode

1.1 Scope.

This specification covers the detail requirements for an 8-bit microprocessor compatible analog-to-digital converter with a built-in track/hold function. The successive approximation technique is used to achieve a conversion time of 5 μ s, while the on-chip track/hold allows full-scale signals up to 50kHz to be digitized. The AD7575 operates with a single +5V supply, a +1.23V bandgap reference and converts an input signal range of 0 to 2V_{REF}.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number ¹
- 1	AD7575S(X)/883B
- 2	AD7575T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V _{DD} to AGND	- 0.3V, +7V
V _{DD} to DGND	- 0.3V, +7V
AGND to DGND	- 0.3V, V _{DD}
Digital Input Voltage to DGND (Pins 1, 2)	- 0.3V, V _{DD}
Digital Output Voltage to DGND (Pins 4, 6-8, 10-14)	- 0.3V, V _{DD}
CLK Input Voltage (Pin 5) to DGND	- 0.3V, V _{DD}
V _{REF} to AGND	- 0.3V to V _{DD}
AIN to AGND	- 0.3V to V _{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-18 and E-20A
 θ_{JA} = 120°C/W for Q-18 and E-20A

AD7575 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error	TUE	-1	2	2	2			± LSB max
		-2	1	2	1	1		
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2	0.5	1	0.5	0.5		
Full-Scale Error		-1, 2	1	1	1			± LSB max
Offset Error		-1, 2	0.5	0.5	0.5		Measured with respect to an ideal first code transition which occurs at 1/2LSB.	± LSB max
Analog Input Voltage Range	A _{IN}	-1, 2	0 to 2V _{REF}					V
DC Input Impedance	Z _{IN}	-1, 2	10	10	10			MΩ min
Slew Rate Tracking		-1, 2	0.386					V/μs max
Signal Noise Ratio		-1, 2	45				V _{IN} = 2.46V p-p @ 10kHz	dB min
Reference Input Current	I _{REF}	-1, 2	500	500	500			μA max
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8		$\overline{CS}$, $\overline{RD}$, CLK	V max
Digital Input High Voltage	V _{IH}	-1, 2	2.4	2.4	2.4		$\overline{CS}$, $\overline{RD}$, CLK	V min
Digital Input Current	I _{IN}	-1, 2	10	1	10		$\overline{CS}$, $\overline{RD}$, V _{IN} = 0 or V _{DD} ; V _{DD} = 5.2V	± μA max
Digital Input Capacitance	C _{IN}	-1, 2	10				$\overline{CS}$, $\overline{RD}$	pF max
Digital Input Low Current	I _{IL}	-1, 2	800	800	800		CLK; V _{IL} = 0V	μA max
Digital Input High Current	I _{IH}	-1, 2	800	800	800		CLK, V _{IH} = V _{DD}	μA max
Digital Output Low Voltage	V _{OL}	-1, 2	0.4	0.4	0.4		$\overline{BUSY}$, DB0 to DB7 I _{SINK} = 1.6mA; V _{DD} = 4.75V	V max
Digital Output High Voltage	V _{OH}	-1, 2	4.0	4.0	4.0		BUSY, DB0 to DB7 I _{SOURCE} = 40μA; V _{DD} = 4.75V	V min
Floating State Leakage Current	I _{OUT}	-1, 2	10	10	10		DB0 to DB7 V _{OUT} = 0 to V _{DD} ; V _{DD} = 5.2V	± μA max
Floating State Output Capacitance	C _{OUT}	-1, 2	10				DB0 to DB7	pF max
Conversion Time with External Clock	t _{CONV}	-1, 2	5	5	5		f _{CLK} = 4MHz	μs
Conversion Time with External Clock @ +25°C	t _{CONV}	-1, 2	5			5	Recommended Clock Components: R = 100kΩ, C = 100pF	μs min
			15			15		μs max
$\overline{CS}$ to $\overline{RD}$ Setup Time, t ₁	t _{W$\overline{CS}$}	-1, 2	0					ns min
$\overline{RD}$ to BUSY Propagation Delay, t ₂	t _{WBPD}	-1, 2	120					ns max
Data Access Time after $\overline{RD}$, t ₃ ²	t _{DAR}	-1, 2	120					ns max
$\overline{RD}$ Pulse Width, t ₄	t _{RD}	-1, 2	120					ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time, t ₅	t _{RHS}	-1, 2	0					ns min
Data Access Time after $\overline{BUSY}$, t ₆ ²	t _{DAB}	-1, 2	100					ns max
Data Hold Time, t ₇ ³	t _{DH}	-1, 2	10					ns min
			100					ns max
BUSY to $\overline{CS}$ Delay, t ₈	t _{BCD}	-1, 2	0					ns min
Power Supply Current	I _{DD}	-1, 2	7	7	7		V _{DD} = 5.2V	mA max
Power Supply Rejection		-1, 2	0.25	0.25	0.25			± LSB max

NOTES

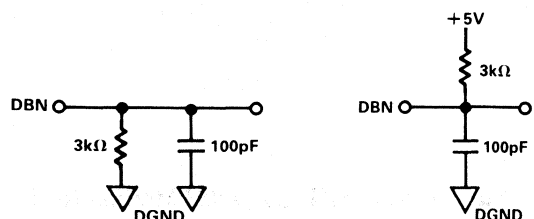
¹V_{DD} = +5V; (unless otherwise stated) V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 4MHz external. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

²t₃ and t₆ are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V to 2.4V.

³t₇ is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

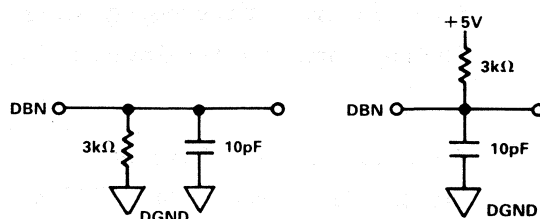
Table 1.

REV. B



a. High-Z to V_{OH}

b. High-Z to V_{OL}



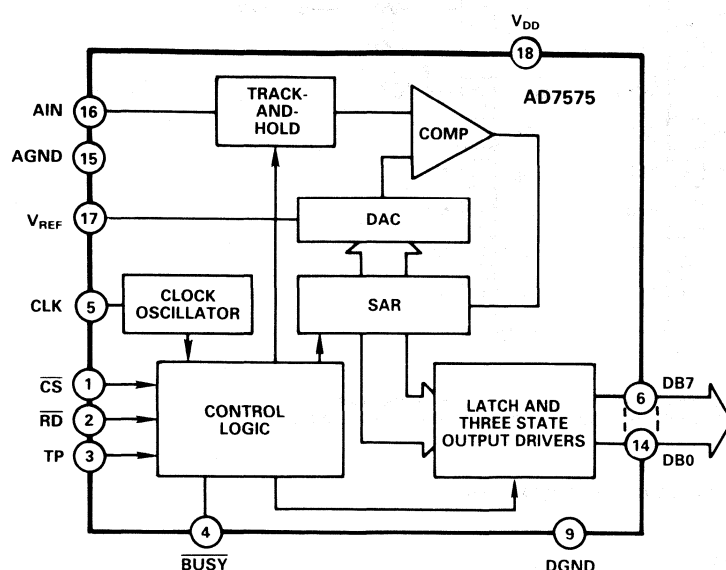
a. V_{OH} to High-Z

b. V_{OL} to High-Z

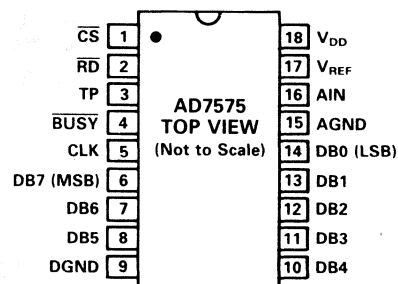
Figure 1. Load Circuits for Data Access Time Test

Figure 2. Load Circuits for Data Hold Time Test

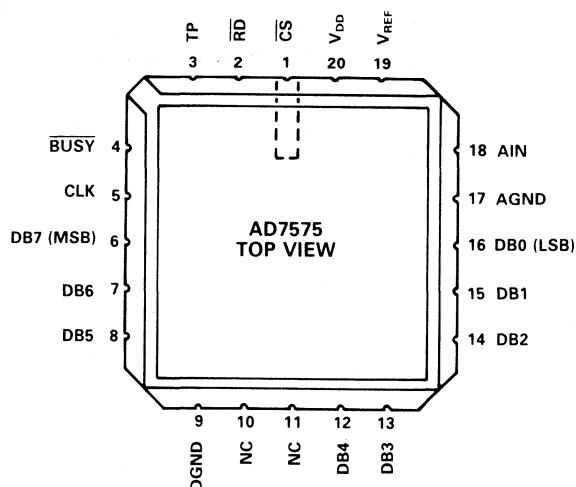
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)



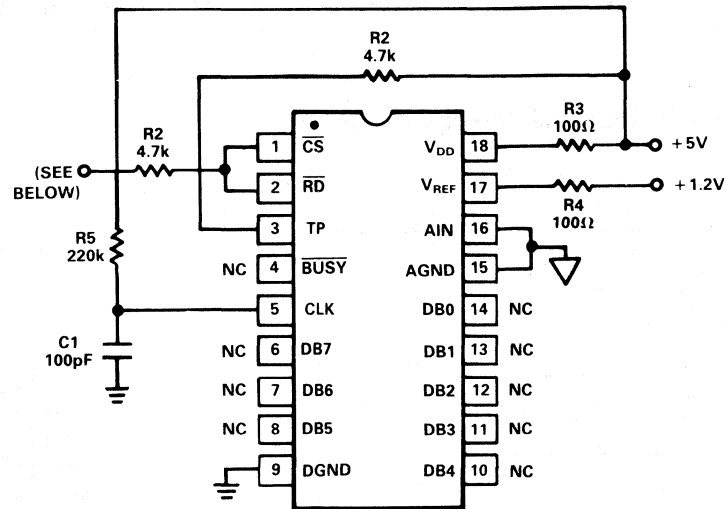
AD7575

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

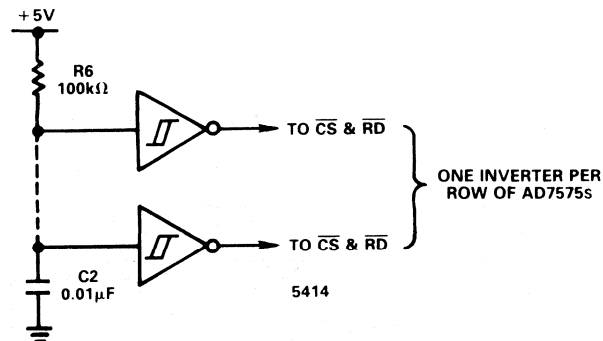


ALL RESISTORS ARE 1/4W.

$\overline{CS}$ AND $\overline{RD}$ ARE TAKEN HIGH FOR 0.6ms - 0.7ms APPROXIMATELY AND ARE THEN BROUGHT LOW. THIS IS ACHIEVED AS FOLLOWS:

NOTE

$\overline{CS}/\overline{RD}$ PULSE MAY BE GENERATED EXTERNALLY.



5.0 Timing and Control of the AD7575.

The two logic inputs on the AD7575, $\overline{CS}$ and $\overline{RD}$, control both the starting of conversion and the reading of data from the part. A conversion is initiated by bringing both these control inputs LOW. Two interface options then exist for reading the output data from the AD7575. These are the Slow Memory Interface and ROM Interface and their operation is outlined below. It should be noted that the TP pin of the AD7575 must be hardwired HIGH to ensure correct operation of the part. This pin is used in testing the device and should not be used as a feedthrough pin in double-sided printed circuit boards.

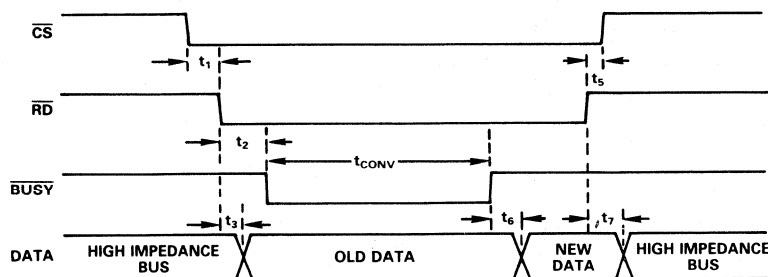


Figure 3. Slow Memory Interface Timing Diagram

5.1 Slow Memory Interface.

The first interface option is intended for use with microprocessors which can be forced into a WAIT STATE for at least $5\mu s$ (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7575 address bringing $\overline{CS}$ and $\overline{RD}$ LOW. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor into a WAIT state. The input signal, which had been tracked by the analog input, is held on the third falling clock edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW. The AD7575 then performs a conversion on this acquired input signal value. When the conversion is complete ($\overline{BUSY}$ goes HIGH), the processor completes the memory READ and acquires the newly-converted data. The timing diagram for this interface is shown in Figure 3.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The fast conversion time of the AD7575 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7575 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is LOW for a READ cycle) provides the READ signal to the AD7575. The connection diagram for the AD7575 to 8085A-2 Slow-Memory interface is shown in Figure 4.

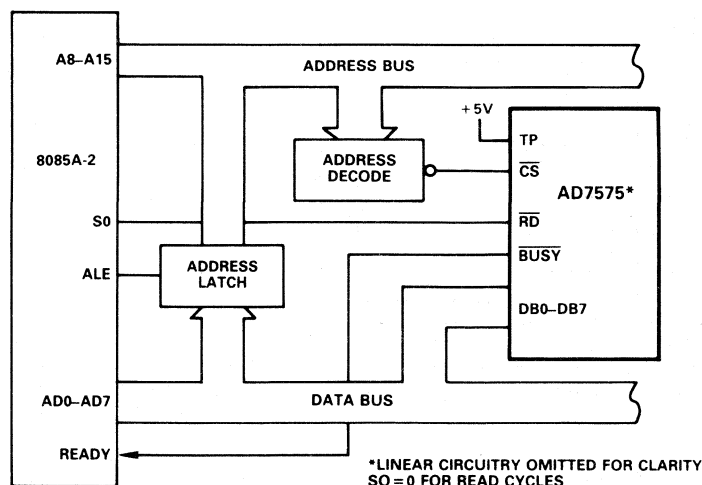


Figure 4. AD7575 to 8085A-2 Slow Memory Interface

5.2 ROM Interface.

The alternative interface option on the AD7575 avoids placing the microprocessor into a WAIT state. In this interface, a conversion is started with the first READ instruction and the second READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5. It is possible to avoid starting another conversion on the second READ (see below).

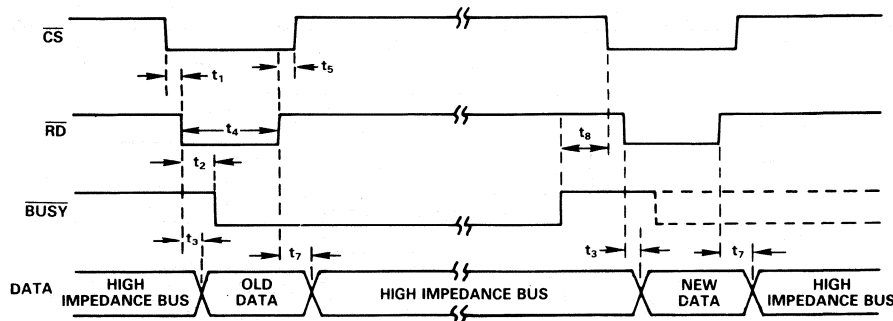


Figure 5. ROM Interface Timing Diagram

Conversion is initiated by executing a memory READ instruction to the AD7575 address causing $\overline{CS}$ and $\overline{RD}$ to go LOW. Data is also obtained from the AD7575 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW indicating that conversion is in progress and returns HIGH when conversion is complete. Once again the input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor or monitored to indicate that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7575 conversion time. For the AD7575 to operate correctly in the ROM interface mode $\overline{CS}$ and $\overline{RD}$ should not go LOW before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

Figures 6 and 7 show connection diagrams for interfacing the AD7575 in the ROM Interface mode.

Figure 6 shows the AD7575 interface to the 6502/6809 microprocessors while the connection diagram for interfacing to the Z-80 is shown in Figure 7.

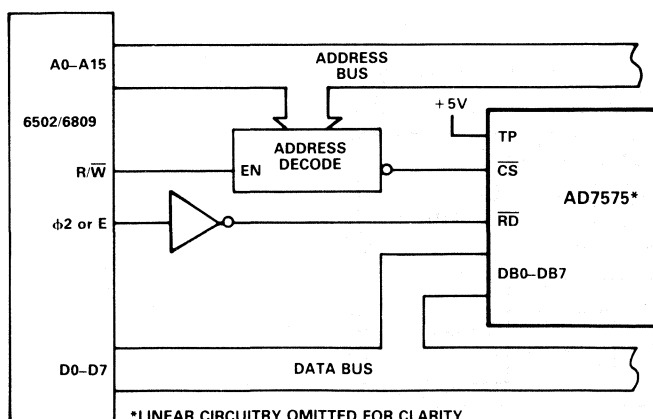


Figure 6. AD7575 to 6502/6809 ROM Interface

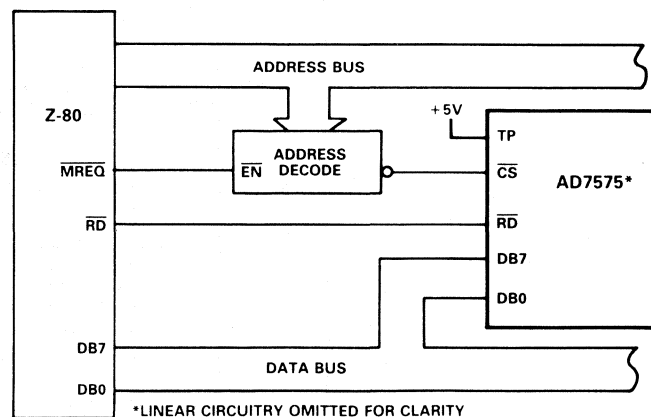


Figure 7. AD7575 to Z-80 ROM Interface

As a result of its very fast interface timing the AD7575 can also be interfaced to the DSP processor, the TMS32010. The AD7575 will interface (within specifications) to the TMS32010 running at up to 18MHz but will typically work over the full clock frequency range of the TMS32010. Figure 8 shows the connection diagram for this interface. The AD7575 is mapped at a port address. Conversion is initiated using an IN A, PA instruction where PA is the decoded port address for the AD7575. The conversion result is obtained from the part using a second IN A, PA instruction and the resultant data is placed in the TMS32010 accumulator.

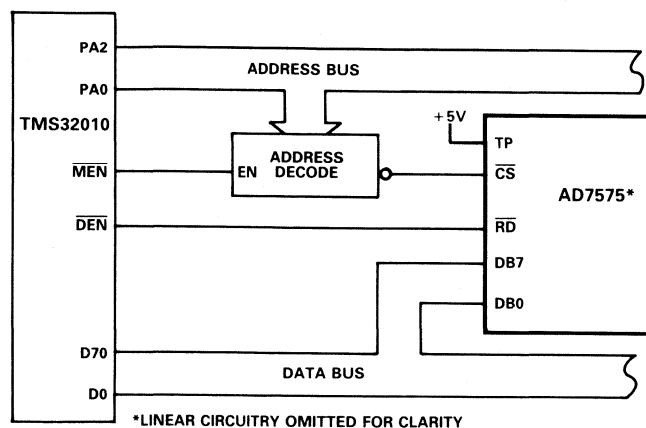


Figure 8. AD7575 to TMS32010 ROM Interface

In many applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. The interfaces outlined previously require that for sampling at equi-distant intervals the user must count clock cycles or match software delays. This is especially difficult in interrupt driven systems where uncertainty in interrupt servicing delays would require that the AD7575 would have to have priority interrupt status and even then redundant software delays may be necessary to equalize loop delays.

This problem can be overcome by using a real time clock to control the starting of conversion. This can be derived from the clock source used to drive the AD7575 CLK pin. Since the sampling instant occurs three clock cycles after $\overline{CS}$ and $\overline{RD}$ go LOW then the input signal sampling intervals are equi-distant. The resultant data is placed in a FIFO latch which can be accessed by the microprocessor at its own rate whenever it requires the data. This ensures that data is not READ from the AD7575 during a conversion. If a data READ is performed during a conversion, valid data from the previous conversion will be accessed but the conversion in progress may be interfered with and an incorrect result is likely.

If $\overline{CS}$ and $\overline{RD}$ go LOW within 20ns of a falling clock edge the AD7575 may or may not see that falling edge as the first of the three falling clock edges to the sampling instant. In this case the sampling instant could vary by one clock period. If it is important to know the exact sampling instant, $\overline{CS}$ and $\overline{RD}$ should not go LOW within 20ns of a falling clock edge.

1.1 Scope.

This specification covers the detail requirements for an 8-bit microprocessor compatible analog-to-digital converter, which uses the successive approximation technique to achieve a conversion time of 10 μ s. The part operates with an external reference of +1.23V and converts input signals from 0V to 2V_{REF}.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number ¹
– 1	AD7576S(X)/883B
– 2	AD7576T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V _{DD} to AGND	– 0.3V, +7V
V _{DD} to DGND	– 0.3V, +7V
AGND to DGND	– 0.3V, V _{DD}
Digital Input Voltage to DGND (Pins 1–3)	– 0.3V, V _{DD}
Digital Output Voltage to DGND (Pins 4, 6–8, 10–14)	– 0.3V, V _{DD}
CLK Input Voltage (Pin 5) to DGND	– 0.3V, V _{DD}
V _{REF} to AGND	– 0.3V to V _{DD}
AIN to AGND	– 0.3V to V _{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	– 55°C to +125°C
Storage Temperature Range	– 65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-18 and E-20A
 θ_{JA} = 120°C/W for Q-18 and E-20A

AD7576 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{\text{man}} - T_{\text{max}}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	– 1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error	TUE	– 1 – 2	2 1	2 2	2 1	1		± LSB max
Relative Accuracy	RA	– 1 – 2	1 0.5	1 1	1 0.5	0.5		± LSB max
Full-Scale Error		– 1, 2	1	1	1			± LSB max
Offset Error		– 1, 2	0.5	0.5	0.5		Measured with respect to an ideal first code transition which occurs at 1/2LSB.	± LSB max
Analog Input Voltage Range	A _{IN}	– 1, 2	0 to 2V _{REF}					V
DC Input Impedance	Z _{IN}	– 1, 2	10	10	10			MΩ min
Reference Input Current	I _{REF}	– 1, 2	500	500	500			μA max
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8		$\overline{\text{CS}}$, $\overline{\text{RD}}$, MODE, CLK	V max
Digital Input High Voltage	V _{IH}	– 1, 2	2.4	2.4	2.4		$\overline{\text{CS}}$, $\overline{\text{RD}}$, MODE, CLK	V min
Digital Input Current	I _{IN}	– 1, 2	10	1	10		$\overline{\text{CS}}$, $\overline{\text{RD}}$, MODE V _{IN} = 0 or V _{DD} , V _{DD} = 5.2V	± μA max
Digital Input Capacitance	C _{IN}	– 1, 2	10				$\overline{\text{CS}}$, $\overline{\text{RD}}$, MODE	pF max
Digital Input Low Current	I _{IL}	– 1, 2	800	800	800		CLK; V _{IL} = 0V	μA max
Digital Input High Current	I _{IH}	– 1, 2	800	800	800		CLK; V _{IH} = V _{DD}	μA max
Digital Output Low Voltage	V _{OL}	– 1, 2	0.4	0.4	0.4		$\overline{\text{BUSY}}$, DB0 to DB7 I _{SINK} = 1.6mA, V _{DD} = 4.75V	V max
Digital Output High Voltage	V _{OH}	– 1, 2	4.0	4.0	4.0		$\overline{\text{BUSY}}$, DB0 to DB7 I _{SOURCE} = 40μA, V _{DD} = 4.75V	V min
Floating State Leakage Current	I _{OUT}	– 1, 2	10	10	10		DB0 to DB7 V _{OUT} = 0 to V _{DD} , V _{DD} = 5.2V	± μA max
Floating State Output Capacitance	C _{OUT}	– 1, 2	10				DB0 to DB7	pF max
Conversion Time with External Clock	t _{CONV}	– 1, 2	10	10	10		f _{CLK} = 2MHz	μs
Conversion Time with External Clock (at + 25°C)	t _{CONV}	– 1, 2	10 30			10 30	Recommended Clock Components: R = 150kΩ, C = 150pF	μs min μs max
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time, t ₁	t _{W_{SCS}}	– 1, 2	0					ns min
$\overline{\text{RD}}$ to $\overline{\text{BUSY}}$ Propagation Delay, t ₂	t _{WBPD}	– 1, 2	120					ns max
Data Access Time after $\overline{\text{RD}}$ ² , t ₃	t _{DAR}	– 1, 2	120					ns max
$\overline{\text{RD}}$ Pulse Width, t ₄	t _{RD}	– 1, 2	120					ns min
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time, t ₅	t _{RHS}	– 1, 2	0					ns min
Data Access Time after $\overline{\text{BUSY}}$, t ₆	t _{DAB}	– 1, 2	100					ns max
Data Hold Time, t ₇ ³	t _{DH}	– 1, 2	10 100					ns min ns max
$\overline{\text{BUSY}}$, to $\overline{\text{CS}}$ Delay, t ₈	t _{BCD}	– 1, 2	0					ns min
Power Supply Current	I _{DD}	– 1, 2	7	7	7		V _{DD} = 5.2V	mA max
Power Supply Rejection		– 1, 2	0.25	0.25	0.25			± LSB max

NOTES

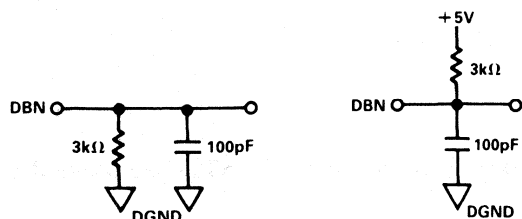
¹V_{DD} = + 5V; (except where otherwise mentioned) V_{REF} = + 1.23V; AGND = DGND = 0V; f_{CLK} = 2MHz external. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of + 5V) and timed from a voltage level of 1.6V.

²t₃ and t₆ are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V to 2.4V.

³t₇ is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

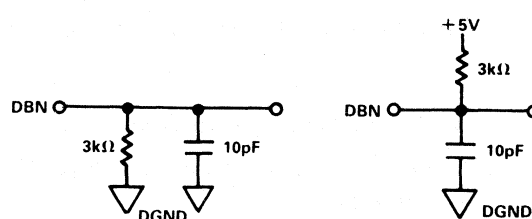
Table 1.

REV. B



a. High-Z to V_{OH}

b. High-Z to V_{OL}



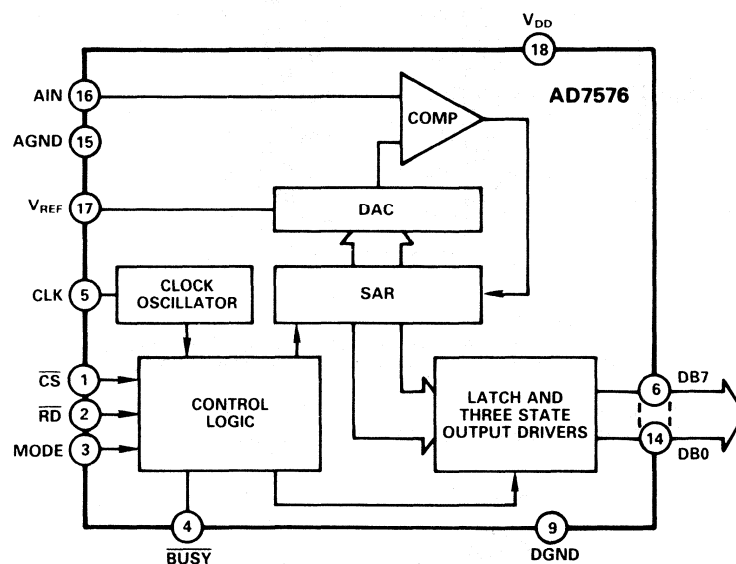
a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 1. Load Circuits for Data Access Time Test

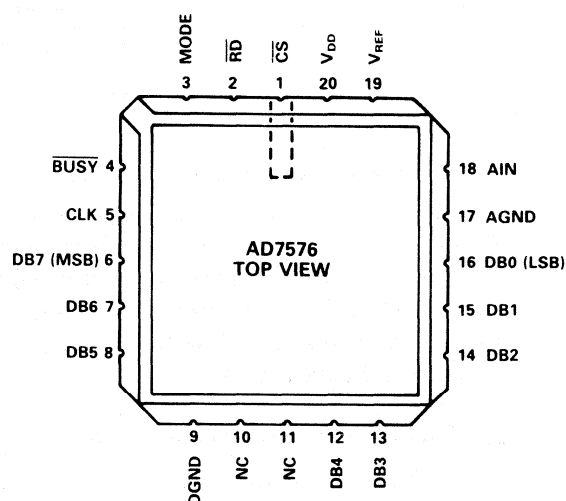
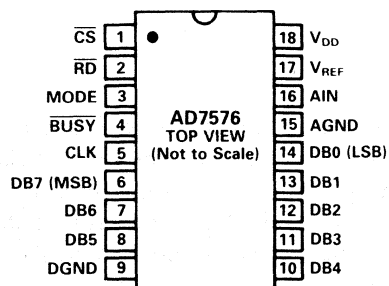
Figure 2. Load Circuits for Data Hold Time Test

3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)

E Package (LCC)



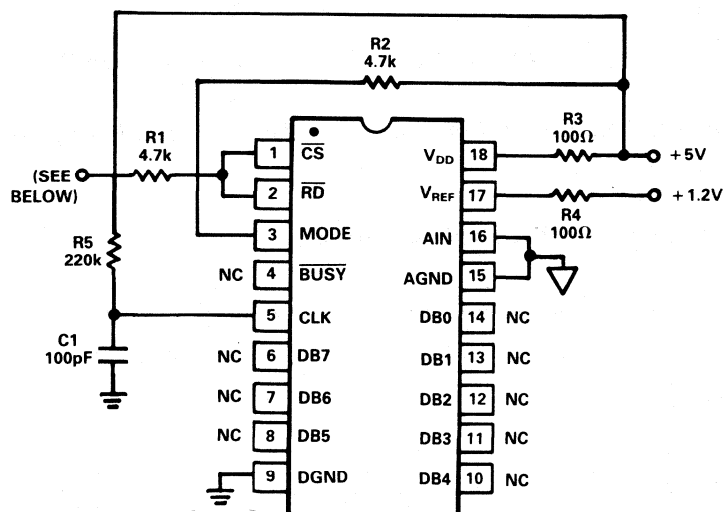
AD7576

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).

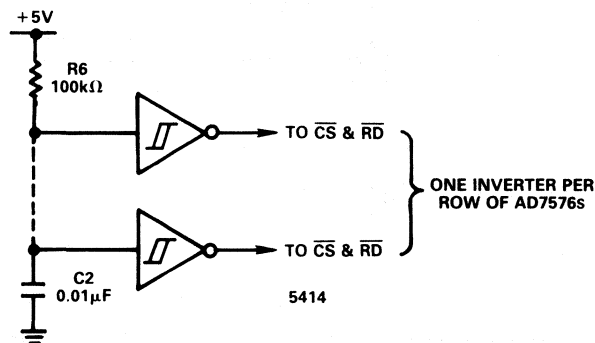


ALL RESISTORS ARE 1/4W.

$\overline{CS}$ AND $\overline{RD}$ ARE TAKEN HIGH FOR 0.6ms – 0.7ms APPROXIMATELY AND ARE THEN BROUGHT LOW. THIS IS ACHIEVED AS FOLLOWS:

NOTE

$\overline{CS}/\overline{RD}$ PULSE MAY BE GENERATED EXTERNALLY.



5.0 Timing and Control of the AD7576.

The AD7576 is capable of two basic operating modes which are outlined in the timing diagrams below. These two operating modes are an Asynchronous Conversion Mode and a Synchronous Conversion Mode. The selection of the required operating mode is determined by the status of the MODE pin. When this pin is HIGH, the device performs conversions only when the required control signals ($\overline{CS}$ and $\overline{RD}$) are applied; with this pin LOW the device performs continuous conversions and $\overline{CS}$ and $\overline{RD}$ are used only to access the output data.

5.1 Synchronous Conversion Mode.

In the Synchronous Conversion mode the AD7576 will perform a conversion when requested to do so by the microprocessor. The MODE pin of the AD7576 is tied HIGH to place the device in Synchronous Conversion operation. Two interface options exist for reading the output data from the AD7576.

REV. B

5.1.1 Slow Memory Interface.

The first of these interface options is intended for use with microprocessors which can be forced into a WAIT STATE for at least 10 μ s (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7576 address. $\overline{\text{BUSY}}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor in a WAIT state. When conversion is complete ($\overline{\text{BUSY}}$ goes HIGH) the processor completes the memory READ.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the AD7576 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time. The timing diagram for this interface is shown in Figure 3.

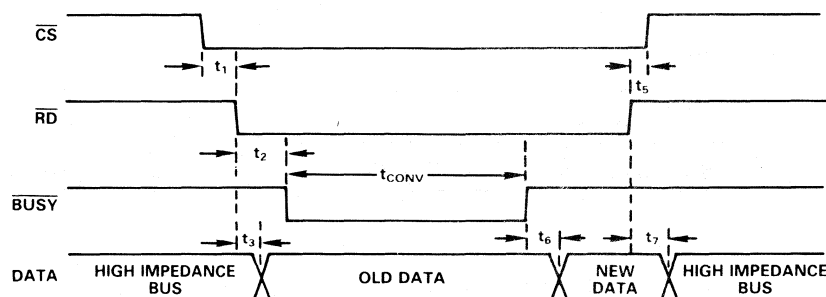


Figure 3. Slow Memory Interface Timing Diagram

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{\text{BUSY}}$ of the AD7576 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is 0 for a READ cycle) provides the READ signal to the AD7576. The AD7576 connection diagram to the 8085A-2 is shown in Figure 4.

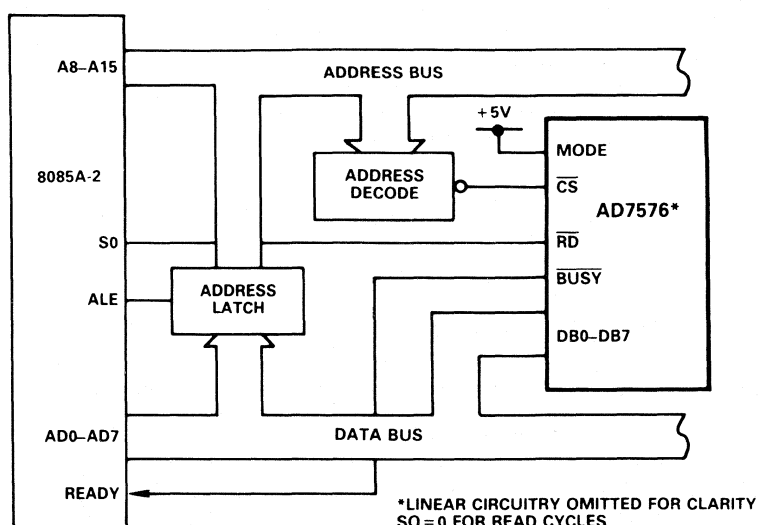


Figure 4. AD7576 to 8085A-2 Slow Memory Interface

5.1.2 ROM Interface.

The alternative interface option in the Synchronous Conversion mode avoids placing the microprocessor into a WAIT state. In this interface, conversion is started with the first read instruction and a second read instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5 while Figure 6 shows the connection diagram for the AD7576 with the 6502/6809 microprocessors.

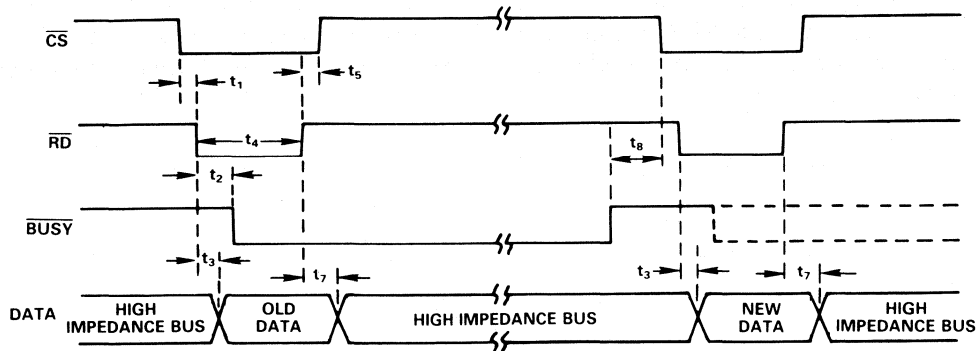


Figure 5. ROM Interface Timing Diagram

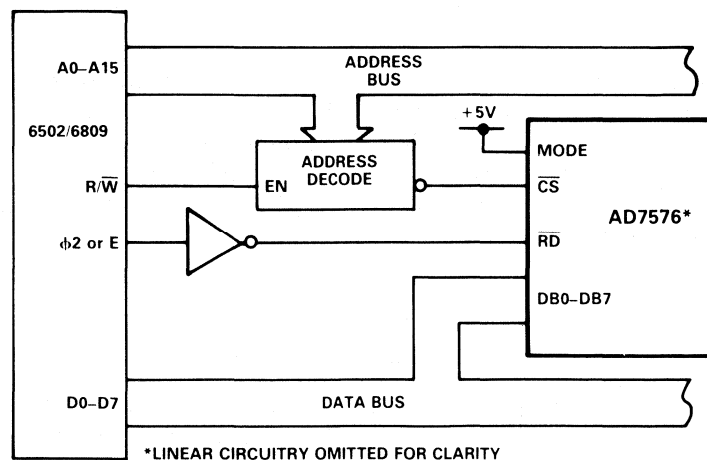


Figure 6. AD7576 to 6502/6809 ROM Interface

Conversion is initiated by executing a memory READ instruction to the AD7576 address. Data is also obtained from the AD7576 during this instruction. This is old data and may be disregarded if not required. **BUSY** goes LOW during conversion and returns HIGH when conversion is complete.

The **BUSY** line may be used to generate an interrupt to the microprocessor indicating that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7576 conversion time. For the AD7576 to operate correctly in the ROM Interface mode **CS** and **RD** should not go low before **BUSY** returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if **CS** and **RD** are brought LOW within one external clock period of **BUSY** going HIGH then a second conversion does not occur.

5.2 Asynchronous Conversion Mode.

When the **MODE** pin of the AD7576 is tied **LOW**, the device performs continuous conversions, and the control lines **CS** and **RD** are used only to read the data from the converter. The timing diagram for this operating mode is outlined in Figure 7, with the connection diagram to the 8085A shown in Figure 8.

Data is obtained from the AD7576 by executing a memory **READ** instruction to its address. The A/D process is completely transparent to the microprocessor and the AD7576 will behave like a ROM. Data may be read at any time completely independent of the clock. This is especially useful in internal clock applications where the user no longer has to worry about synchronizing the clock with the **READ** line of the microprocessor.

The data latches are normally updated by **BUSY** going **HIGH**. However, if **CS** and **RD** are **LOW** when **BUSY** goes **HIGH**, the contents of the data latches are frozen until **CS** or **RD** returns **HIGH**. This ensures that incorrect data cannot be read from the AD7576. The output latches are updated when **CS** or **RD** return **HIGH** and the converter is re-enabled. If **CS** or **RD** do not return **HIGH** the AD7576 will stop performing continuous conversions, and will not start again until either line goes **HIGH**.

The advantage of this mode is its simplicity. The disadvantage of this mode is that the data which is read is not clearly defined in time. However, it will not be older than one conversion period and if this uncertainty is a problem it can be overcome by monitoring the **BUSY** line.

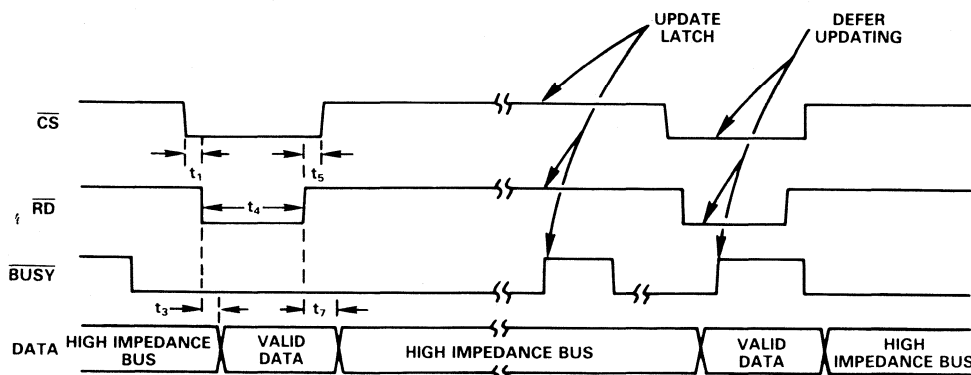


Figure 7. Asynchronous Conversion Mode Timing Diagram

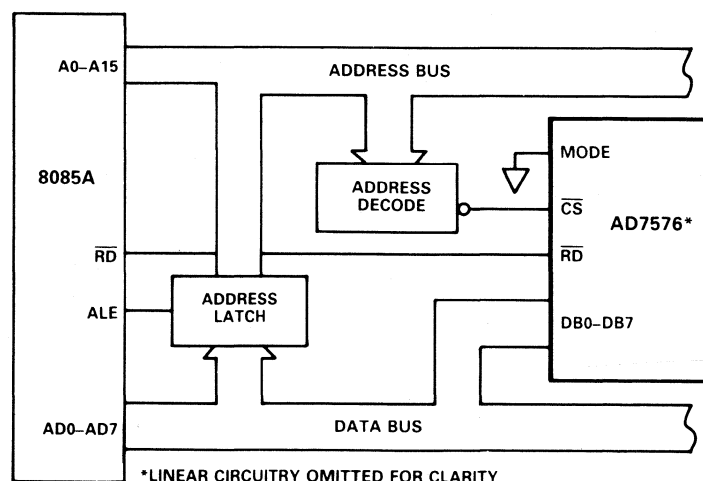


Figure 8. AD7576 to 8085A Asynchronous Conversion Mode Interface

1.1 Scope.

This specification covers the detail requirements of a monolithic 12-bit CMOS analog-to-digital converter which uses the successive approximation technique to provide a conversion time of 100 μ s.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD7578T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-24	24-Pin DIP
Q	Q-24	24-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	– 0.3V, + 17V
V_{SS} to DGND	+ 0.3V, – 7V
AGND to DGND	– 0.3V, $V_{REF} + 0.3V$
V_{CC} to DGND	– 0.3V, $V_{DD} + 0.3V$
V_{REF} to AGND	– 0.3V, $V_{DD} + 0.3V$
AIN to AGND	– 0.3V, $V_{DD} + 0.3V$
Digital Input Voltage to DGND (Pins 16–19, 21)	– 0.3V, $V_{DD} + 0.3V$
Digital Output Voltage to DGND (Pins 8–15, 20)	– 0.3V, $V_{DD} + 0.3V$
Power Dissipation	
Up to $+75^\circ\text{C}$	1000mW
Derates above $+75^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	– 55 $^\circ\text{C}$ to + 125 $^\circ\text{C}$
Storage Temperature Range	– 65 $^\circ\text{C}$ to + 150 $^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

AD7578 – SPECIFICATIONS

Test	Symbol	Device ²	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ^{1,2}	Units
Resolution	RES	– 1	12				Bits
Total Unadjusted Error ³	TUE	– 1	1	1	1		± LSB max
Differential Nonlinearity	DNL	– 1	1	1	1	No Missing Codes Guaranteed	± LSB max
Gain Error	AE	– 1	1/4	1/4	1/4	Gain Error TC is 5ppm/°C typ	± LSB max
Offset Error	V _{OS}	– 1	1/4	1/4	1/4	Offset Error TC is 5ppm/°C typ	± LSB max
Analog Input Range	A _{IN}	– 1	0			V _{REF} = +5V	V min
			5				V max
Input Leakage Current	I _{AIN}	– 1	100	10	100	A _{IN} ; 0 to +5V	nA max
Reference Voltage Range	V _{REF}	– 1	4			Degraded Transfer Accuracy	V min
			6				V max
V _{REF} Input Reference Current	I _{REF}	– 1	1	1	1	V _{REF} = +5V	mA max
Digital Input High Level	V _{IH}	– 1	2.4	2.4	2.4	RD (Pin 16), CS (Pin 17) WR (Pin 18), BYSL (Pin 19)	V min
Digital Input Low Level	V _{IL}	– 1	0.8	0.8	0.8		V max
Digital Input Leakage Current ⁴	I _{IN}	– 1	+10	±1	+10		µA max
Digital Input Capacitance	C _{IN}	– 1	10				pF max
Digital Input High Level	V _{IH}	– 1	3.0	3.0	3.0	CLK (Pin 21)	V min
Digital Input Low Level	V _{IL}	– 1	0.8	0.8	0.8	CLK (Pin 21)	V max
Digital Input Low Current	I _{IL}	– 1	10	10	10	CLK (Pin 21)	± µA max
Digital Input High Current	I _{IH}	– 1	1.5	1.5	1.5	CLK (Pin 21)	+ mA max
Digital Output High Voltage	V _{OH}	– 1	4.0	4.0	4.0	V _{CC} = +4.75V, I _{SOURCE} = 200µA DB0–DB7 (Pins 8–15), BUSY (Pin 20) (See Note 5)	V min
Digital Output Low Voltage	V _{OL}	– 1	0.4	0.4	0.4	V _{CC} = +5.25V, I _{SINK} = 1.6mA DB0–DB7 (Pins 8–15), BUSY (Pin 20) (See Note 5)	V max
Floating State Leakage Current (Pins 8–15)		– 1	1	1	1	V _{OUT} = 0V and V _{CC}	± µA max
Floating State Output Capacitance	C _{OUT}	– 1	15	15	15		pF max
Conversion Time with External Clock ⁶		– 1	100	100	100	f _{CLK} = 140kHz	µs min
Conversion Time with Internal Clock at +25°C		– 1	100	100		Using Recommended Clock Circuit Shown in Figure 5.	µs min
			150	150			µs max
Supply Current from V _{DD} ⁷	I _{DD}	– 1	7.5	7.5	7.5		mA max
Supply Current from V _{SS} ⁷	I _{SS}	– 1	7.5	7.5	7.5		mA max
Supply Current from V _{CC} ⁷	I _{CC}	– 1	1.0	1.0	1.0	V _{IN} = V _{IL} or V _{IH}	mA max
CS to WR Setup Time	t ₁	– 1	0				ns min
WR Pulse Width (Internal Clock Operation) ⁸	t ₂ (INT)	– 1	280			(200ns min at +25°C)	ns min
WR Pulse Width (External Clock Operation) ⁸	t ₂ (EXT)	– 1	10				ns min
CS to WR Hold Time	t ₃	– 1	0				ns min
WR to BUSY Propagation Delay	t ₄	– 1	300			(200ns max at +25°C)	ns max
BUSY to CS Setup Time	t ₅	– 1	0				ns min
CS to RD Setup Time	t ₆	– 1	0				ns min
RD Pulse Width	t ₇	– 1	280			(200ns min at +25°C)	ns min
CS to RD Hold Time	t ₈	– 1	0				ns min

Table 1. (Continued on next page)

Test	Symbol	Device ²	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Test Condition ^{1,2}	Units
BYSL to $\overline{RD}$ Setup Time	t_9	-1	50				ns min
BYSL to $\overline{RD}$ Hold Time	t_{10}	-1	0				ns min
$\overline{RD}$ to Valid Data (Bus Access Time) ⁹	t_{11}	-1	280			(200ns max at +25°C)	ns max
$\overline{RD}$ to Three-State Output (Bus Relinquish Time) ¹⁰	t_{12}	-1	20			(130ns max at +25°C)	ns min
			180				ns max

NOTES

¹ $V_{DD} = +15V$; $V_{CC} = +5V$; $V_{SS} = -5V$; $V_{REF} = +5V$; $f_{CLK} = 140kHz$ external.

²All input control signals are specified with $t_r = t_f = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{OH} , V_{OL} .

³Includes full-scale error, offset error and relative accuracy.

⁴ $V_{IN} = 0$ to V_{CC} .

⁵ I_{SINK} for Busy (Pin 20) is 1.0mA.

⁶Conversion time includes auto-zero cycle time.

⁷Power supply current is measured when the AD7578 is inactive i.e., $\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY} = \text{LOGIC HIGH}$.

⁸When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10 μs (see External Clock Operation).

⁹ t_{11} is defined as the time required for an output to cross 0.8V or 2.4V and is measured with the load circuits of Figure 3.

¹⁰ t_{12} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.

Table 1.

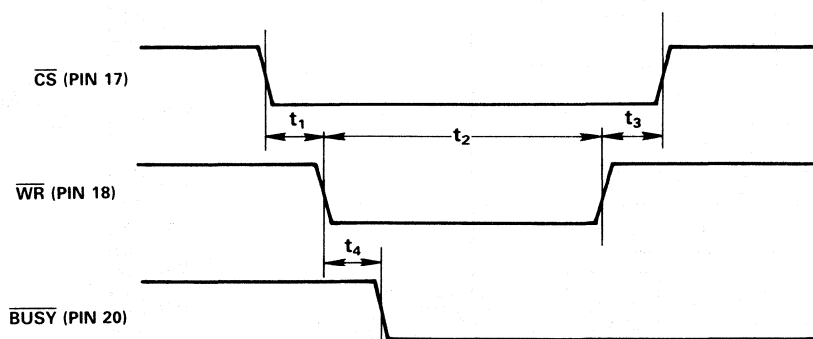
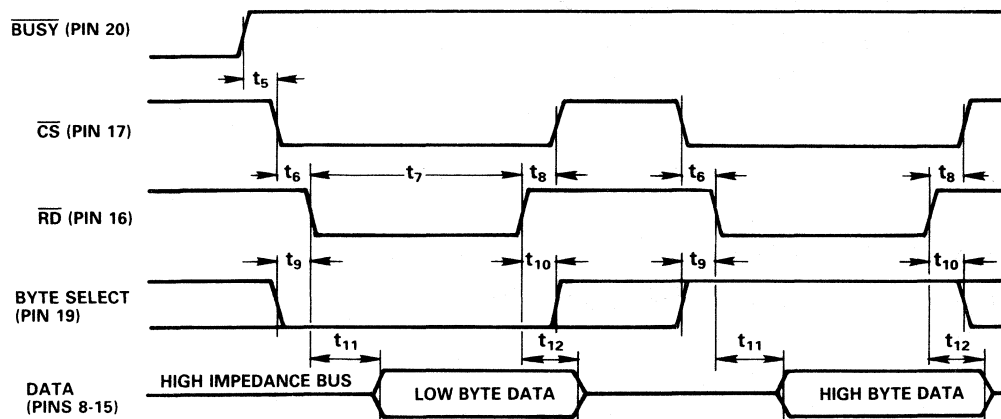
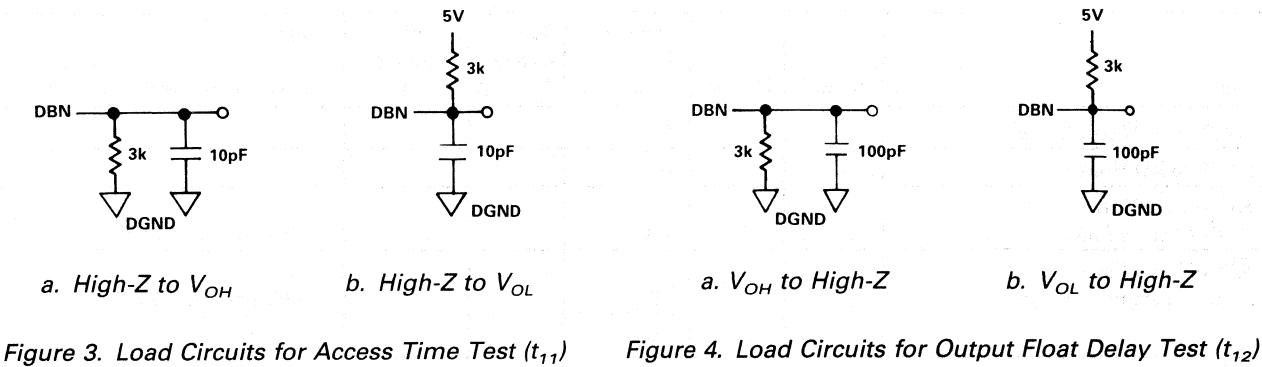


Figure 1. Start Cycle Timing

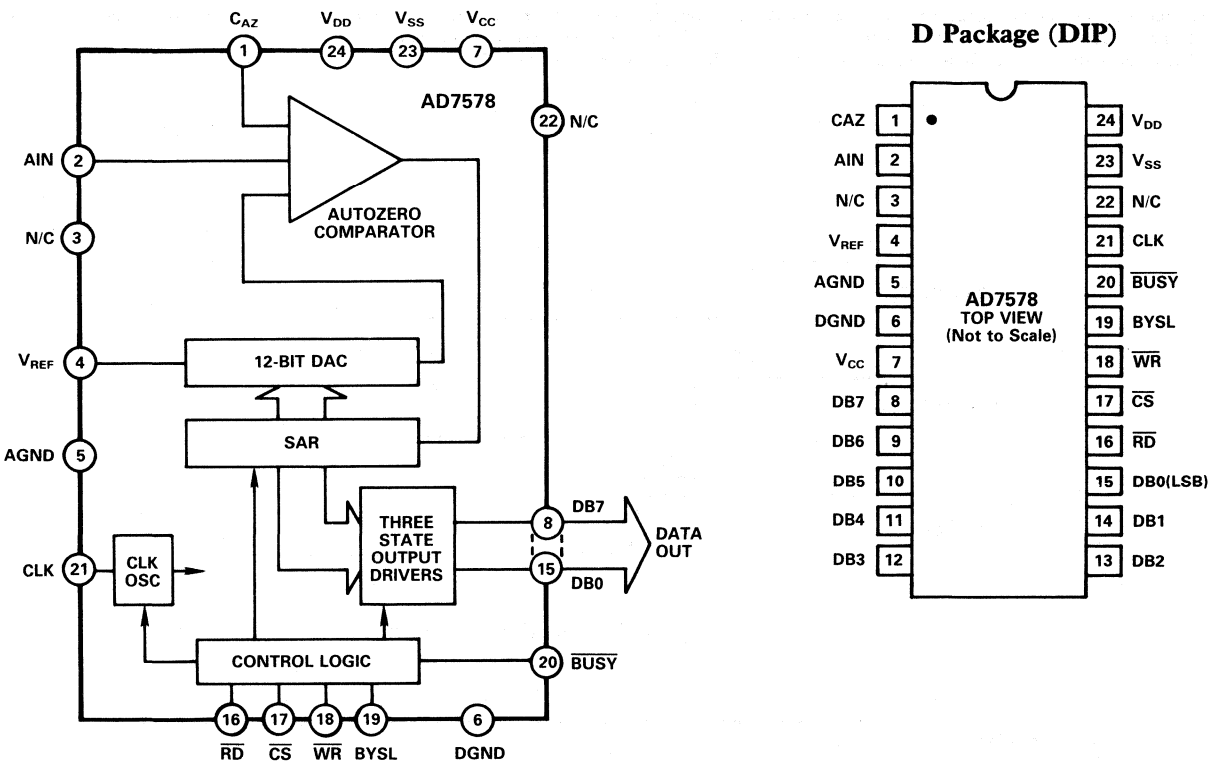


NOTES
THE TWO-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. FIGURE IS FOR LOW BYTE, HIGH BYTE ORDER.
IF BYSL CHANGES WHILE CS & RD ARE LOW THE DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

Figure 2. Read Cycle Timing



3.2.1 Functional Block Diagram and Terminal Assignments.

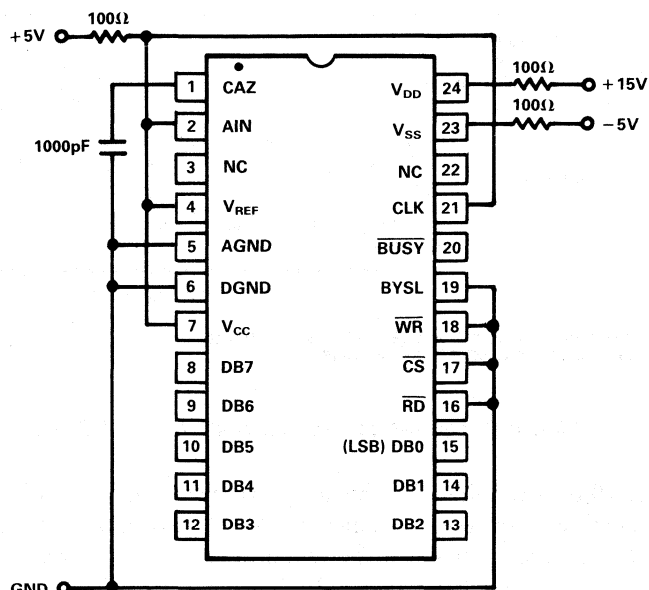


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



24-PIN - 0.3" PACKAGE
ALL RESISTORS FOR PROTECTION ONLY
POWER-UP SEQUENCE -
+15, +5, -5
IN THAT ORDER OR SIMULTANEOUSLY

5.0 Internal Clock Operation.

The clock circuitry for internal clock operation is shown in Figure 5 and the AD7578 operating waveforms are shown in Figure 6.

Between conversions ($\overline{\text{BUSY}} = \text{HIGH}$) the AD7578 is in the autozero cycle. When $\overline{\text{WR}}$ goes LOW (with $\overline{\text{CS}}$ LOW) to start a new conversion, the autozero capacitor C_{AZ} charges to $\text{AIN} - V_{\text{OS}}$ where V_{OS} is the input offset voltage of the autozero comparator.

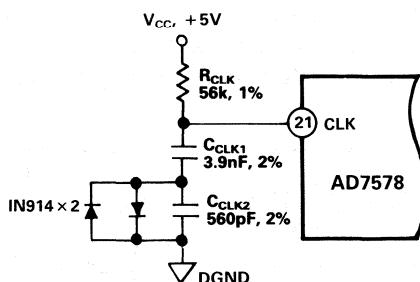


Figure 5. Circuitry Required for Internal Clock Operation

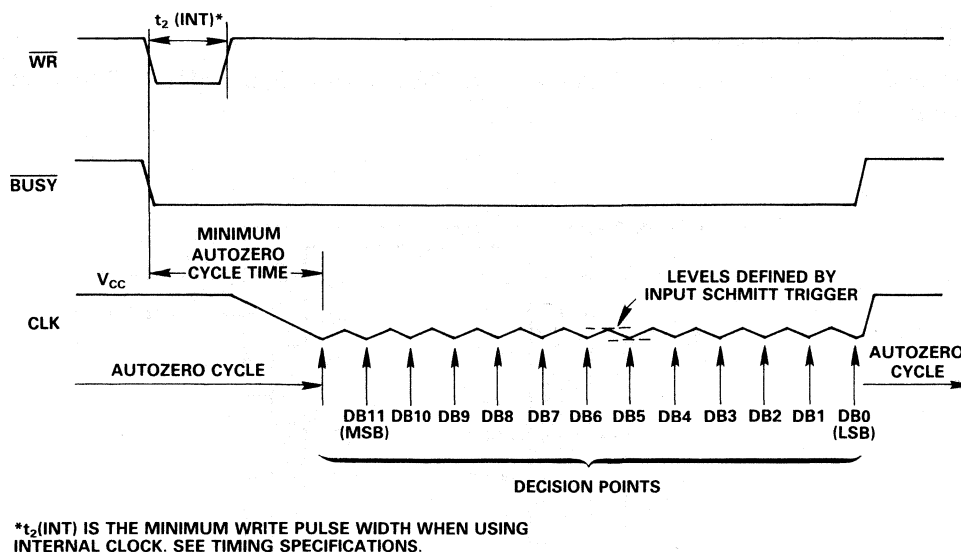


Figure 6. Operating Waveforms – Internal Clock

A minimum time of $10\mu\text{s}$ is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{\text{WR}}$ to remain LOW for this period of time since it is automatically provided by the AD7578. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2} , causing the voltage at the CLK input pin to slowly decay from V_{CC} . This occurs after $\overline{\text{WR}}$ returns HIGH. The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK} . When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2} . The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 5 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

5.1 External Clock Operation.

For external clock operation R_{CLK} , C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The AD7578 $\overline{\text{WR}}$ pulse width must now be extended to provide the minimum autozero cycle time of $10\mu\text{s}$ since this is no longer provided automatically by the AD7578. Referring to the operating waveforms of Figure 8, the minimum $\overline{\text{WR}}$ pulse width when using an external clock source is $t_2(\text{EXT})$. The $\overline{\text{CS}}$ input must now remain valid for the extended $\overline{\text{WR}}$ pulse width. One approach to stretching the available μP signals is shown in the general 8-bit μP interface circuit of Figure 9. It is not necessary to synchronize the external clock source with the extended $\overline{\text{WR}}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{\text{WR}}$ input returns HIGH.

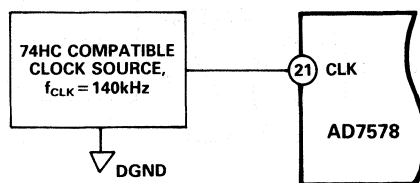


Figure 7. External Clock Operation

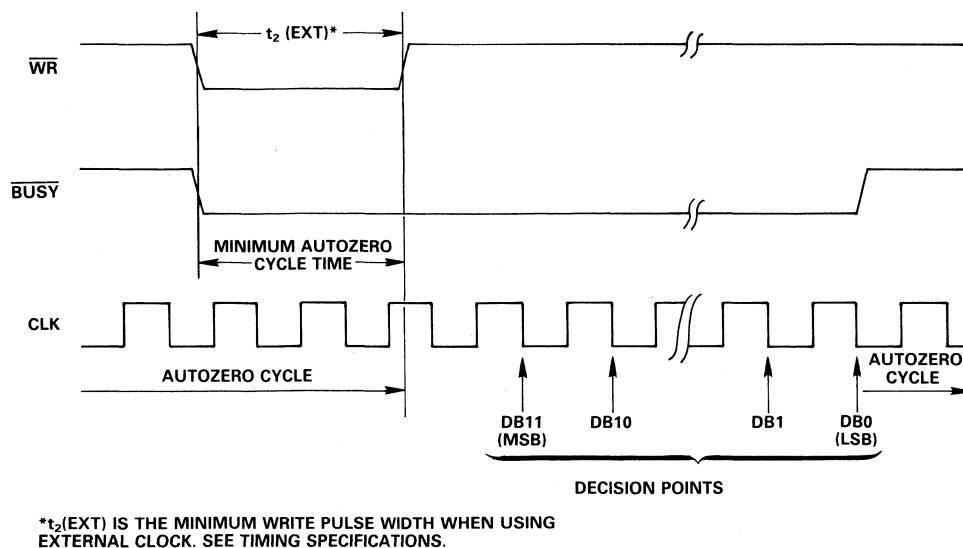


Figure 8. Operating Waveforms – External Clock

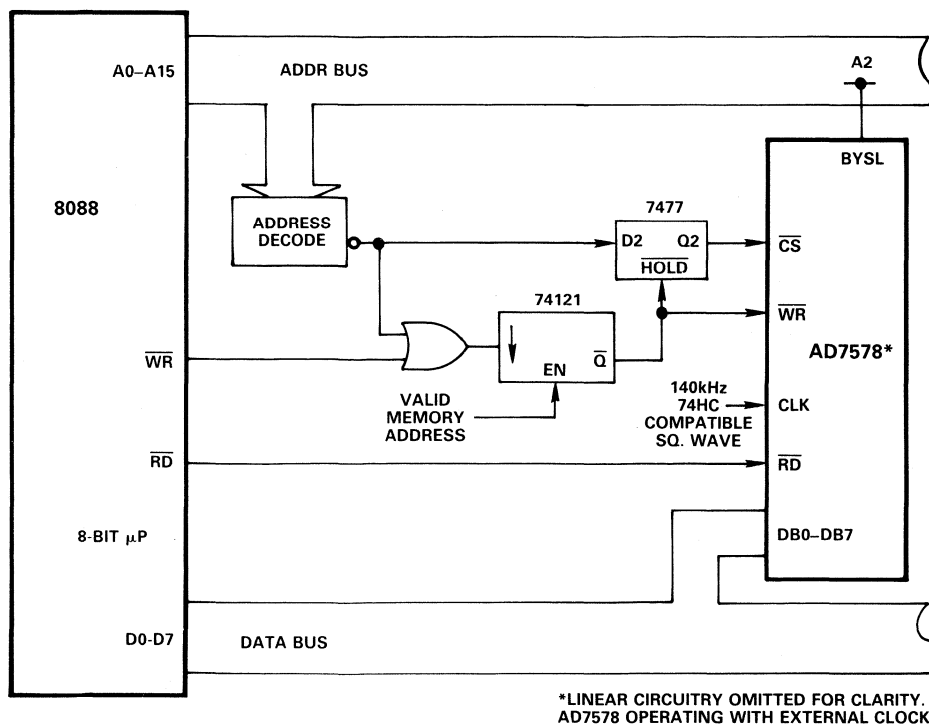


Figure 9. Interface to AD7578 Using External Clock

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 10-bit sampling analog-to-digital converter with parallel (AD7580) and byte (AD7579) output formats.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7579S(X)/883B
-2	AD7580S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to AGND	-0.3 V to +7 V
V_{DD} to DGND	-0.3 V to +7 V
AGND to DGND	-0.3 V, $V_{DD} + 0.3$ V
$V_{IN}(+)A$, $V_{IN}(+)B$ to AGND (Figure 6)	-0.3 V, $V_{DD} + 0.3$ V
$V_{IN}(-)A$, $V_{IN}(-)B$ to AGND (Figure 6)	-0.3 V, $V_{DD} + 0.3$ V
$V_{IN}(+)A$, to AGND (Figure 7)	-0.6 V, $2 V_{DD} + 0.6$ V
$V_{IN}(-)A$, AGND (Figure 7)	-0.6 V, $2 V_{DD} + 0.6$ V
$V_{IN}(+)A$, to AGND (Figure 8)	$-V_{REF} - 0.6$ V, $2 V_{DD} - V_{REF} + 0.6$ V
$V_{IN}(-)A$, AGND (Figure 8)	$-V_{REF} - 0.6$ V, $2 V_{DD} - V_{REF} + 0.6$ V
Digital Input Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
Digital Output Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
CLK Input Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
V_{REF} to AGND	-0.3 V, V_{DD}
Power Dissipation (to $+75^\circ\text{C}$)	450 mW
Derates above $+75^\circ\text{C}$	6 mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-24 and E-28A

AD7579/AD7580 – SPECIFICATIONS

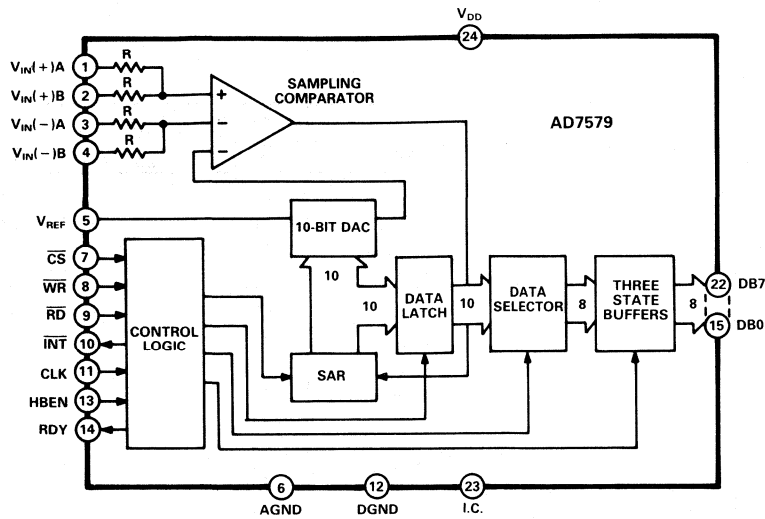
Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2,	10				Minimum Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	-1, 2	1	1	1			±LSB max
Differential Nonlinearity	DNL	-1, 2	0.9	0.9	0.9			±LSB max
Full-Scale Error	FSE	-1, 2	5	5	5			±LSB max
Zero Code Error	ZCE	-1, 2	2	2	2		Figure 6	±LSB max
Power Supply Rejection	PSR	-1, 2	0.5					±LSB max
Zero Code Error	ZCE	-1, 2	3	3	3		Figure 7 or Figure 8	±LSB max
Conversion Time	t_{CONV}	-1, 2	16.9	16.9	16.9			µs min
			18.5	18.5	18.5			µs max
Clock Range		-1, 2	250					kHz min
			2.5					MHz max
Signal-to-Noise Ratio	SNR	-1, 2	55	55	55			dB min
Total Harmonic Distortion	THD	-1, 2	-58	-58	-58			dB max
Attenuator Input Resistance		-1, 2	5	5	5			kΩ min
			15	15	15			kΩ max
Comparator Input Resistance		-1, 2	10	10	10		Figure 6	MΩ min
Reference Input Current	I_{REF}	-1, 2	1.5	1.5	1.5			mA max
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Input Current	I_{IN}	-1, 2	10	10	10		$V_{IN} = 0\text{ V or }V_{DD}$	±µA max
Input Capacitance	C_{IN}	-1, 2	10					pF max
Digital Output Low Voltage	V_{OL}	-1, 2	0.4	0.4	0.4		$I_{SINK} = 1.6\text{ mA}$	V max
Digital Output High Voltage	V_{OH}	-1, 2	4.0	4.0	4.0		$I_{SOURCE} = 400\text{ µA}$	V min
Floating State Leakage Current	I_{OUT}	-1, 2	10	10	10		$V_{OUT} = 0\text{ to }V_{DD}$	±µA max
Floating State Output Capacitance	C_{OUT}	-1, 2	10					pF max
Supply Current from V_{DD}	I_{DD}	-1, 2	10	10	10			mA max

NOTE

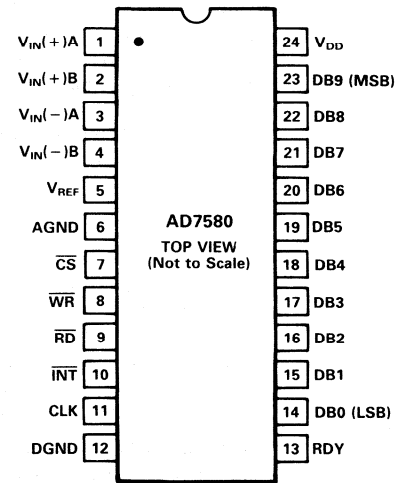
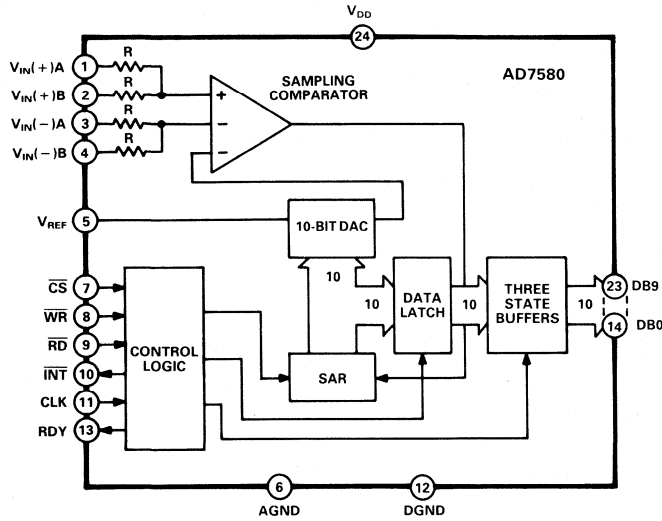
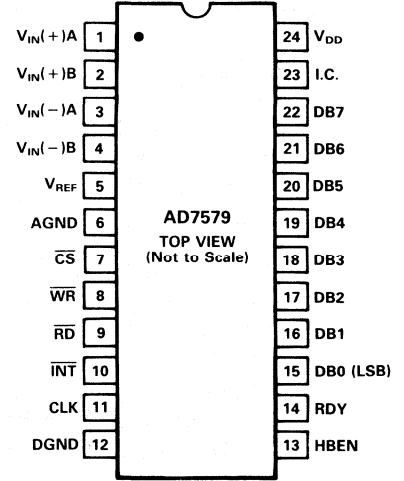
¹ $V_{DD} = +5\text{ V} \pm 5\%$, $V_{REF} = +2.5\text{ V}$, $AGND = DGND = 0\text{ V}$, $f_{CLK} = 2.5\text{ MHz}$.

Table 1.

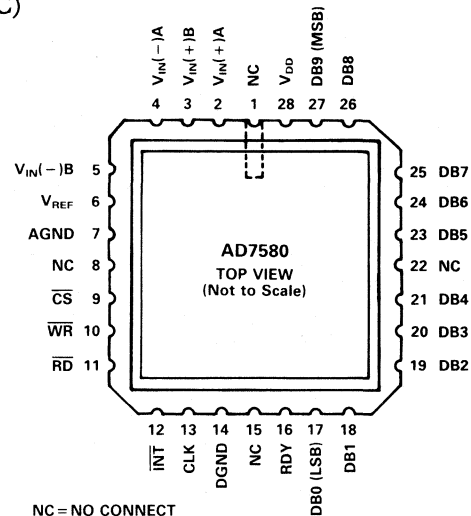
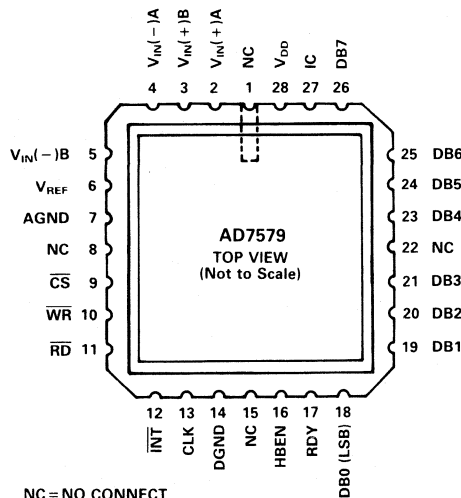
3.2.1 Functional Block Diagram and Terminal Assignments.



**Q Package
(DIP)**



**E Package
(LCC)**



NC = NO CONNECT

NC = NO CONNECT

AD7579/AD7580

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by Technology Group (81).

AD7579/AD7580 TIMING¹

Test	Symbol ^{2, 3, 4}	Device	Design Limit $T_{\min}$ to $T_{\max}$	Units
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1	-1, 2	0	ns min
$\overline{WR}$ Pulse Width	t_2	-1, 2	50	ns min
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3	-1, 2	0	ns min
$\overline{WD}$ to $\overline{INT}$ Propagation Delay	t_4	-1, 2	120	ns max
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_5	-1, 2	0	ns min
$\overline{RD}$ Pulse Width	t_6	-1, 2	t_{12}	ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_7	-1, 2	0	ns min
HBEN to $\overline{RD}$ Setup Time	t_8	-1, 2	30	ns min
HBEN to $\overline{RD}$ Hold Time	t_9	-1, 2	10	ns min
RDY Access Time	t_{10}	-1, 2	150	ns min
$\overline{RD}$ to $\overline{INT}$ Propagation Delay	t_{11}	-1, 2	120	ns max
Data Access Time After $\overline{RD}$	t_{12}	-1, 2	150	ns max
Data Hold Time, RDY Hold Time	t_{13}	-1, 2	10	ns min
			90	ns max

NOTES

¹Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20$ ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

² t_4 , t_{10} , t_{11} and t_{12} are measured with the load circuits of Figures 3 and 5 and are defined as the time required for an output to cross 0.8 V or 2.4 V.

³ t_{13} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 4.

⁴ $\overline{INT}$ and RDY are open-drain outputs and need 3 k Ω external pull-up resistors for operation.

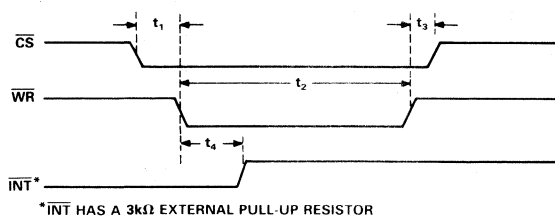


Figure 1. AD7579/AD7580 Start Cycle Timing

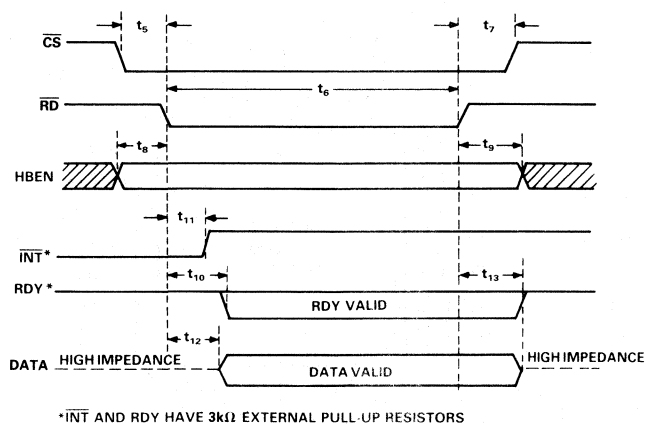


Figure 2. AD7579/AD7580 Read Cycle Timing

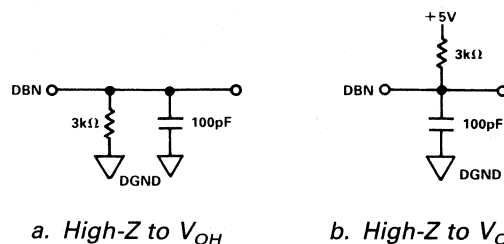


Figure 3. Load Circuits for Access Time Tests (t_{12})

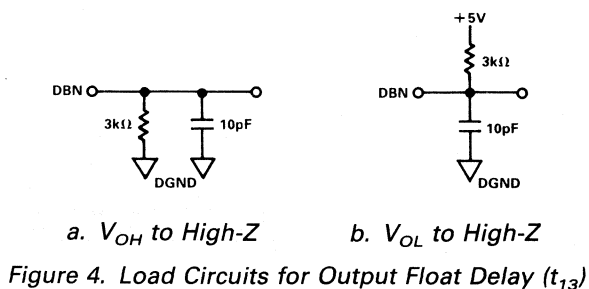


Figure 4. Load Circuits for Output Float Delay (t_{13})

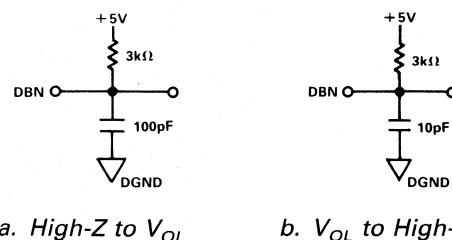


Figure 5. Load Circuits for $\overline{INT}$ Propagation Delays

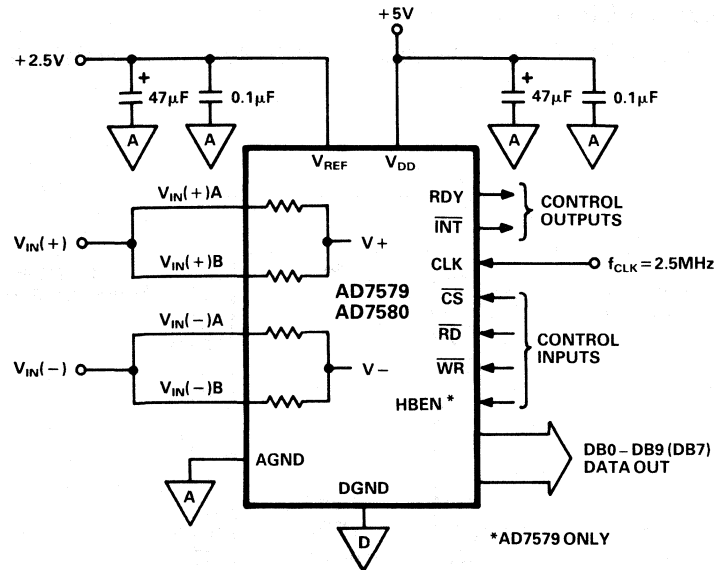
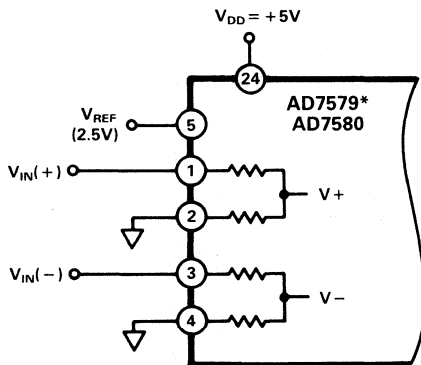


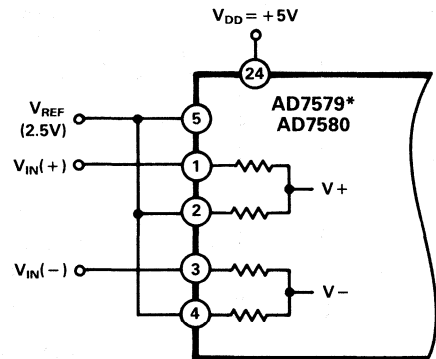
Figure 6. Unipolar 2.5 V Operational Diagram



*DECOUPLING CIRCUITRY AND CONTROL CIRCUITRY AS IN FIGURE 10

$V_{IN}(+) - V_{IN}(-)$	OUTPUT CODE
0V	00 0000 0000
0.00488V	00 0000 0001
2.500V	10 0000 0000
4.99512V	11 1111 1111

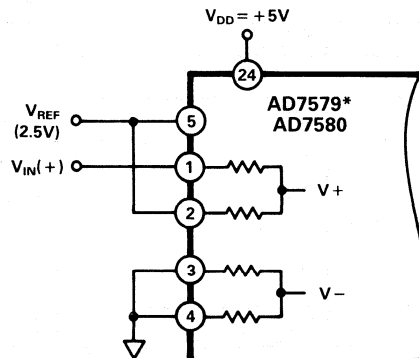
Figure 7. 5 V Span with 0 to 10 V CMR



*DECOUPLING CIRCUITRY AND CONTROL CIRCUITRY AS IN FIGURE 10

$V_{IN}(+) - V_{IN}(-)$	OUTPUT CODE
0V	00 0000 0000
0.00488V	00 0000 0001
2.500V	10 0000 0000
4.99512V	11 1111 1111

Figure 8. 5 V Span with -2.5 V to +7.5 V CMR



*DECOUPLING CIRCUITRY AND CONTROL CIRCUITRY AS IN FIGURE 10

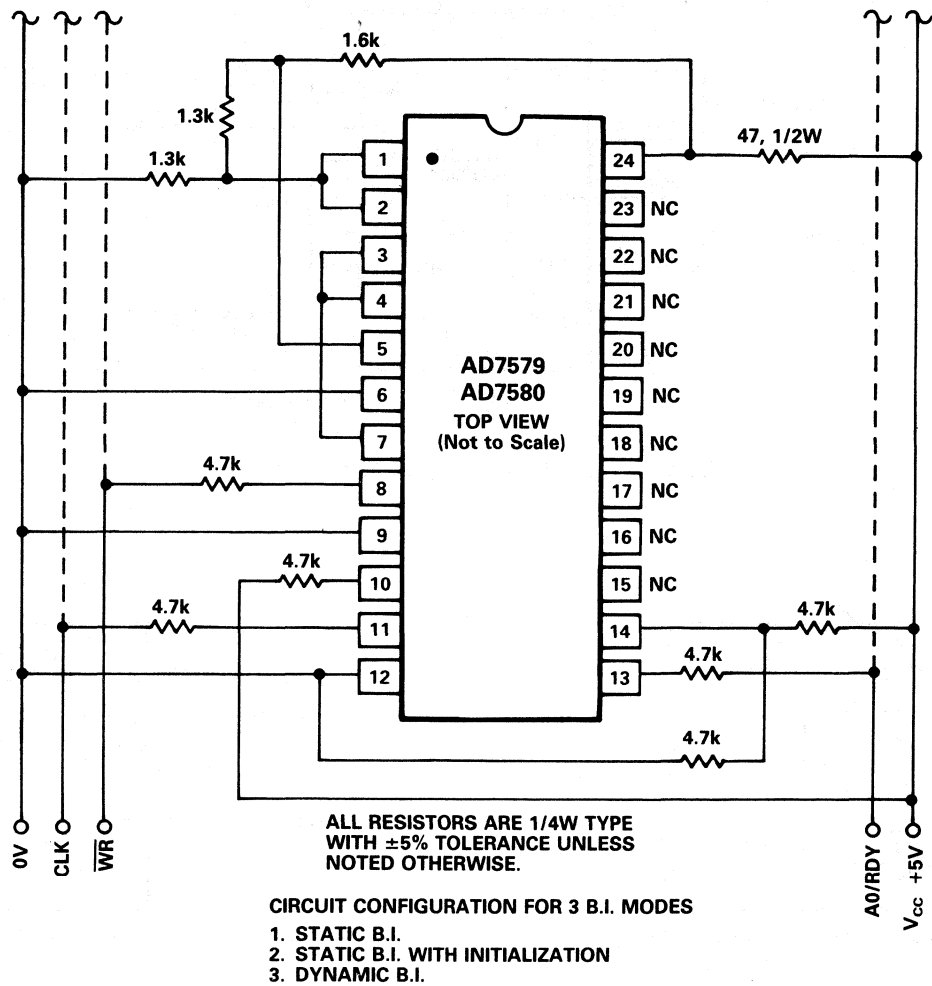
$V_{IN}(+)$	OUTPUT CODE
-2.500V	00 0000 0000
-2.49512V	00 0000 0001
0.00V	10 0000 0000
+2.49512V	11 1111 1111

Figure 9. Single-Ended Bipolar Operation, -2.5V to +2.5 V

AD7579/AD7580

4.2.1 Life Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7579/AD7580 signals applied to V_{CC} , CLK $\overline{WR}$, A0/RDY.

1. Static Burn-In

SEQ	V_{CC}	CLK	$\overline{WR}$	A0/RDY
Power-Up	V	0 V	0 V	0 V
Burn-In	5 V	0 V	5 V	0 V

2. Static Burn-In with Initialization

SEQ	V_{CC}	CLK	$\overline{WR}$	A0/RDY
Power-Up	5 V	0 V	0 V	0 V
Start Conversions	5 V	SQR-Wave FREQ = 20 kHz $V_{Lo} = 0 V$ $V_{Hi} = V_{CC}$	0 V	0 V
Min of 16 CLK-Periods				
	5 V	SQR-Wave	V_{CC}	0 V
Convert	5 V	SQR-Wave	V_{CC}	0 V
Min of 64 CLK Periods				
Burn-In	5 V	0 V	V_{CC}	0 V

3. Dynamic Burn-In

SEQ	V _{CC}	CLK	WR	A0/RDY
Power-Up	5 V	0 V	0 V	0 VC
Burn-In	5 V	SQR-Wave FREQ = 20 kHz V _{LO} = 0 V V _{HI} = V _{CC}	SQR-Wave FREQ = 20/128 kHz V _{LO} = 0 V V _{HI} = V _{CC}	SQR-Wave FREQ = 20/256 kHz V _{LO} = 0 V V _{HI} = V _{CC}

NOTES

WR signal = CLK divided by 128, TRIG on rising edge of CLK.

A0/RDY signal = CLK divided by 256 TRIG on rising edge of CLK.

6.0 Differential Applications.

Figure 10 shows the AD7579/AD7580 connected in the standard unipolar mode. Figure 11 and Table 2 show the ideal input/output transfer characteristics and the input/output code table, respectively. Code transitions occur between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, etc.). The output code is straight binary with 1 LSB = $FS/1024 = 2.5/1024 \text{ V} = 2.4 \text{ mV}$. The input voltage span is 2.5 V and the common mode range is 0 V to + 5 V, when $V_{DD} = 5 \text{ V}$. This means that the lowest voltage which can be tolerated at any of the analog inputs is 0 V, and the highest voltage which can be tolerated is + 5 V.

Figures 7 and 8 show the input attenuators on the AD7579/AD7580 configured to change the basic range of the device. A 5 V range can be configured by grounding one end of each attenuator and applying the

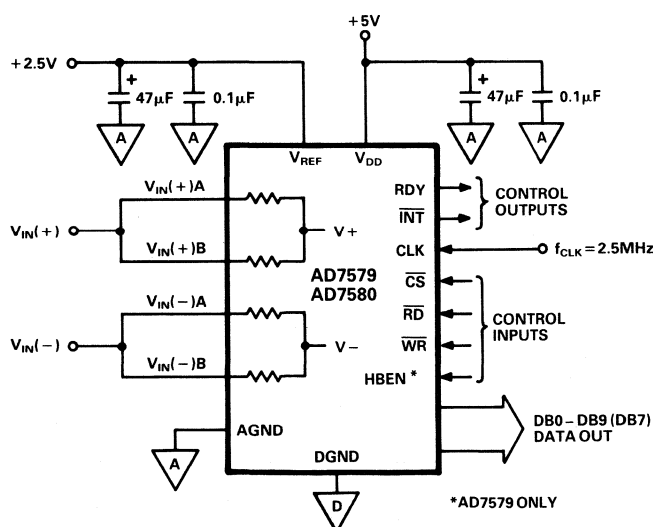


Figure 10. Unipolar 2.5 V Operational Diagram

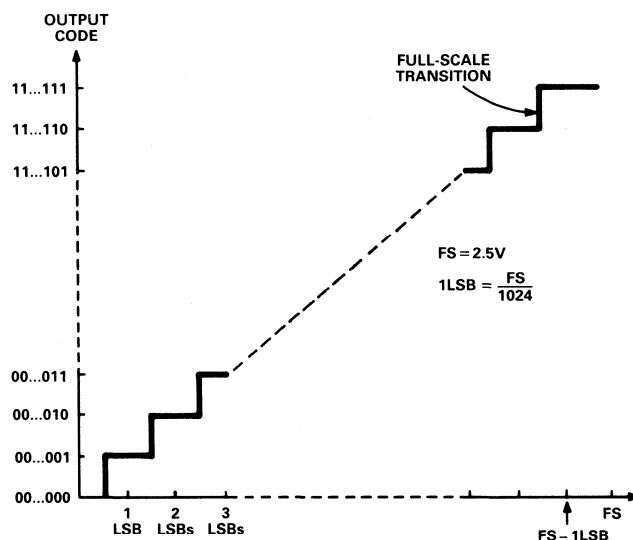


Figure 11. Ideal Input/Output Transfer Characteristics

Differential Analog Input, Volts	Digital Output DB9 DB0
+0.000	00 0000 0000
+0.00244	00 0000 0001
+1.24756	01 1111 1111
+1.25	10 0000 0000
+1.25244	10 0000 0001
+2.49512	11 1111 1110
+2.49756	11 1111 1111

Table 2. Input/Output Code Table For Figure 10

AD7579/AD7580

differential input to the other ends. This is shown in Figure 7. The span is 5 V and the common mode range is 0 to +10 V. In Figure 8, one end of each attenuator is tied to V_{REF} (2.5 V), and this allows each of the other legs to go to -2.5 V without causing the comparator input to go negative. Assuming V_{REF} is 2.5 V, the span of this circuit is 5 V and the common mode range is -2.5 V to +7.5 V. Note that reducing V_{DD} below 5 volts causes a corresponding reduction in CMR. See Specifications page for full details.

6.1 Single-Ended Applications.

In many cases, users of the AD7579/AD7580 will want to measure single-ended input voltages (i.e., ground referred signals). The circuits of Figures 6, 7 and 8 can be easily adapted to accept such signals. If $V_{IN(-)}$ in Figure 6 is tied to AGND, then the analog input range is 0 V to +2.5 V. By connecting $V_{IN(-)}$ of Figure 7 to AGND, the analog input range becomes 0 V to +5 V. Figure 8 can be modified as in Figure 9 to accept input voltages in the range -2.5 V to +2.5 V. Each of these circuits are special cases of the differential input circuits and are achieved by making the negative input to the internal comparator equal to AGND.

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 4-channel 12-bit analog-to-digital converter which uses the successive approximation technique to provide a conversion time of 100 μ s per channel. Conversion results are available in two bytes, 8LSBs and 4MSBs, via an 8-bit three-state output bus.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD7582T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Ceramic
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	–0.3V, +17V
V_{SS} to DGND	+0.3V, –7V
AGND to DGND	–0.3V, V_{REF} +0.3V
V_{CC} to DGND	–0.3V, V_{DD} +0.3V
V_{REF} to AGND	–0.3V, V_{DD} +0.3V
AIN (0-3) to AGND	–0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 18-21, 23-25)	–0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 10-17, 22)	–0.3V, V_{DD} +0.3V
Power Dissipation	
Up to $+75^\circ\text{C}$	1000mW
Derates above $+75^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	–55 $^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature	–65 $^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for D-28, E-28A and Q-28.

$\theta_{JA} = 120^\circ\text{C/W}$ for D-28, E-28A and Q-28.

AD7582 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ^{1, 2}	Units
Resolution	RES	– 1	12				Bits
Total Unadjusted Error ³	TUE	– 1	1	1	1	All Channels, AIN0-AIN3	± LSB max
Differential Nonlinearity	DNL	– 1	1	1	1	No Missing Codes Guaranteed	± LSB max
Gain Error	AE	– 1	1/4	1/4	1/4	All Channels, AIN0-AIN3 Gain Error TC is 5ppm/°C typ.	± LSB max
Offset Error	V _{OS}	– 1	1/4	1/4	1/4	All Channels, AIN0-AIN3 Offset Error TC is 5ppm/°C typ.	± LSB max
Channel-to-Channel Mismatch	CCM	– 1	1/4				± LSB max
Analog Input Range	V _{IN}	– 1	0 5				V min V max
Input Leakage Current	I _{LIN}	– 1	100	10	100	AIN0-AIN3; 0 to +5V	nA max
Reference Voltage Range	V _{REF}	– 1	4 6			Degraded Transfer Accuracy	V min V max
V _{REF} Input Reference Current	I _{REF}	– 1	1	1	1		mA max
Digital Input High Level	V _{IH}	– 1	2.4	2.4	2.4	$\overline{RD}$ (Pin 18), $\overline{CS}$ (Pin 19) WR (Pin 20), BYSL (Pin 21) A0 (Pin 24), A1 (Pin 25)	V min
Digital Input Low Level	V _{IL}		0.8	0.8	0.8		V max
Digital Input Leakage Current ⁴	I _{IN}		10	1	10		± µA max
Digital Input Capacitance	C _{IN}		10				pF max
Digital Input High Level	V _{IH}	– 1	3.0	3.0	3.0	CLK (Pin 23)	V min
Digital Input Low Level	V _{IL}		0.8	0.8	0.8		V max
Digital Input Low Current	I _{IL}		10	10	10		± µA max
Digital Input High Current	I _{IH}		1.5	1.5	1.5		
Digital Output High Voltage ⁵	V _{OH}	– 1	4.0	4.0	4.0	V _{CC} = +4.75V, I _{SOURCE} = 200µA DB0-DB7 (Pin 10-17), BUSY (Pin 22)	V min
Digital Output Low Voltage ⁵	V _{OL}	– 1	0.4	0.4	0.4	V _{CC} = +5.25V, I _{SINK} = 1.6mA DB0-DB7 (Pin 10-17), BUSY (Pin 22)	V max
Floating State Leakage Current		– 1	1	1	1	DB0-DB7 (Pin 10-17) V _{OUT} = 0V and V _{CC}	± µA max
Floating State Output Capacitance	C _{OUT}	– 1	15				pF max
Conversion Time with External Clock ⁶		– 1	100	100	100	f _{CLK} = 140kHz	µs min
Conversion Time with Internal Clock at +25°C		– 1	100	100		Using Recommended Clock Circuit Shown in Figure 5.	µs min
			150	150			µs max
Supply Current ⁷	I _{DD}	– 1	7.5	7.5	7.5		mA max
Supply Current ⁷	I _{SS}	– 1	7.5	7.5	7.5		mA max
Supply Current ⁷	I _{CC}	– 1	1.0	1.0	1.0	V _{IN} = V _{IL} or V _{IH}	mA max
$\overline{CS}$ to $\overline{WR}$ Setup Time	t ₁	– 1	0				ns min
WR Pulse Width (Internal Clock Operation)	t ₂ (INT)	– 1	280			(200ns min at +25°C)	ns min
WR Pulse Width (External Clock Operation) ⁸	t ₂ (EXT)	– 1	10				ns min
$\overline{CS}$ to $\overline{WR}$ Hold Time	t ₃	– 1	0				ns min
WR to BUSY Propagation Delay	t ₄	– 1	300			(100ns max at +25°C)	ns max
A0, A1 Valid to $\overline{WR}$ Setup Time	t ₅	– 1	0				ns min
A0, A1 Valid to $\overline{WR}$ Hold Time	t ₆	– 1	20				ns min
BUSY to $\overline{CS}$ Setup Time	t ₇	– 1	0				ns min
$\overline{CS}$ to $\overline{RD}$ Setup Time	t ₈	– 1	0				ns min

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ^{1,2}	Units
BYSL to $\overline{RD}$ Hold Time	t_{12}	-1	0				ns min
$\overline{RD}$ to Valid Data (Bus Access Time) ⁹	t_{13}	-1	280			(150ns max at +25°C)	ns max
$\overline{RD}$ to Three-State Output (Bus Relinquish Time) ¹⁰	t_{14}	-1	20				ns min
			180				ns max
						(130ns max at +25°C)	

NOTES

¹ $V_{DD} = +15V$; $V_{CC} = +5V$; $V_{SS} = -5V$; $V_{REF} = +5V$; $f_{CLK} = 140kHz$ external.

²All input control signals are specified with $t_r = t_f = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is time from V_{IH} , V_{IL} , or V_{OH} , V_{OL} .

³Includes full scale error, offset error and relative accuracy.

⁴Digital inputs = 0V or +5V.

⁵ I_{SINK} for Busy (Pin 22) is 1.0mA.

⁶Conversion time includes auto-zero cycle time.

⁷Power supply current is measured when the AD7582 is inactive i.e., $\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY} = \text{LOGIC HIGH}$.

⁸When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10 μs (see External Clock Operation).

⁹ t_{13} is defined as the time required for an output to cross 0.8V or 2.4V and is measured with the load circuits of Figure 3.

¹⁰ t_{14} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.

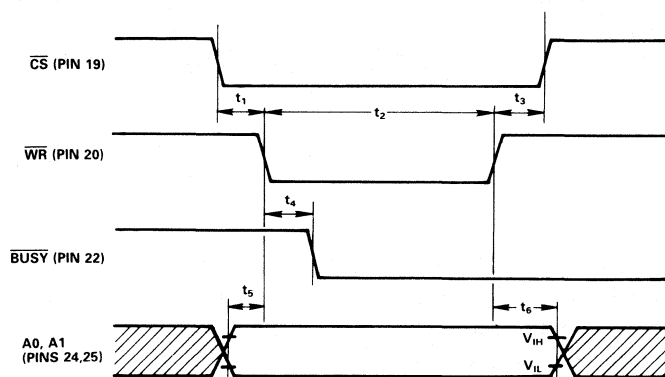
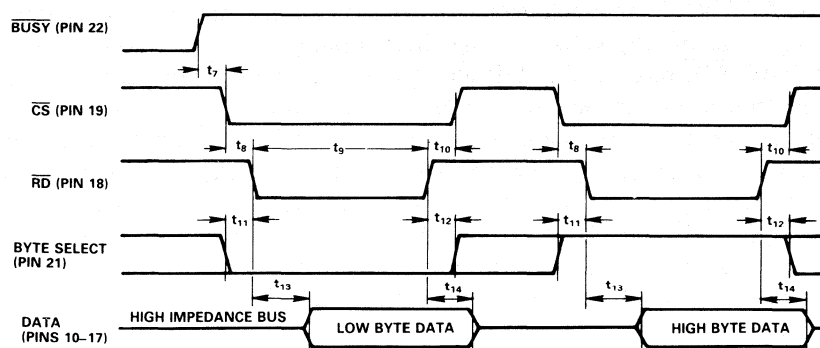
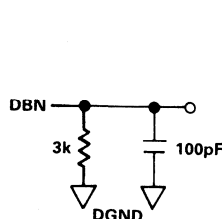


Figure 1. Start Cycle Timing

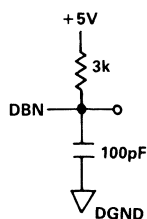


NOTES
THE TWO-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. FIGURE IS FOR LOW BYTE, HIGH BYTE ORDER.
IF BYSL CHANGES WHILE CS & RD ARE LOW THE DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

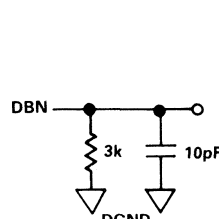
Figure 2. Read Cycle Timing



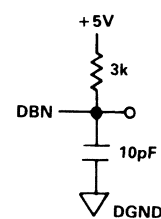
a. High-Z to V_{OH}



b. High-Z to V_{OL}



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 3. Load Circuits for Access Time Test (t_{13})

Figure 4. Load Circuits for Output Float Delay Test (t_{14}) REV. A

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 5 and the AD7582 operating waveforms are shown in Figure 6.

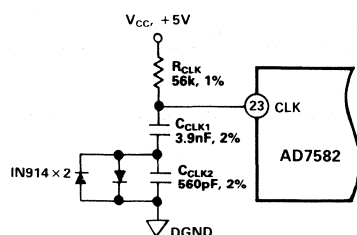


Figure 5. Circuitry Required for Internal Clock Operation

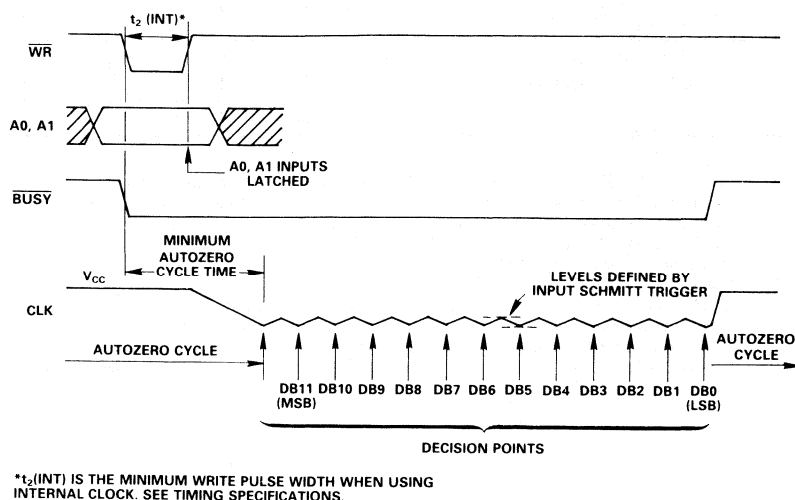


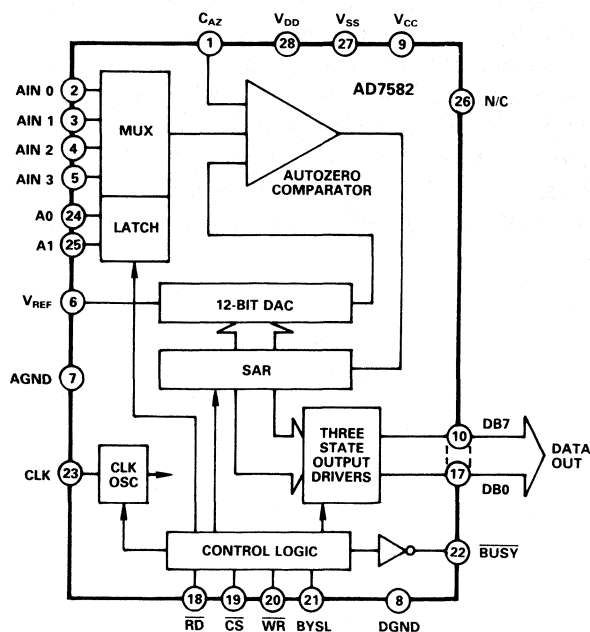
Figure 6. Operating Waveforms - Internal Clock

Between conversions ($\overline{\text{BUSY}} = \text{HIGH}$) the AD7582 is in the autozero cycle. When $\overline{\text{WR}}$ goes LOW (with $\overline{\text{CS}}$ LOW) to start a new conversion, the input multiplexer is switched to the selected channel N, via address inputs A0, A1. The autozero capacitor C_{AZ} now charges to $\text{AIN}_N - V_{\text{OS}}$ where V_{OS} is the input offset voltage of the autozero comparator.

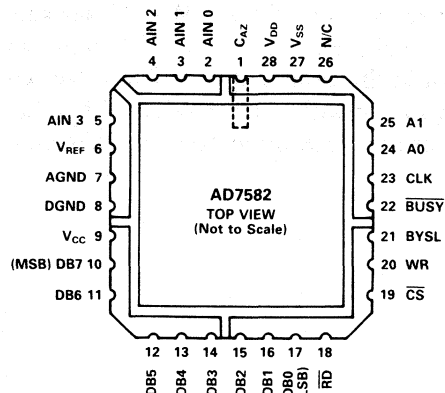
A minimum time of $10\mu\text{s}$ is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{\text{WR}}$ to remain LOW for this period of time since it is automatically provided by the AD7582. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2} , causing the voltage at the CLK input pin to slowly decay from V_{CC} . This occurs after $\overline{\text{WR}}$ returns HIGH; $\overline{\text{WR}}$ returning HIGH also latches the multiplexer address inputs A0, A1 (see Figure 6). The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK} . When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2} . The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 5 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

AD7582

3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

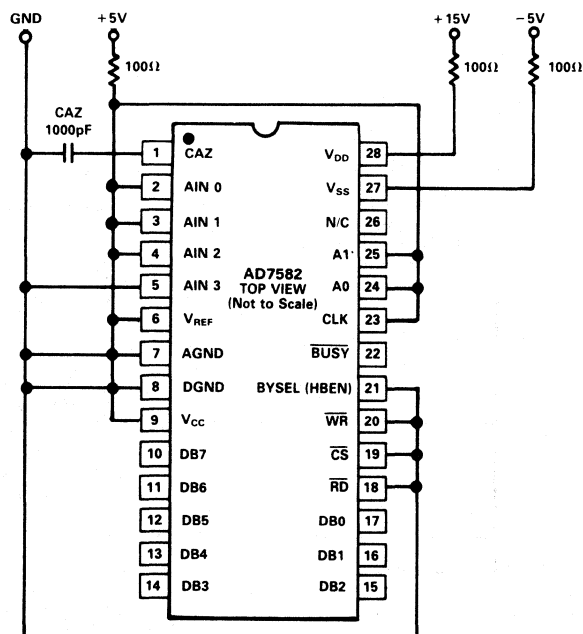


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS FOR PROTECTION ONLY
POWER μ P SEQUENCE: +15, +5, -5 IN THAT ORDER
-OR SIMULTANEOUSLY.



AD7590DI/AD7591DI/AD7592DI

1.1 Scope.

This specification covers the detail requirements for a family of protected (latch proof) dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25V$ above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent single-pole, single-throw analog switches. They differ only in that the switch control logic is inverted. The AD7592DI has two independent single-pole, double-throw switches.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
- 1	AD7590DIT(X)/883B
- 2	AD7591DIT(X)/883B
- 3	AD7592DIT(Y)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	(Y)	Package	Description
Q		Q-16	16-Pin Cerdip
E	E	E-20A	20-Terminal LCC
	Q	Q-14	14-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ C$)

V_{DD} to GND	+17V
V_{SS} to GND	-17V
Overvoltage at V_D (V_S), One Switch Only	$\pm 25V$
(1 Second Surge)	$V_{DD} + 25V$ or $V_{SS} - 25V$
(Continuous)	$V_{DD} + 20V$ or $V_{SS} - 20V$ or 20mA, whichever Occurs First
Switch Current (I_{DS} , Continuous)	50mA
Switch Current (I_{DS} , Surge)	
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	-0.3V to $V_{DD} + 0.3V$
Power Dissipation 14- & 16-Pin Cerdip	
Up to $+75^\circ C$	450mW
Derates above $+75^\circ C$ by	6mW/ $^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Operating Temperature	$-55^\circ C$ to $+125^\circ C$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ C/W$ for Q-14, Q-16 and E-20A
 $\theta_{JA} = 120^\circ C/W$ for Q-14, Q-16 and E-20A

AD7590DI/AD7591DI/AD7592DI – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Analog Signal Range	A_{IN}	- 1, 2, 3	± 10				V
On Resistance	R_{ON}	- 1, 2, 3	150	90	150	$-10 \leq V_S \leq +10V$, $I_{DS} = 1mA$; Test Circuit 1	Ω max
Leakage Current, Switch Open	$I_D(I_S)$ Off	- 1, 2, 3	200	5	200	Test Circuit 2	nA max
Output Current	$I_D(I_S)$ On	- 1, 2, 3	200	5	200	Test Circuit 3	nA max
	I_{OUT}	- 3	400	10	400	Test Circuit 4	nA max
Digital Input Low Voltage	V_{INL}	- 1, 2, 3	0.8	0.8	0.8		V max
Digital Input High Voltage	V_{INH}	- 1, 2, 3	2.4	2.4	2.4		V min
Digital Input High Current	I_{INH}	- 1, 2, 3	1.0	1.0	1.0	Inputs are MOS Gates. $V_{IN} = 0$ or V_{DD}	μA max
Digital Input Low Current	I_{INL}	- 1, 2, 3	1.0	1.0	1.0	Inputs are MOS Gates. $V_{IN} = 0$ or V_{DD}	μA max
Enable to Switch "ON"	t_{ON}	- 1 - 2	380 500			Test Circuit 5	ns max
Enable to Switch "OFF"	t_{OFF}	- 1 - 2	500 380			Test Circuit 5	ns max
Transition Time	t_{TRANS}	- 3	450			Test Circuit 6	ns max
Write Pulse Width	t_{WR}	- 1, 2, 3	400			See Figure 1	ns min
Address Setup Time	t_{AS}	- 1, 2, 3	400			See Figure 1	ns min
Address Hold Time	t_{AH}	- 1, 2, 3	40			See Figure 1	ns min
Power Supply Current	I_{DD}	- 1, 2, 3	2	1	2	Digital Inputs = V_{INL} or V_{INH}	mA max
	I_{SS}	- 1, 2, 3	1	1	1		mA max

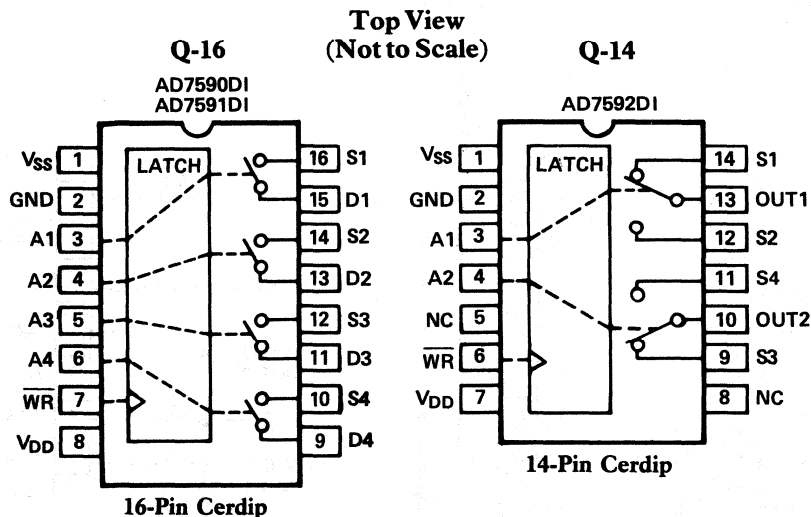
NOTE

¹ $V_{DD} = +15V$; $V_{SS} = -15V$ unless otherwise specified.

Table 1.

AD7590DI/AD7591DI/AD7592DI

3.2.1 Functional Block Diagram and Terminal Assignments.



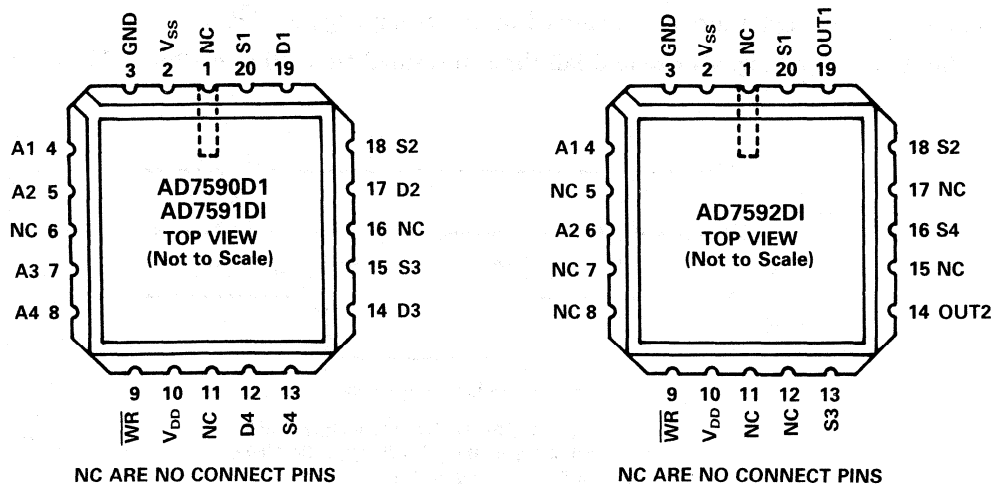
Control Logic ($\overline{WR}$ Held Low)

AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

AD7592DI: Address "HIGH" makes S1 to Out 1
and S3 to Out 2

E-20A 20-Contact LCC



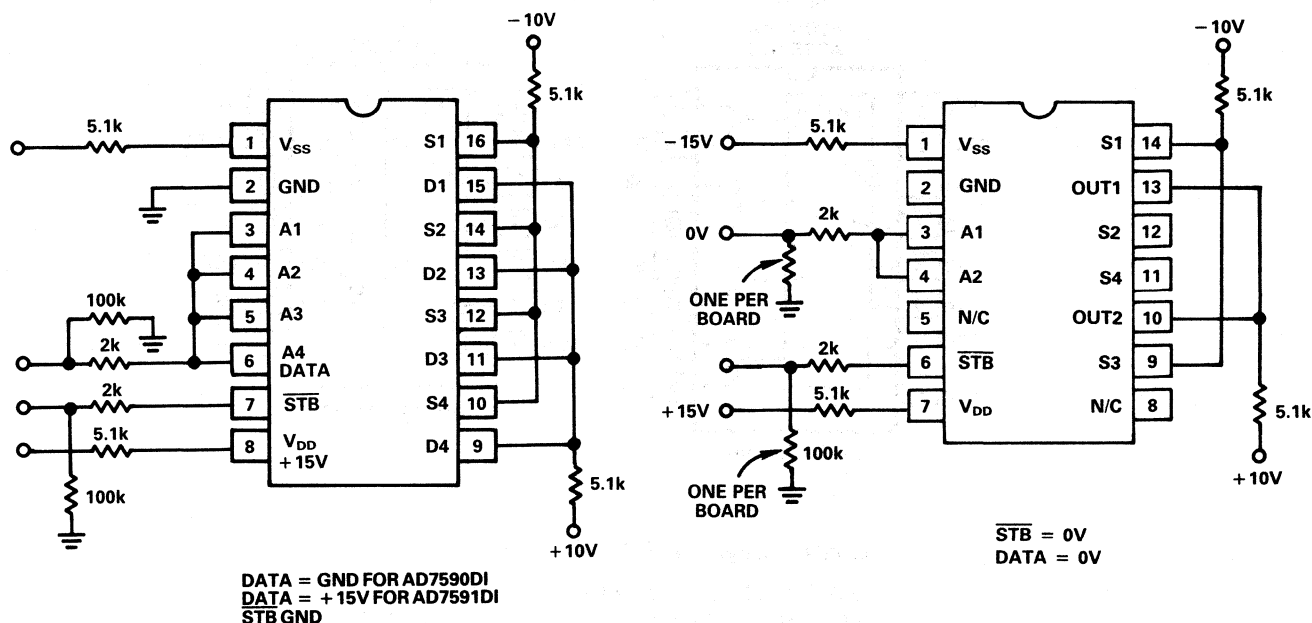
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

AD7590DI/AD7591DI/AD7592DI

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Timing and Control Sequence.

Figure 1 shows the timing sequence for latching the switch digital inputs (A1–A4). The latches are level sensitive and therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20\text{ns}$.

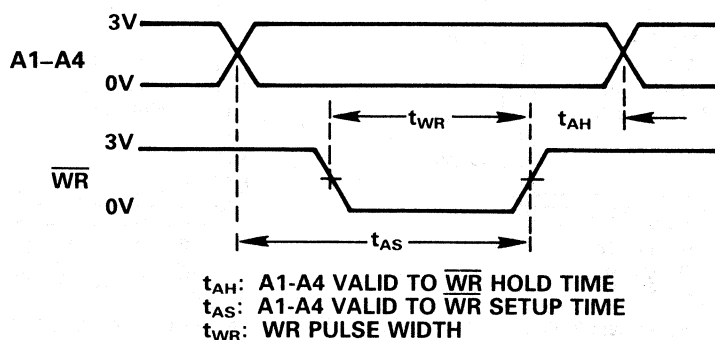
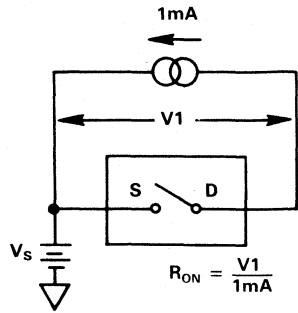
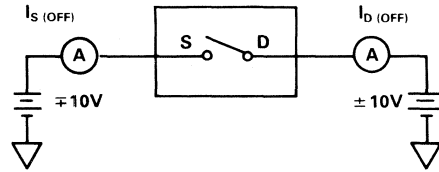


Figure 1. Timing and Control Sequence

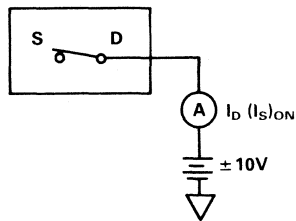
AD7590DI/AD7591DI/AD7592DI



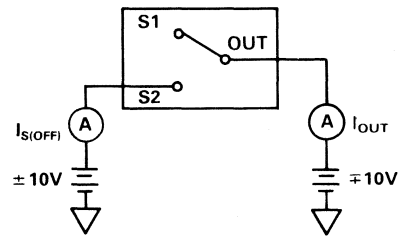
Test Circuit 1



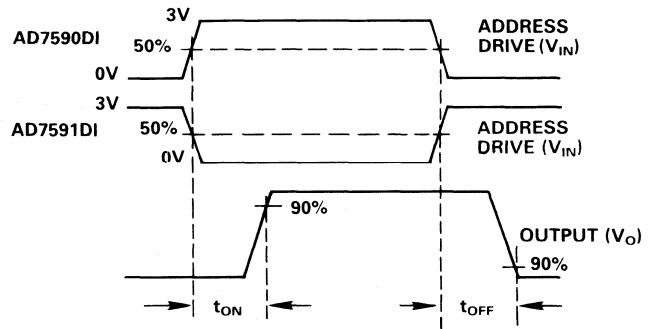
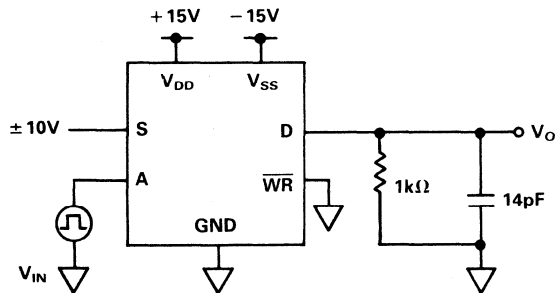
Test Circuit 2



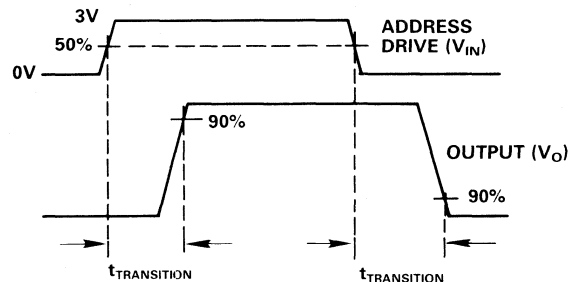
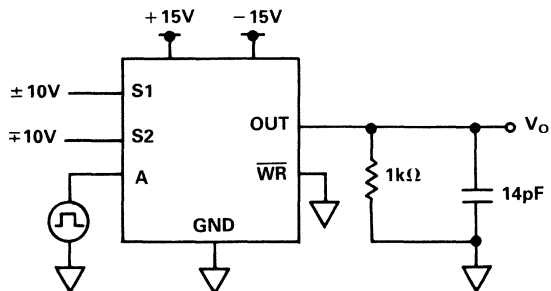
Test Circuit 3



Test Circuit 4
(AD7592DI Only)



Test Circuit 5
Switching Time of AD7590DI and AD7591DI, t_{ON} , t_{OFF} .



Test Circuit 6¹
Switching Time of AD7592DI, $t_{TRANSITION}$.

NOTE
¹ALL DIGITAL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF 3V. $t_R = t_F = 20\text{ns}$.

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS successive approximation 12-bit analog-to-digital converter allowing unipolar or bipolar input ranges and converting in 5 or 10 μ s.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7672T(X)05/883B and AD7672T(X)10/883B
-2	AD7672U(X)05/883B and AD7672U(X)10/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V_{DD} to DGND		-0.3 V, +7 V
V_{SS} to DGND		+0.3 V, -17 V
AGND to DGND		-0.3 V, $V_{DD} + 0.3$ V
AIN1, AIN2 to AGND		-15 V, +15 V
V_{REF} to AGND		$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V
Digital Input Voltage to DGND		-0.3 V, $V_{DD} + 0.3$ V
Digital Output Voltage to DGND		-0.3 V, $V_{DD} + 0.3$ V
Power Dissipation (to $+75^\circ\text{C}$)		450 mW
Derates above $+75^\circ\text{C}$		6 mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-24 and E-28A

AD7672 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	12				Minimum Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	-1	1	1	1		Tested Range ± 5 V	$\pm$ LSB max
		-2	3/4	1	3/4	1/2		
Differential Nonlinearity	DNL	-1, 2	0.9	0.9	0.9			$\pm$ LSB max
Unipolar Offset Error		-1	6	5	6		Input Range 0 to 5 V or 0 to 10 V	$\pm$ LSB max
		-2	4	5	4	3		
Unipolar Gain Error		-1	7	5	7		Input Range 0 to 5 V or 0 to 10 V	$\pm$ LSB max
		-2	6	5	6	4		
Bipolar Zero Error		-1	6	5	6		Input Range ± 5 V	$\pm$ LSB max
		-2	4	5	4	3		
Bipolar Gain Error		-1	7	5	7		Input Range ± 5 V	$\pm$ LSB max
		-2	6	5	6	4		
Unipolar Input Current		-1, 2	3.5	3.5	3.5		Input Range: 0 to 5 V or 0 to 10 V	mA max
Bipolar Input Current		-1, 2	1.75	1.75	1.75		Input Range: ± 5 V	$\pm$ mA max
Reference Input Current		-1, 2	-3					μ A max
Digital Input Low Level	V_{IL}	-1, 2	0.8	0.8	0.8		$\overline{CS}$, $\overline{RD}$, CLK IN	V max
Digital Input High Level	V_{IH}	-1, 2	2.4	2.4	2.4		$\overline{CS}$, $\overline{RD}$, CLK IN	V min
Digital Input Capacitance	C_{IN}	-1, 2	10				$\overline{CS}$, $\overline{RD}$, CLK IN	pF max
Digital Input Current (1)	I_{I1}	-1, 2	± 10	± 10	± 10		$\overline{CS}$, $\overline{RD}$, $V_{IN} = 0$ to V_{DD}	$\pm \mu$ A max
Digital Input Current (2)	I_{I2}	-1, 2	± 20	± 20	± 20		CLK IN, $V_{IN} = 0$ to V_{DD}	$\pm \mu$ A max
Digital Output Low Level	V_{OL}	-1, 2	0.4	0.4	0.4		DB11-DB0, $\overline{BUSY}$, CLK OUT	V max
Digital Output High Level	V_{OH}	-1, 2	4.0	4.0	4.0		DB11-DB0, $\overline{BUSY}$, CLK OUT	V min
Floating State Leakage Current	I_{OUT}	-1, 2	± 10	± 10	± 10		DB1-DB0	$\pm \mu$ A max
Floating State Output Capacitance	C_{OUT}	-1, 2	15					pF max
Conversion Time ² Synchronous Clock	t_{CONV}	-1, 2	5	5	5		$f_{CLK} = 2.5$ MHz	μ s max
			10	10	10		$f_{CLK} = 1.25$ MHz	
Conversion Time ² Asynchronous Clock	t_{CONV}	-1, 2	4.8	4.8	4.8		$f_{CLK} = 2.5$ MHz	μ s min
			5.2	5.2	5.2			μ s max
Conversion Time ² Asynchronous Clock	t_{CONV}	-1, 2	9.6	9.6	9.6		$f_{CLK} = 1.25$ MHz	μ s min
			10.4	10.4	10.4			μ s max
Supply Current from V_{SS}	I_{SS}	-1, 2	-12	-12	-12		$\overline{CS} = \overline{RD} = V_{DD}$ $AIN1 = AIN2 = 5$ V	mA max
Supply Current from V_{DD}	I_{DD}	-1, 2	7	7	7		$\overline{CS} = \overline{RD} = V_{DD}$ $AIN1 = AIN2 = 5$ V	mA max

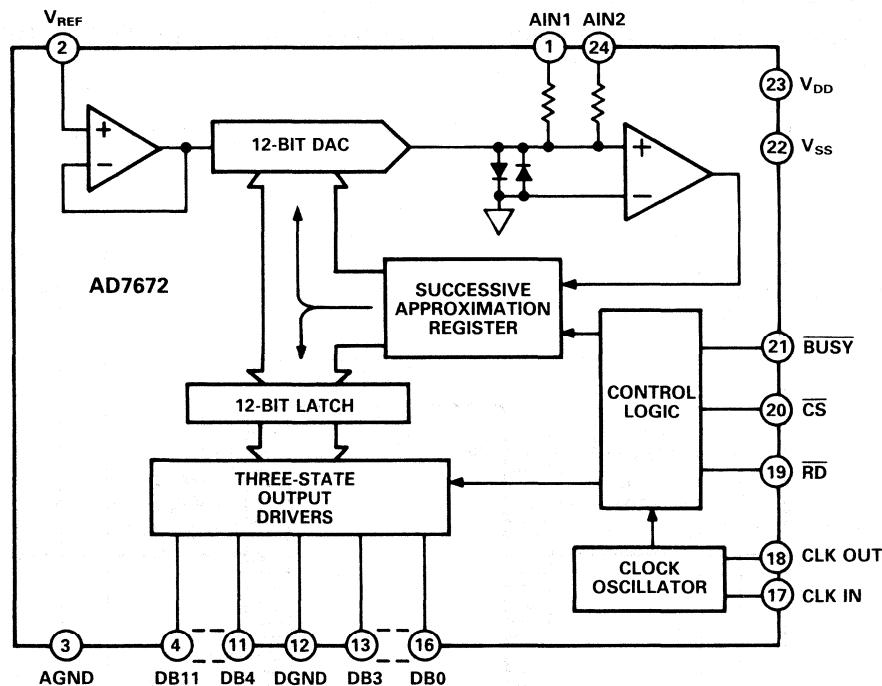
NOTES

¹ $V_{DD} = +5$ V $\pm 5\%$, $V_{SS} = -12$ V $\pm 10\%$, $V_{REF} = -5$ V $\pm 1\%$.

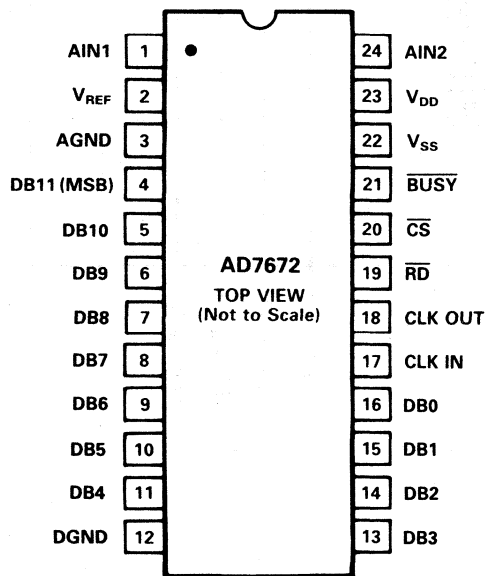
²Order AD7672T(X)05/883B or AD7672T(X)10/883B.

Table 1.

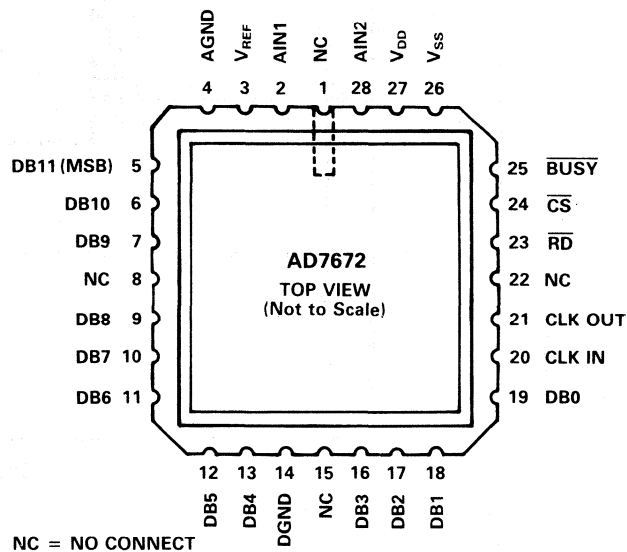
3.2.1 Functional Block Diagram and Terminal Assignments.



**Q Package
(DIP)**



**E Package
(LCC)**

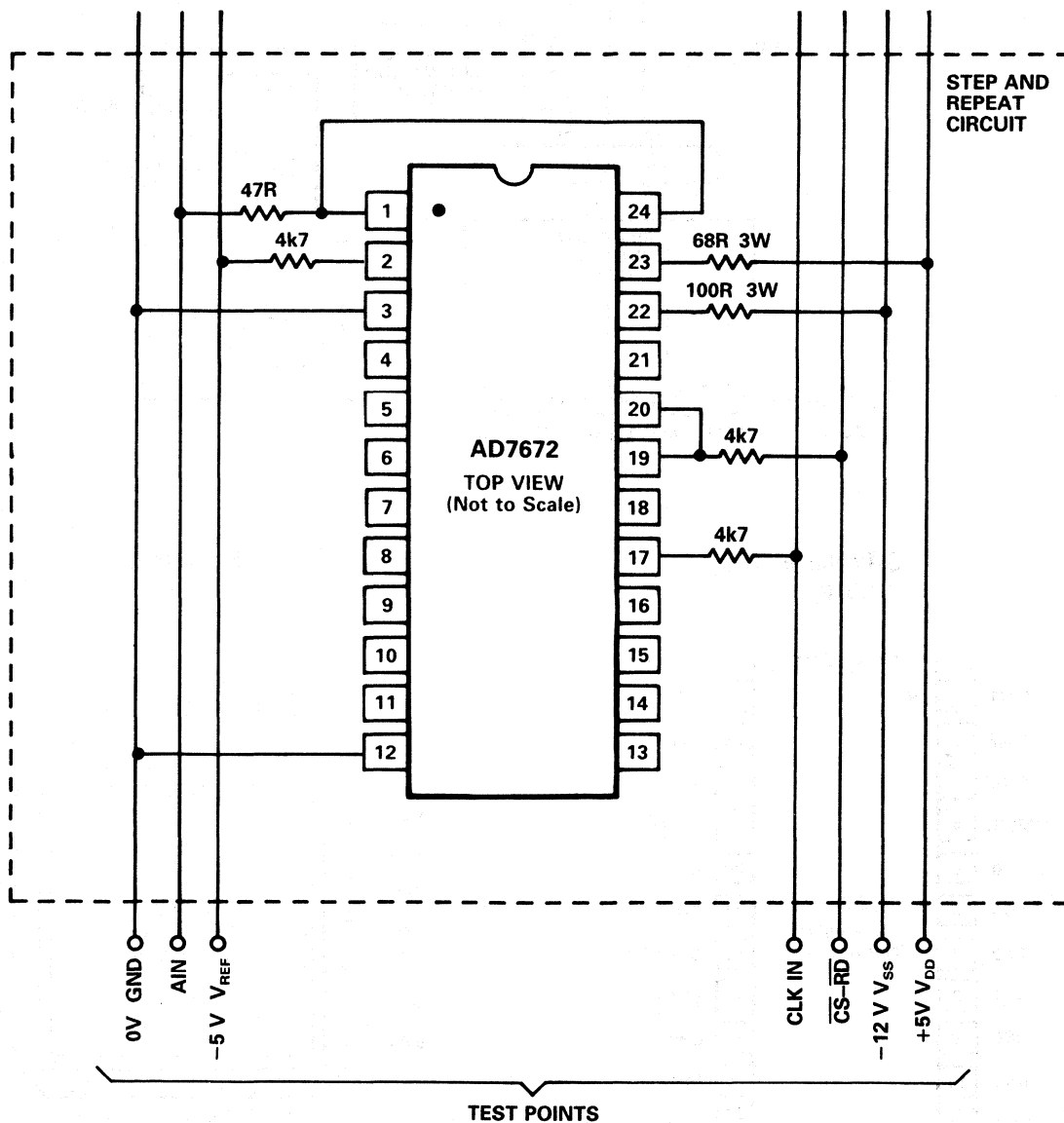


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by Technology Group (81).

4.2.1 Life Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7672 Burn-In**Power Supplies Max Current**

$V_{DD} = +5 \text{ V}$	$I_{DD} = 7 \text{ mA}$
$V_{SS} = -12 \text{ V}$	$I_{SS} = 12 \text{ mA}$
$V_{REF} = -5 \text{ V}$	$A_{IN} = 3.5 \text{ mA}$

Input Logic Levels are 0 to +5 V.

1. Static Burn-In

A_{IN} is tied to ground.

CLK IN Frequency is 35 kHz.

After power up $\overline{CS-RD}$ is taken high for 10 secs and is then taken low.

CLK IN is then removed and tied high.

2. Dynamic Burn-In

CLK IN is 100 kHz.

A_{IN} is driven with a 10 Hz sine wave input.

$\overline{CS-RD}$ is driven with a 160 μs period.

A_{IN} peak voltage 5 V.

Power Up Sequence

- (1) V_{DD}
- (2) V_{SS}
- (3) V_{REF}
- (4) Inputs

AD7672 Burn-In Philosophy**Static Burn-In**

1. After power-up the device performs a conversion on $\overline{CS-RD}$ going low.
2. With $A_{IN} = 0 \text{ V}$ and $\overline{CS-RD}$ held low after the conversion, the digital outputs will be at 0 volts ensuring that the o/p n-channels will be put under maximum stress for the period of burn-in.
3. At the end of conversion with $A_{IN} = 0 \text{ V}$, little or no differential stress will exist between the input devices of the comparator.

Dynamic Burn-In

$\overline{CS-RD}$ is brought low every 160 μs to start a new conversion and to ensure that the previous conversion has been completed.

AD7672 TIMING¹ SPECIFICATIONS

Test	Symbol	Device	Design Limit T _{min} to T _{max}	Units
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1	-1, 2	0	ns min
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2	-1, 2	270	ns max
Data Access Time after $\overline{RD}$, $C_L=100$ pF	t_3^2		170	ns max
$\overline{RD}$ Pulse Width	t_4	-1, 2	t_3	ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5	-1, 2	0	ns min
Data Setup Time after $\overline{BUSY}$	t_6^2	-1, 2	100	ns max
Bus Relinquish Time	t_7^3	-1, 2	20	ns min
			90	ns max
Delay Between Successive Read Operations	t_8	-1, 2	200	ns min

NOTES
¹All input control signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
² t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
³ t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

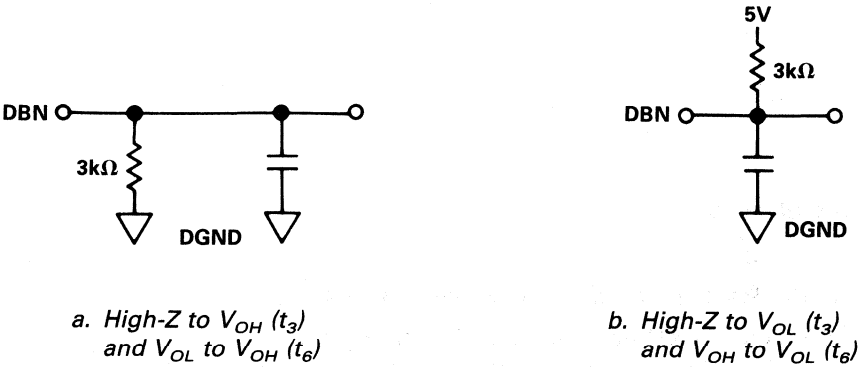


Figure 1. Load Circuits for Access Time

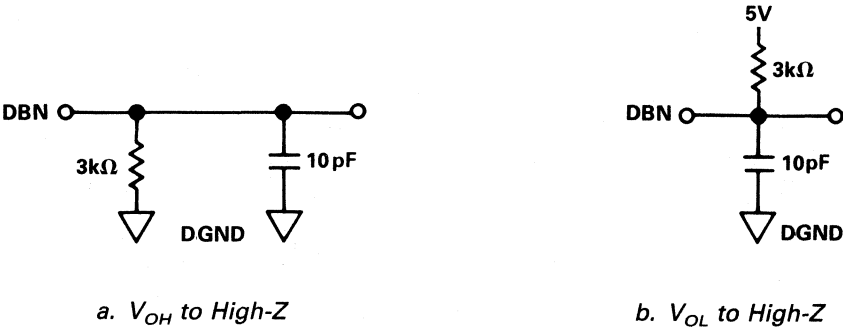


Figure 2. Load Circuits for Output Float Delay

6.0 Control Inputs Synchronization.

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock, conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach may be used: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT. This ensures a fixed conversion time that is 12.5 times the CLK IN frequency.

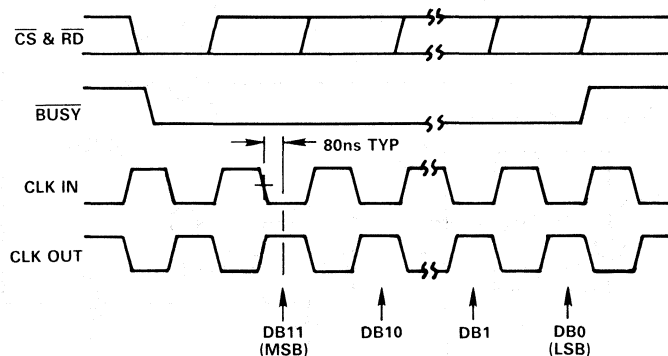


Figure 3. Operating Waveforms Using an External Clock Source for CLK IN

6.1 Driving the Analog Inputs.

During conversion current from the analog inputs is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4 MHz when CLK IN = 4 MHz). This causes voltage spikes (glitches) to appear at the analog inputs. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample-and-hold driving these inputs. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive one of the analog inputs is typically 11 mV with a 200 ns settling time. Suitable devices capable of driving the AD7672 AIN input are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

6.2 Analog Input Ranges.

The AD7672 provides three user selectable analog input ranges: 0 to +5 V, 0 to +10 V and ± 5 V. Figure 4 shows how to configure the two analog inputs (AIN1 and AIN2) for these ranges.

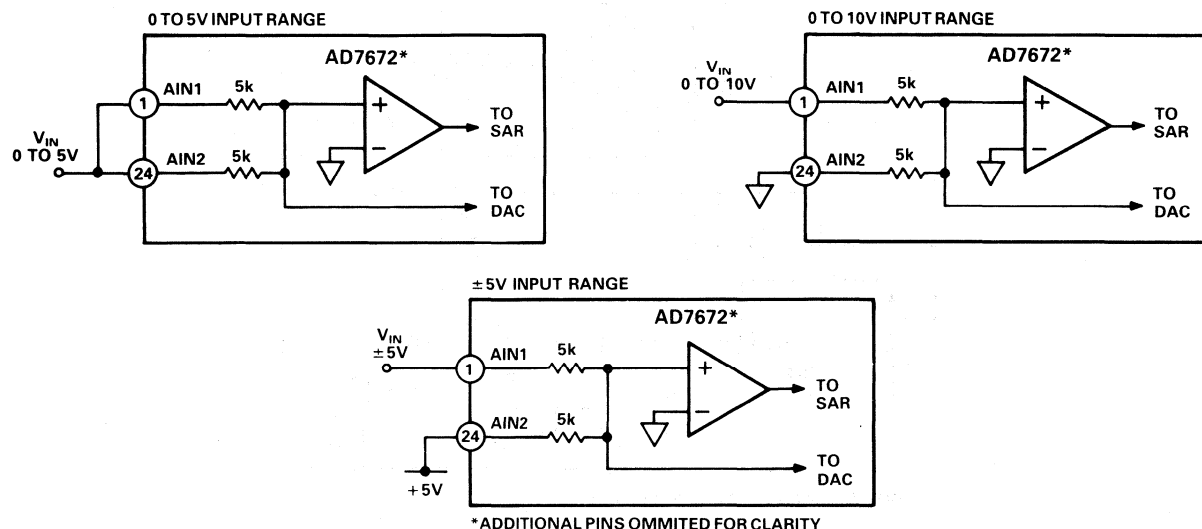


Figure 4. Analog Input Range Configurations

6.3 Unipolar Operation.

Figure 5 shows how to configure an AD584 to produce a reference voltage of -5 V for unipolar operation. The designed code transitions occur midway between successive integer LSB values (i.e., $1/2\text{ LSB}$, $3/2\text{ LSBs}$, $\dots\text{ FS} - 3/2\text{ LSBs}$).

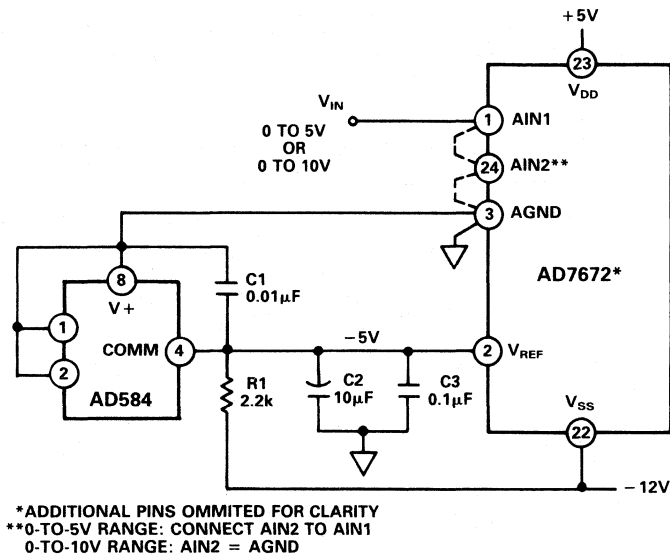


Figure 5. Unipolar Operation Using the AD584 as a Reference

6.4 Bipolar Operation.

Bipolar operation is achieved by providing a $+10\text{ V}$ span at the AIN1 input which is offset to $\pm 5\text{ V}$ by applying $+5\text{ V}$ at the AIN2 input. This requires two reference voltages, -5 V for the V_{REF} input and $+5\text{ V}$ for the AIN2 input. Figure 6 demonstrates how to produce these voltages from an AD584 and an inverting amplifier configuration. This device generates the required $\pm 5\text{ V}$ with a minimum of additional components. It also offers excellent temperature stability with voltage drifts as low as $1.5\text{ ppm}/^\circ\text{C}$.

The LSB size is $(10/4096)\text{ V} = 2.44\text{ mV}$.

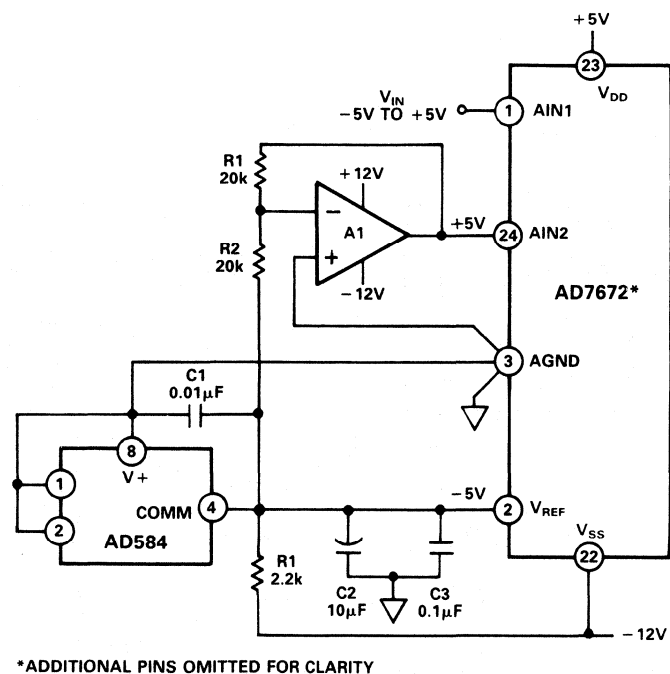


Figure 6. Bipolar Operation Using an AD584 and an AD711 Op Amp



LC²MOS

High Speed μ P-Compatible

8-Bit ADC with Track/Hold Function

AD7820

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS, microprocessor compatible 8-bit analog-to-digital converter which was a half-flash conversion technique to achieve a conversion time of 1.6 μ s. The converter has a 0V to +5V analog input voltage range with a single +5V supply.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7820T(X)/883B
-2	AD7820U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	0V, +7V
Digital Input Voltage to GND (Pins 6-8, 13)	-0.3V, V_{DD}
Digital Output Voltage to GND (Pins 2-5, 14-18)	-0.3V, V_{DD}
$V_{REF}(+)$ to GND	$V_{REF}(-)$, V_{DD}
$V_{REF}(-)$ to GND	0V, $V_{REF}(+)$
V_{IN} to GND	-0.3V, V_{DD}
Operating Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-20 and E-20A

AD7820 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
Resolution	RES	- 1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error ³	TUE	- 1	1	1	1			± LSB max
		- 2	1/2	1	1/2	1/2		
Analog Input Leakage Current	I_{IN}	- 1, 2	3	3	3			± µA max
Analog Input Capacitance	C_I	- 1, 2	45					pF typ
Reference Input Resistance	R_I	- 1, 2	1	1	1			kΩ min
			4	4	4			kΩ max
Digital Input High Level	V_{IH}	- 1, 2	2.4	2.4	2.4		$\overline{CS}, \overline{WR}, \overline{RD}$	V min
			3.5	3.5	3.5		Mode (Pin 7)	
Digital Input Low Level	V_{IL}	- 1, 2	0.8	0.8	0.8		$\overline{CS}, \overline{WR}, \overline{RD}$	V max
			1.5	1.5	1.5		Mode (Pin 7)	
Digital Input High Current	I_{IH}	- 1, 2	1.0	1.0	1.0		$\overline{CS}, \overline{RD}$	µA max
			3.0	3.0	3.0		$\overline{WR}$	
			200.0	200.0	200.0		Mode (Pin 7)	
Digital Input Low Current	I_{IL}	- 1, 2	1.0	1.0	1.0		$\overline{CS}, \overline{WR}, \overline{RD}$ Mode (Pin 7)	- µA max
Digital Input Capacitance	C_I	- 1, 2	8.0				$\overline{CS}, \overline{WR}, \overline{RD}$ Mode (Pin 7)	pF max
Digital Output High Level	V_{OH}	- 1, 2	4.0	4.0	4.0		DB0-DB7, $\overline{OFL}$, $\overline{INT}$ $I_{SOURCE} = 360\mu A$	V min
Digital Output Low Level	V_{OL}	- 1, 2	0.4	0.4	0.4		DB0-DB7, $\overline{OFL}$, $\overline{INT}$ $I_{SINK} = 1.6mA$	V max
Digital Output Low Level	V_{OL}	- 1, 2	0.4				$RDY; I_{SINK} = 2.6mA$	V max
Floating State Leakage Current	I_{OUT}	- 1, 2	3.0	3.0	3.0		DB0-DB7	µA max
Digital Output Capacitance	C_{OUT}	- 1, 2	8.0				(Typically 5pF)	pF max
Slew Rate, Tracking		- 1, 2	0.1					V/µs
Supply Current from V_{DD}	I_{DD}	- 1, 2	15.0	20.0	20.0		$\overline{CS} = \overline{RD} = 0V$	mA max
Power Supply Sensitivity		- 1, 2	1/4	1/4	1/4		$V_{DD} = 5V \pm 5\%$	± LSB max
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time	t_{CS}	- 1, 2	0					ns min
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time	t_{CH}	- 1, 2	0					ns min
$\overline{CS}$ to RDY Delay. Pull-Up Resistor 2kΩ ⁴	t_{RDY}	- 1, 2	100				70ns max at + 25°C	ns max
Conversion Time ($\overline{RD}$ Mode)	t_{CRD}	- 1, 2	2.5	1.6	2.5			µs max
Data Access Time ($\overline{RD}$ Mode) ⁵	t_{ACCO}	- 1, 2	$t_{CRD} + 50$				$(t_{CRD} + 20)$ ns max at + 25°C	ns max
$\overline{RD}$ to $\overline{INT}$ Delay ($\overline{RD}$ Mode) ⁴	t_{INTH}	- 1, 2	225				175ns max at + 25°C	ns max
Data Hold Time ⁶	t_{DH}	- 1, 2	100				60ns max at + 25°C	ns max
Delay Time Between Conversions	t_P	- 1, 2	600				500ns min at + 25°C	ns min
Write Pulse Width	t_{WR}	- 1, 2	600					ns max
			50					ns max
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}	- 1, 2	700				600ns max at + 25°C	ns min
Data Access Time ⁵ ($\overline{WR}/\overline{RD}$ Mode, See Fig. 4)	t_{ACCI}	- 1, 2	250				160ns max at + 25°C	ns max
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}	- 1, 2	225				140ns max at + 25°C	ns max
$\overline{WR}$ to $\overline{INT}$ Delay ⁴	t_{INTL}	- 1, 2	1700				1000ns max at + 25°C	ns max

Table 1. (Continued on next page)

REV. A

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Data Access Time ⁵ ($\overline{WR}/\overline{RD}$ Mode, See Fig. 3)	t_{ACC2}	-1, 2	110				70ns max at +25°C	ns max
$\overline{WR}$ to INT Delay (Stand-Alone Operation) ⁴	t_{IHWR}	-1, 2	150				100ns max at +25°C	ns max
Data Access Time after INT (Stand-Alone Operation)	t_{ID}	-1, 2	75				50ns max at +25°C	ns max

NOTES

¹ $V_{DD} = +5V$; $V_{REF}(+) = +5V$; $V_{REF}(-) = GND = 0V$ unless otherwise specified. Specifications apply for $\overline{RD}$ mode (Pin 7 = 0V).

²All input control signals are specified with $t_r = t_f = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

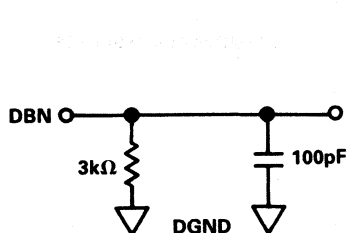
³Includes gain error, offset error and linearity error.

⁴ $C_L = 50pF$.

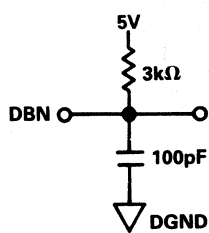
⁵Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

⁶Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

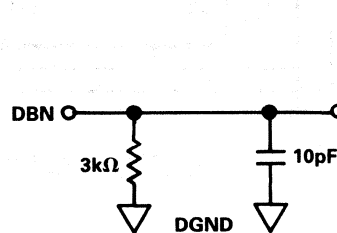
Table I.



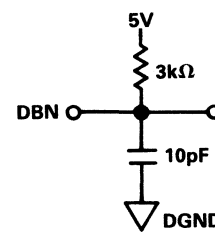
a. High-Z to V_{OH}



b. High-Z to V_{OL}



a. V_{OH} to High-Z

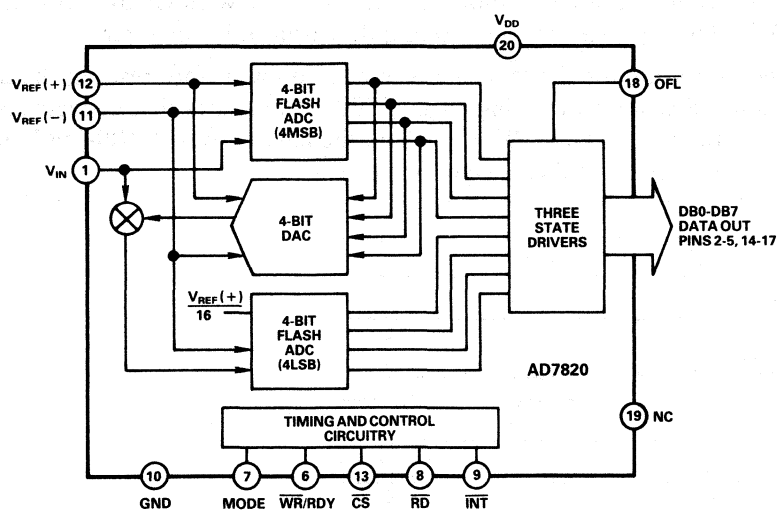


b. V_{OL} to High-Z

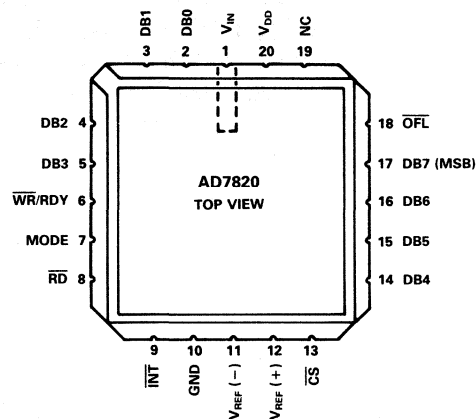
Figure 1. Load Circuits for Data Access Time Test

Figure 2. Load Circuits for Data Hold Time Test

3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)



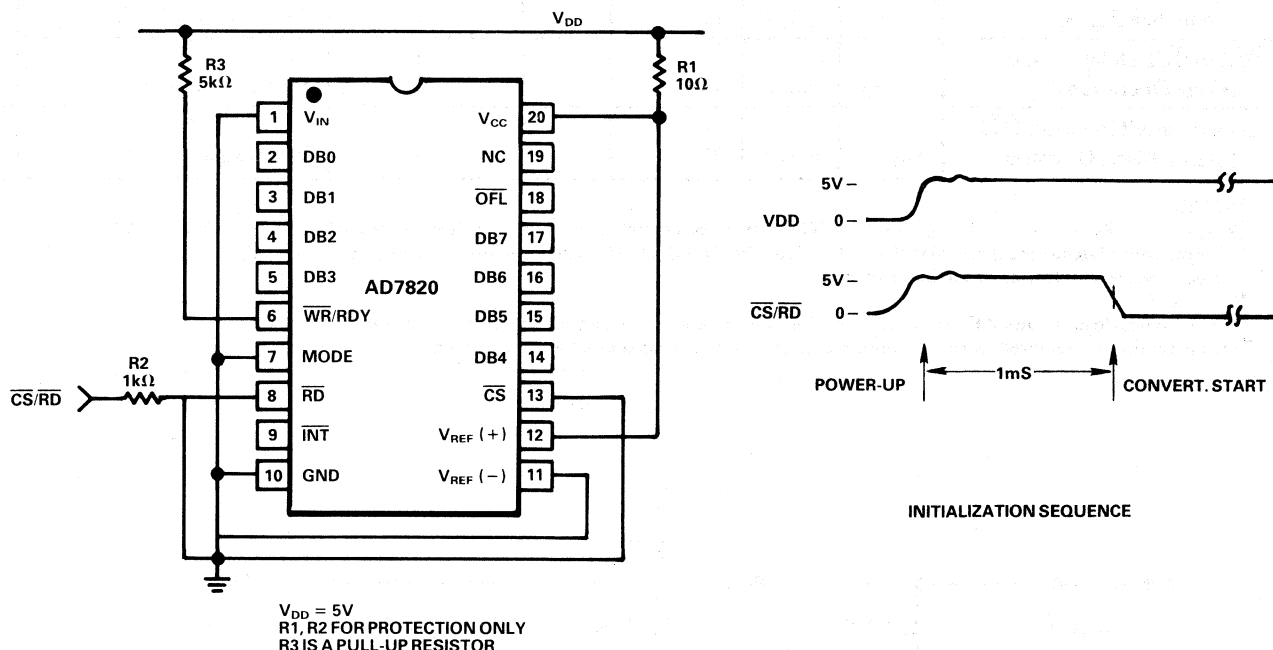
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

AD7820

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Digital Interface.

The AD7820 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low the converter is in the RD mode, with this pin high the AD7820 is set up for the WR-RD mode.

5.1 WR-RD Mode.

In the WR-RD mode, pin 6 is configured as the WRITE input for the AD7820. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 3). $\overline{INT}$ typically goes low 700ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

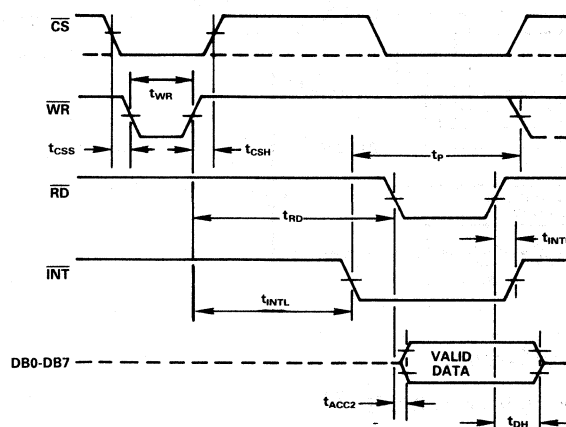


Figure 3. WR-RD Mode ($t_{RD} > t_{INTL}$)

The alternative option can be used to shorten the conversion time. To achieve this, the status of the $\overline{\text{INT}}$ line is ignored and $\overline{\text{RD}}$ can be brought low 600ns after the rising edge of $\overline{\text{WR}}$. In this case $\overline{\text{RD}}$ going low transfers the data result into the output latch and activates the data outputs (DB0-DB7). $\overline{\text{INT}}$ also goes low on the falling edge of $\overline{\text{RD}}$ and is reset on the rising edge of $\overline{\text{RD}}$ or $\overline{\text{CS}}$. The timing for this interface is shown in Figure 4.

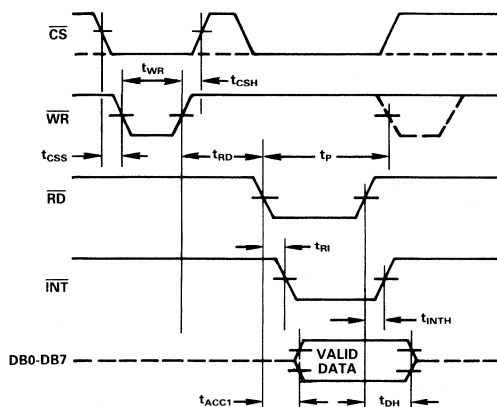


Figure 4. WR-RD Mode ($t_{RD} > t_{INTL}$)

5.2 RD Mode.

The timing diagram for the RD mode is shown in Figure 5. In the RD mode configuration, conversion is initiated by taking $\overline{\text{RD}}$ low. The $\overline{\text{RD}}$ line is then kept low until output data appears. It is very useful with microprocessors which can be forced into a WAIT state, with the microprocessor starting a conversion, waiting, and then reading data with a single READ instruction. In this mode, pin 6 of the AD7820 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{\text{CS}}$ and goes high impedance at the end of conversion. An $\overline{\text{INT}}$ line is also provided which goes low at the completion of conversion. $\overline{\text{INT}}$ returns high on the rising edge of $\overline{\text{CS}}$ or $\overline{\text{RD}}$.

The AD7820 can also be used in stand-alone operation in the WR-RD mode. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are tied low and a conversion is initiated by bringing $\overline{\text{WR}}$ low. Output data is valid typically 700ns after the rising edge of $\overline{\text{WR}}$. The timing diagram for this mode is shown in Figure 6.

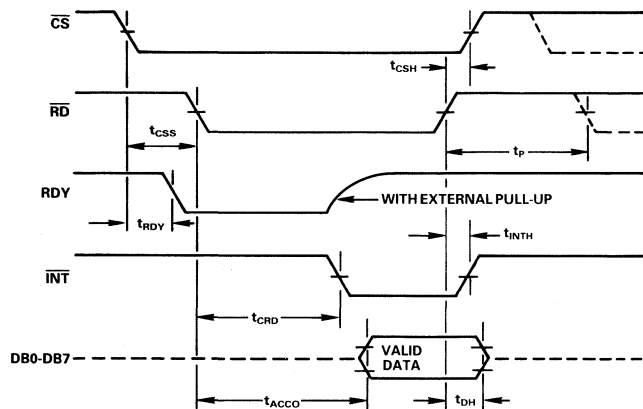


Figure 5. RD Mode

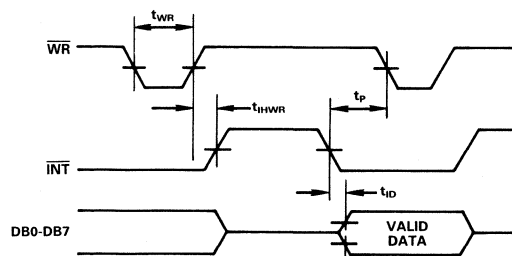


Figure 6. WR-RD Mode Stand-Alone Operation, $\overline{\text{CS}} = \overline{\text{RD}} = 0$

1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 8-bit sampling analog-to-digital converter. It features a conversion time of 660 ns and accepts unipolar or bipolar inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7821T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V_{DD} to GND		-0.3 V, +7 V
V_{SS} to GND		+0.3 V, -7 V
V_{IN} to GND		$V_{SS} - 0.3 \text{ V}$, $V_{DD} + 0.3 \text{ V}$
$V_{REF(+)}$ to GND		$V_{SS} - 0.3 \text{ V}$, $V_{DD} + 0.3 \text{ V}$
$V_{REF(-)}$ to GND		$V_{SS} - 0.3 \text{ V}$, $V_{DD} + 0.3 \text{ V}$
V_{IN} to GND		$V_{SS} - 0.3 \text{ V}$, $V_{DD} + 0.3 \text{ V}$
Digital Inputs to DGND		-0.3 V, $V_{DD} + 0.3 \text{ V}$
Digital Outputs to DGND		-0.3 V, $V_{DD} + 0.3 \text{ V}$
Power Dissipation (to $+75^\circ\text{C}$)		450 mW
Derates above $+75^\circ\text{C}$		6 mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-20 and E-20A

AD7821 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
Resolution	RES	–1	8				This Is the Minimum Resolution for Which No Missing Codes Are Guaranteed.	Bits
Total Unadjusted Error ³	TUE	–1	1	1	1			±LSB max
Analog Input Leakage Current	I_{IN}	–1	3	3	3			±μA max
Analog Input Capacitance	C_I	–1	55					pF typ
Reference Input Resistance	R_I	–1	1	1	1			kΩ min
			4	4	4			kΩ max
Digital Input High Level	V_{IH}	–1	2.4	2.4	2.4		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	V min
			3.5	3.5	3.5		Mode (Pin 7)	
Digital Input Low Level	V_{IH}	–1	0.8	0.8	0.8		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	V max
			1.5	1.5	1.5		Mode (Pin 7)	
Digital Input High Current	I_{IH}	–1	1.0	1.0	1.0		$\overline{CS}$, $\overline{RD}$	μA max
			3.0	3.0	3.0		$\overline{WR}$	
			200.0	200.0	200.0		Mode (Pin 7)	
Digital Input Low Current	I_{IL}	–1	1.0	1.0	1.0		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Mode (Pin 7)	–μA max
Digital Input Capacitance	C_I	–1	8.0				$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Mode (Pin 7)	pF max
Digital Output High Level	V_{OH}	–1	4.0	4.0	4.0		DB0–DB7, $\overline{OFL}$, $\overline{INT}$ $I_{SOURCE} = 360 \mu A$	V min
Digital Output Low Level	V_{OL}	–1	0.4	0.4	0.4		DB0–DB7, $\overline{OFL}$, $\overline{INT}$ $I_{SINK} = 1.6 mA$	V max
			0.4				RDY: $I_{SINK} = 2.6 mA$	
Floating State Leakage Current	I_{OUT}	–1	3.0	3.0	3.0		DB0–DB7	μA max
Digital Output Capacitance	C_{OUT}	–1	8.0				(Typically 5 pF)	pF max
Slew Rate Tracking		–1	1.6				Typically 2.36	V/μs
Supply Current from V_{DD}	I_{DD}	–1	25	25	25		$\overline{CS} = \overline{RD} = 0 V$	mA max
Supply Current from V_{SS}	I_{SS}	–1	100	100	100		$\overline{CS} = \overline{RD} = 0 V$	μA max
Power Supply Sensitivity		–1	1/4	1/4	1/4		$V_{DD} = 5 V \pm 5\%$	±LSB max
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time	t_{CS}	–1	0					ns min
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time	t_{CH}	–1	0					ns min
$\overline{CS}$ to RDY Delay. Pull-Up Resistor 2 kΩ ⁴	t_{RDY}	–1	100				70 ns max at +25°C	ns max
Conversion Time ($\overline{RD}$ Mode)	t_{CRD}	–1	975				700 ns max at +25°C	ns max
Data Access Time ($\overline{RD}$ Mode) ⁵	t_{ACCO}	–1	$t_{CRD} + 75$				($t_{CRD} + 50$) ns max at +25°C	ns max
$\overline{RD}$ to $\overline{INT}$ Delay ($\overline{RD}$ Mode) ⁴	t_{INTH}	–1	90				80 ns max at +25°C	ns max
Data Hold Time ⁶	t_{DH}	–1	80				60 ns max at +25°C	ns max
			15				15 ns min at +25°C	ns min
Delay Time Between Conversions	t_P	–1	500				350 ns min at +25°C	ns min
Write Pulse Width	t_{WR}	–1	400					ns min
			10				250 ns min at +25°C	μs max
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}	–1	450				250 ns min at +25°C	ns min
Data Access Time ⁵ ($\overline{WR}/\overline{RD}$ Mode, See Figure 4)	t_{ACCI}	–1	275				185 ns min at +25°C	ns max
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}	–1	220				150 ns max at +25°C	ns max

Table 1. (Continued on next page)

REV. A

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
$\overline{WR}$ to $\overline{INT}$ Delay ⁴	t_{INTL}	-1	700				500 ns max at +25°C	ns max
Access Time ⁵ ($\overline{WR}/\overline{RD}$ Mode, See Figure 3)	t_{ACC2}	-1	130				90 ns max at +25°C	ns max
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation) ⁴	t_{IHWR}	-1	120				80 ns max at +25°C	ns max
Data Access Time after $\overline{INT}$ (Stand-Alone Operation)	t_{ID}	-1	70				45 ns max at +25°C	ns max

NOTES

¹ $V_{DD} = +5\text{ V}$; $V_{REF(+)} = +5\text{ V}$; $V_{REF(-)} = \text{GND} = 0\text{ V}$ unless otherwise specified. Specifications apply for $\overline{RD}$ mode (Pin 7 = 0 V).

²All input control signals are specified with $t_r = t_f = 20\text{ ns}$ (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.

³Includes gain error, offset error and linearity error.

⁴ $C_L = 50\text{ pF}$.

⁵Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

⁶Defined as the time required for the data lines to changed 0.5 V when loaded with the circuits of Figure 2.

Table 1.

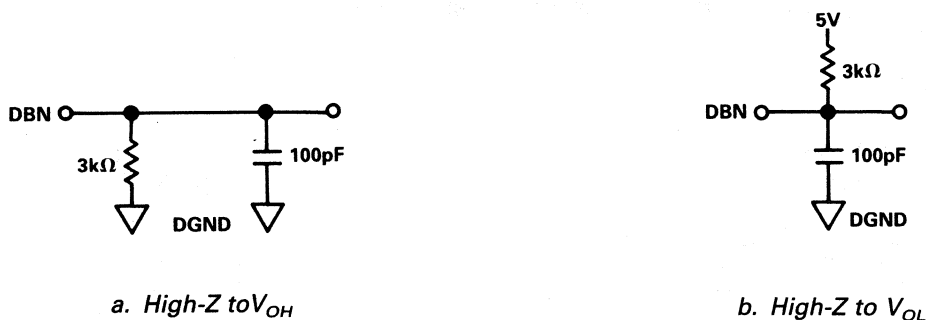


Figure 1. Load Circuits for Data Access Time Test

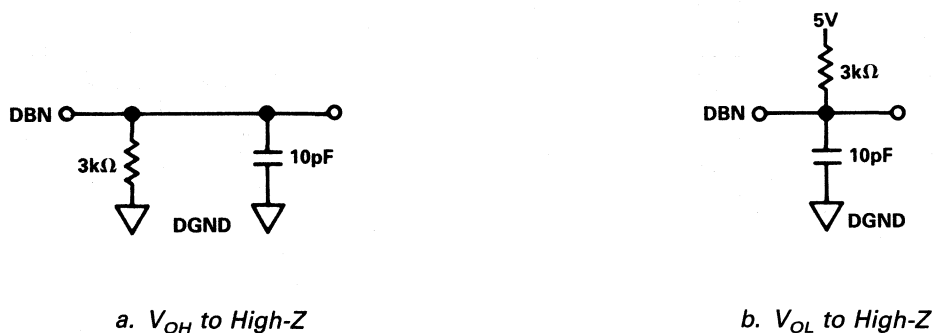
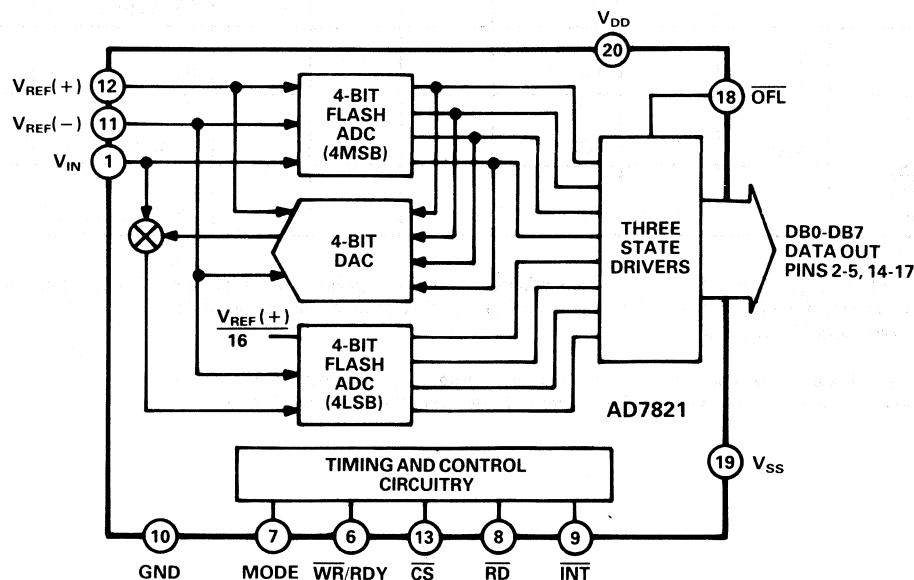


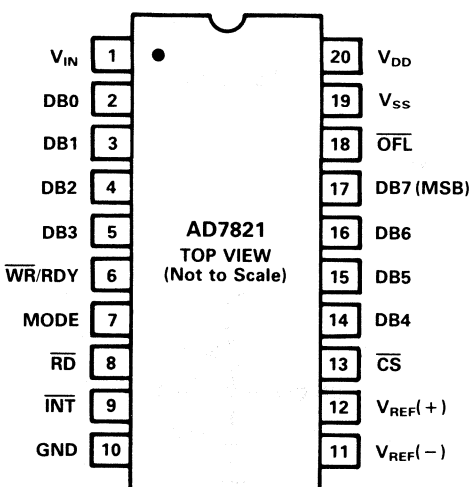
Figure 2. Load Circuits for Data Hold Time Test

AD7821

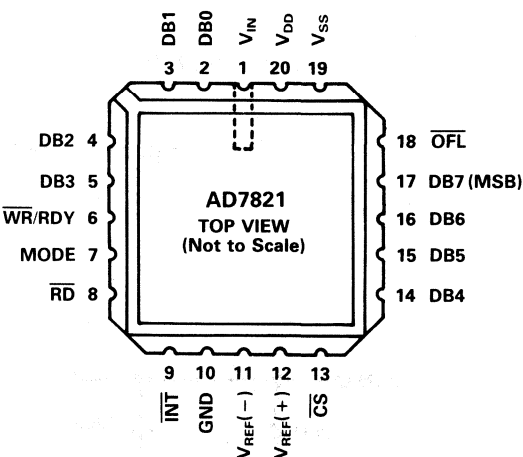
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package
(DIP)



E Package
(LCC)

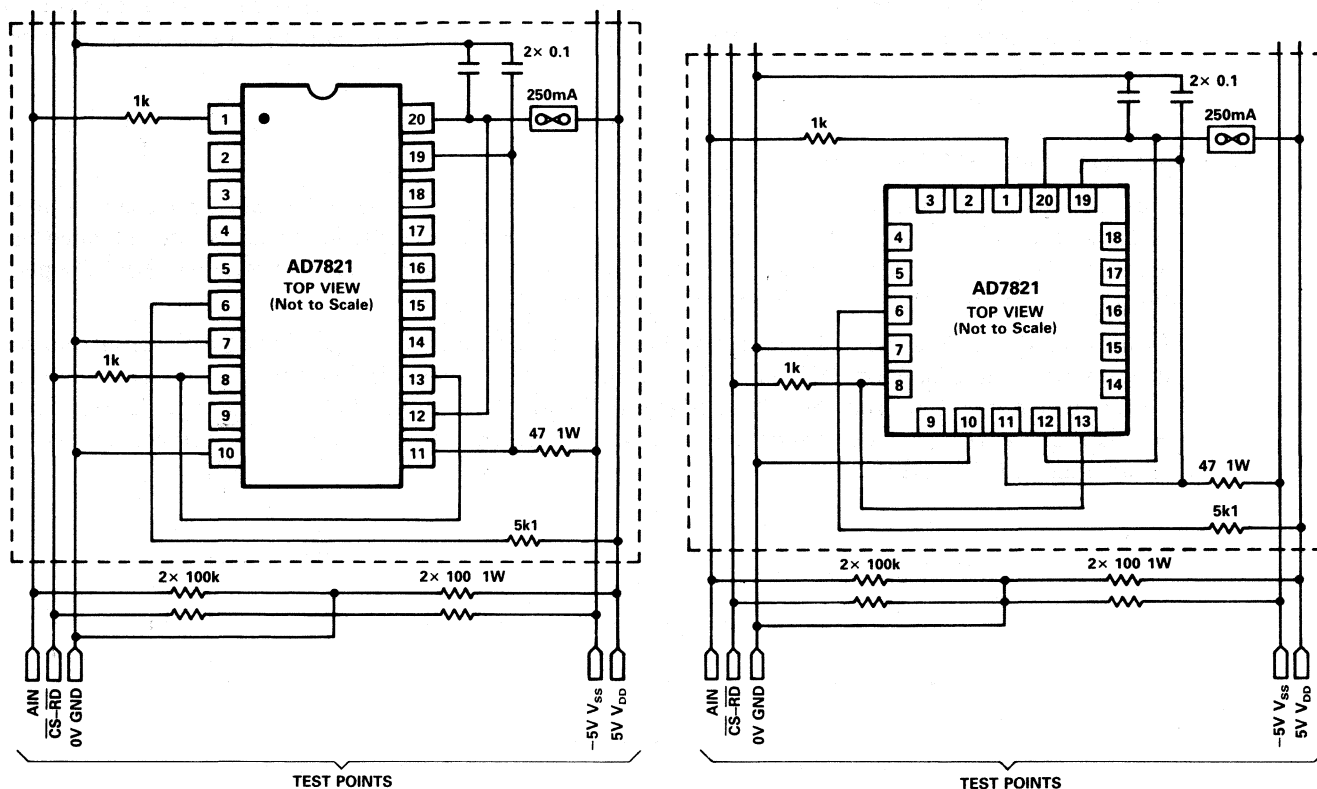


3.2.4 Microcircuit Technology Group.

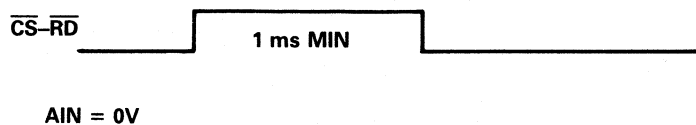
This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

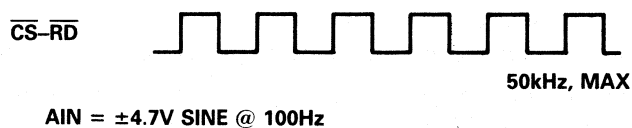
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7821 Edge Connections



Static Burn-In Initialization



Dynamic Burn-In Signals

6.0 Digital Interface.

The AD7821 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low, the converter is in the RD mode; with this pin high, the AD7821 is set up for the WR-RD mode.

The RD mode is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when the conversion is complete. The WR-RD mode does not require microprocessor WAIT states. A WRITE operation (i.e., $\overline{CS}$ and $\overline{WR}$ are taken low) initiates a conversion, and a READ operation reads the result when the conversion is complete.

6.1 RD Mode (MODE = 0).

The timing diagram for the RD mode is shown in Figure 3. This mode is intended for use with microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low (READ operation). Both $\overline{CS}$ and $\overline{RD}$ are then kept low until output data appears.

In this mode, Pin 6 of the AD7821 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low when a conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

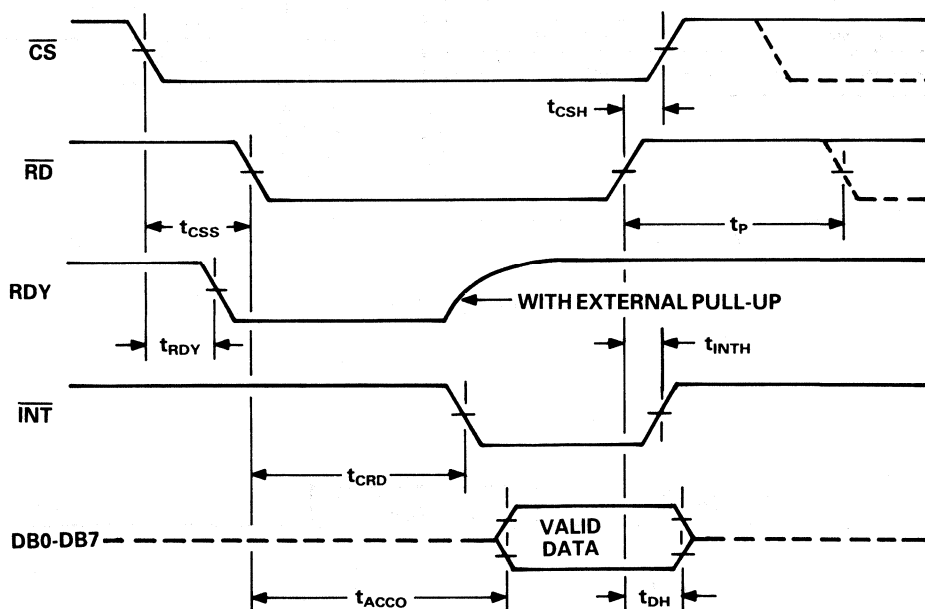
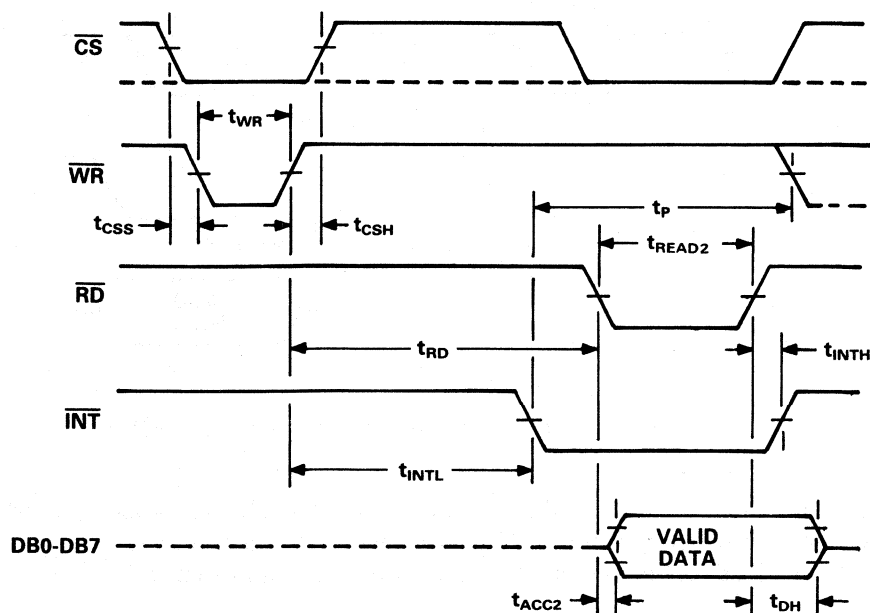


Figure 3. RD Mode

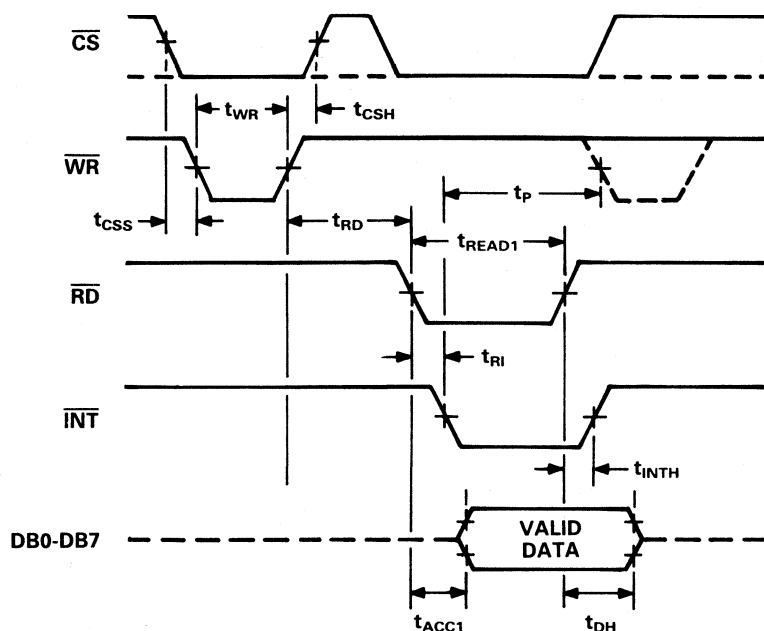
6.2 WR-RD Mode (MODE = 1).

In the WR-RD mode, Pin 6 is configured as a WRITE ($\overline{WR}$) input for the AD7821. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 4). $\overline{INT}$ typically goes low within 380 ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

Figure 4. WR-RD Mode ($t_{RD} > t_{INTL}$)

The alternative option can be used to shorten the conversion time. This is a method for bypassing the internal time-out circuit. The $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 250 ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data output (DB0-DB7). $\overline{INT}$ is driven low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 5.

Figure 5. WR-RD Mode ($t_{RD} < t_{INTL}$)

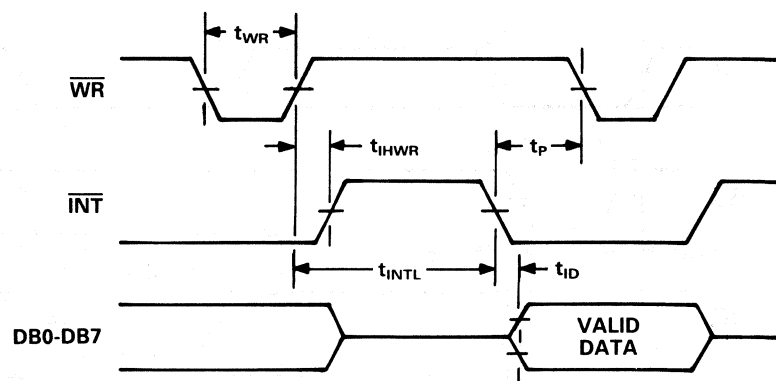


Figure 6. WR-RD Stand-Alone Operation, $\overline{CS} = \overline{RD} = 0$

The AD7821 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low, and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid 530 ns ($t_{INTL} + t_{ID}$) after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.



LC²MOS High Speed 4- and 8-Channel 8-Bit ADCs

AD7824/AD7828

1.1 Scope.

This specification covers the detail requirements of 4- and 8-channel high speed 8-bit A/D converters. The AD7824 provides 4 multiplexed analog inputs, while the AD7828 provides 8. A half-flash conversion technique gives a conversion rate of 2.5μs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of up to 10kHz on all channels.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number ¹
– 1	AD7824TQ/883B and AD7828T(X)883B
– 2	AD7824UQ/883B and AD7828U(X)883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-24 for AD7824

(X)	Package	Description
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V _{DD}	0V, +7V
Digital Input Voltage to GND ($\overline{RD}$, $\overline{CS}$, A0, A1 & A2)	–0.3V, V _{DD}
Digital Output Voltage to GND (DB0, DB7, RDY & $\overline{INT}$)	–0.3V, V _{DD}
V _{REF} (+) to GND	V _{REF} (–), V _{DD}
V _{REF} (–) to GND	0V, V _{REF} (+)
Analog Input (Any Channel)	–0.3V, V _{DD}
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24, Q-28 and E-28A
 θ_{JA} = 120°C/W for Q-24, Q-28 and E-28A

AD7824/AD7828 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	–1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error ²	TUE	–1 –2	1 1/2	1 1	1 1/2	1/2		± LSB max
Analog Input Voltage Range	V_{IN}	–1, 2	$V_{REF}(-)$ $V_{REF}(+)$					V min V max
Analog Input Leakage Current	I_{IN}	–1, 2	3	3	3		(Any Channel)	± μA max
Analog Input Capacitance		–1, 2	45				0V to +5V	pF typ
Reference Input Resistance	R_{IN}	–1, 2	1 4	1 4	1 4			k Ω min k Ω max
Digital Input High Level	V_{IH}	–1, 2	2.4	2.4	2.4		A0, A1 & A2, $\overline{RD}$, $\overline{CS}$	V min
Digital Input Low Level	V_{IL}	–1, 2	0.8	0.8	0.8		A0, A1 & A2, $\overline{RD}$, $\overline{CS}$	V max
Digital Input High Current	I_{IN}	–1, 2	1.0	1.0	1.0		$\overline{CS}$, $\overline{RD}$, A0, A1 & A2	μA max
Digital Input Low Current	I_{IL}	–1, 2	–1.0	–1.0	–1.0		$\overline{CS}$, $\overline{RD}$, A0, A1 & A2	μA max
Digital Input Capacitance	C_{IN}	–1, 2	8.0				$\overline{CS}$, $\overline{RD}$, A0, A1 & A2	pF max
Digital Output High Level	V_{OH}	–1, 2	4.0	4.0	4.0		DB0–DB7, $\overline{INT}$ $I_{SOURCE} = 360\mu A$	V min
Digital Output Low Level	V_{OL}	–1, 2	0.4	0.4	0.4		DB0–DB7, $\overline{INT}$ $I_{SINK} = 1.6mA$	V max
Digital Output Low Level ³	V_{OL}	–1, 2	0.4	0.4	0.4		RDY; $I_{SINK} = 2.6mA$	V max
Floating State Leakage Current	I_{OUT}	–1, 2	3.0	3.0	3.0		DB0–DB7	μA max
Digital Output Capacitance	C_{OUT}	–1, 2	8.0					pF max
Slew Rate, Tracking		–1, 2	0.157					V/ μs max
Supply Current from V_{DD}	I_{DD}	–1, 2	16.0	20.0	20.0		$\overline{CS} = \overline{RD} = 2.4V$	mA max
Power Supply Sensitivity		–1, 2	1/4	1/4	1/4		$V_{DD} = 5V \pm 5\%$	± LSB max
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}	–1, 2	0					ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CSH}	–1, 2	0					ns min
$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5k Ω ⁴	t_{RDY}	–1, 2	60				40ns max at +25°C	ns max
Conversion Time, Mode 0	t_{CRD}	–1, 2	2.8	2.0	2.8		2.0 μs max at +25°C	μs max
Data Access Time after $\overline{RD}$ ⁵	t_{ACCI}	–1, 2	120				85ns max at +25°C	ns max
$\overline{RD}$ to INT Delay ⁴	t_{INTH}	–1, 2	100				75ns max at +25°C	ns max
Data Hold Time ⁶	t_{DH}	–1, 2	70				60ns max at +25°C	ns max
Delay Time Between Conversions	t_P	–1, 2	600				500ns min at +25°C	ns min
Read Pulse Width, Mode 1	t_{RD}	–1, 2	80 400					ns min ns max
Data Access Time After INT, Mode 0 ⁵	t_{ACC2}	–1, 2	70				50ns max at +25°C	ns max
Multiplexer Address Setup Time	t_{AS}	–1, 2	0					ns min
Multiplexer Address Hold Time	t_{AH}	–1, 2	40					ns min

NOTES

¹ $V_{DD} = +5V$; $V_{REF}(+) = +5V$; $V_{REF}(-) = GND = 0V$ unless otherwise specified. Specifications apply for Mode 0.

All input control signals are specified with $t_r = t_f = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

²Total unadjusted error includes offset, full scale and linearity errors.

³RDY in an open drain output.

⁴ $C_L = 50pF$.

⁵Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

⁶Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Table 1.

REV. A

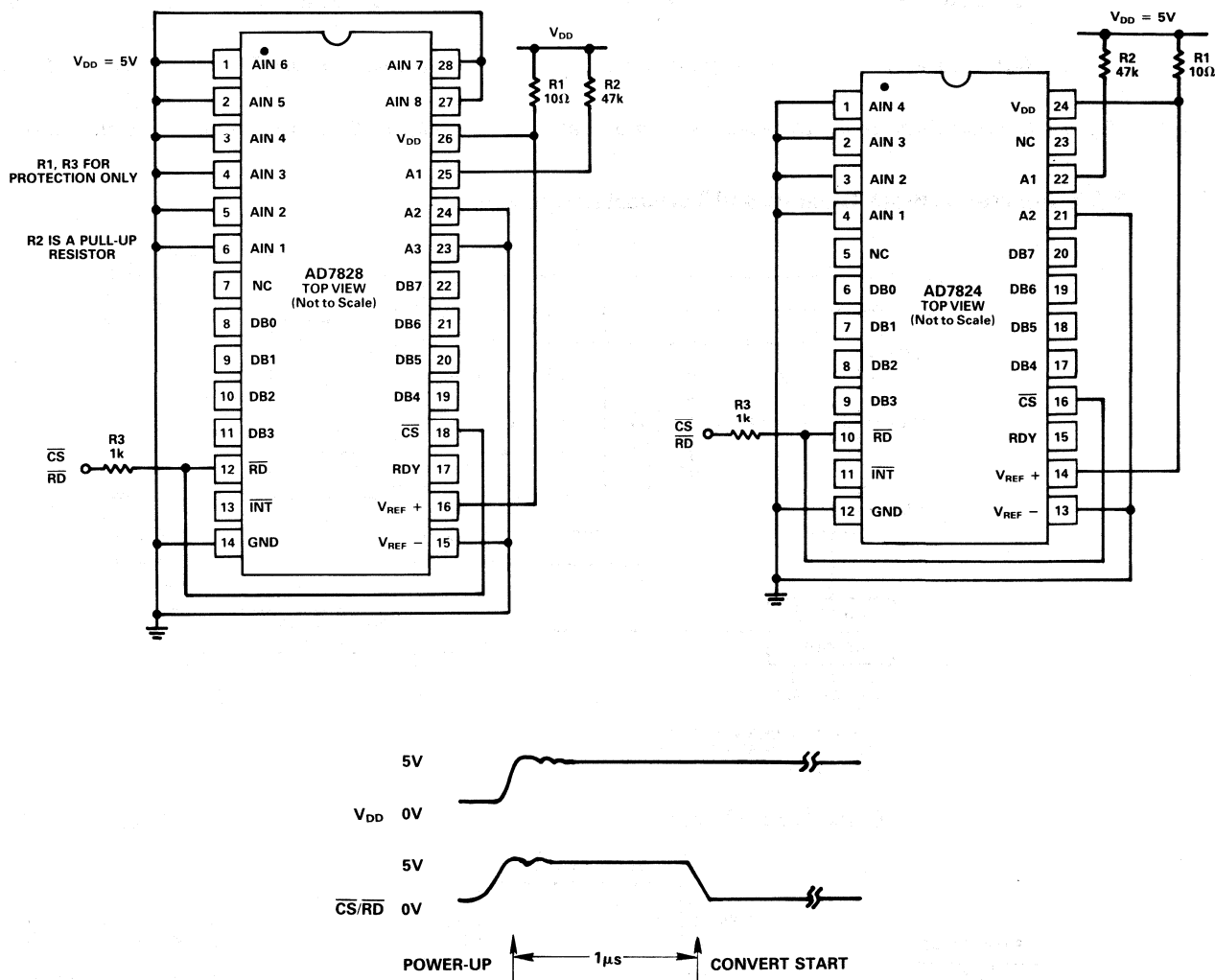
AD7824/AD7828

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7824/AD7828 Burn-In Philosophy

After power-up the device performs a conversion on $\overline{CS}/RD$ going low. AIN 1 and AIN 4 are tied to ground so the device will output the all zeros code, thus putting the output drive N-channels under maximum stress for the period of burn-in.

The pull-up resistor on the A1 pin will stress this input inverter during burn-in to show up drifts in input logic threshold. Address input A2 is tied to ground causing the initial conversion to occur on channel 2. $\overline{CS}$ and $\overline{RD}$, require 0V to maintain all zeros on the 3-state outputs.

Apart from the conversion on power-up the device is burned-in the static mode taking a maximum I_{DD} of 15mA from the 5V supply.

5.0 Timing and Control.

The AD7824/AD7828 have two digital inputs for timing and control. These are Chip Select ($\overline{CS}$) and Read ($\overline{RD}$). A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion and latches the multiplexer address inputs (see Table 2). There are two modes of operation as outlined by the timing diagrams of Figures 3 and 4. Mode 0 is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when conversion is complete. Mode 1 does not require microprocessor WAIT states. A READ operation initiates a conversion and reads the previous conversion results.

AD7824		AD7828			CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

Table 2. Truth Table for Input Channel Selection

5.1 Mode 0.

Figure 3 shows the timing diagram for Mode 0 operation. This mode can only be used for microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which latches the analog multiplexer address inputs and starts a conversion. The data bus (DB7-DB0) remains in the three-state condition until conversion is complete. There are two converter status outputs on the AD7824/AD7828, interrupt ($\overline{INT}$) and ready (RDY) which can be used to drive the microprocessor READY/WAIT input. The RDY is an open drain output (no internal pull-up device) which goes low on the falling edge of $\overline{CS}$ and $\overline{RD}$ and goes high impedance at the end of conversion, when the 8-bit conversion result appears on the data outputs. If the RDY output status is not required, then the external pull-up resistor can be omitted. The $\overline{INT}$ input goes low when conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

5.2 Mode 1.

Mode 1 operation is designed for applications where the microprocessor is not forced into a WAIT state. A READ operation takes $\overline{CS}$ and $\overline{RD}$ low, which latches the multiplexer address inputs and triggers a conversion (see Figure 4). Data from the previous conversion is read from the three-state data outputs (DB7-DB0). This data may be disregarded if not required. The RDY output (open drain output) is low for the duration of the READ operation and goes high impedance on the rising edge of $\overline{CS}$ or $\overline{RD}$. If the RDY output status is not required, then the external pull-up resistor can be omitted. At the end of conversion $\overline{INT}$ goes low. A second READ operation is required to access the new conversion result. This READ operation latches a new address into the multiplexer inputs and starts another conversion. $\overline{INT}$ returns high at the end of the second READ operation, when $\overline{CS}$ and $\overline{RD}$ returns high. A delay of 2.5 μ s must be allowed between READ operations.

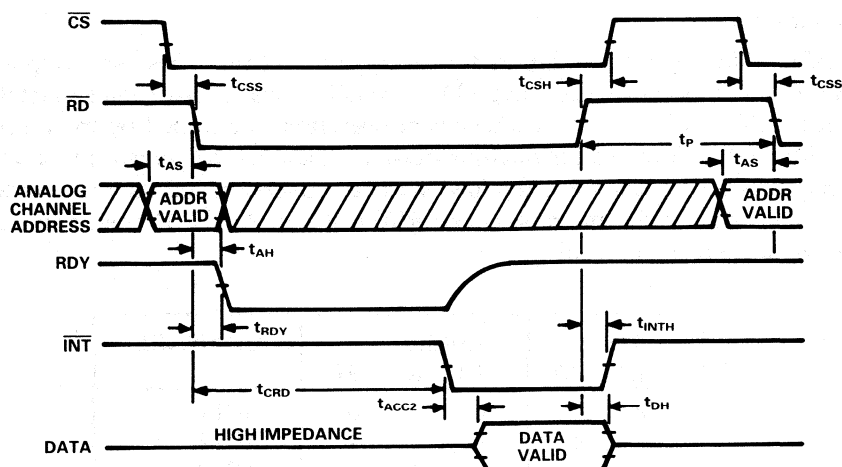


Figure 3. Mode 0 Timing Diagram

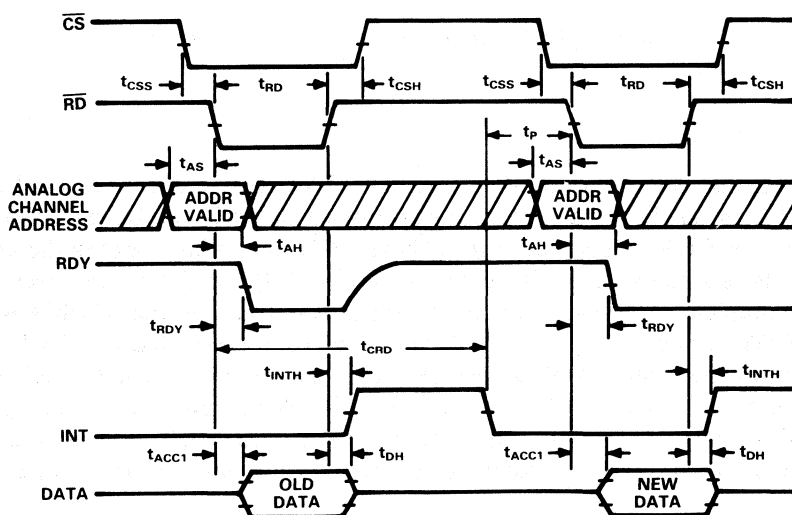


Figure 4. Mode 1 Timing Diagram

1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 14-bit D/A converter, with output amplifier and operating off 5 V supplies. It has a fast parallel and serial microprocessor interface structure.

1.2 Part Number.

The complete part number is:

Device	Part Number ¹
-1	AD7840S(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3"
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to AGND	 -0.3 V to +7 V
V_{SS} to AGND	 +0.3 V to -7 V
AGND to DGND	 -0.3 V to $V_{DD} + 0.3$ V
V_{OUT} to AGND	 V_{SS} to V_{DD}
REF OUT to AGND	 0 V to V_{DD}
Digital Inputs to DGND	 -0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$
Storage Temperature Range	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	 $+300^\circ\text{C}$
Power Dissipation (Any Package)	
Up to $+75^\circ\text{C}$	 450 mW
Derates above $+75^\circ\text{C}$	 100 mW/ $^\circ\text{C}$

1.4 Recommended Operating Conditions.

Supply Voltage: $V_{DD} = +5\text{ V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, AGND = DGND = 0 V.
Reference: REF IN = +3 V, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$.

1.1 Scope.

This specification covers the detail requirements for a monolithic voltage output 12-bit multiplying digital-to-analog converter with a parallel loading structure.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7845S(X)/883B
-2	AD7845T(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3" Width
E	E-28	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	 -0.3 V, +17 V
V_{SS} to DGND	 +0.3 V, -17 V
V_{REF} to AGND	 ± 25 V
V_{RFB} to AGND	 ± 25 V
V_{RA} to AGND	 ± 25 V
V_{RB} to AGND	 ± 25 V
V_{RC} to AGND	 ± 25 V
V_{OUT} to AGND ¹	 $V_{DD} + 0.3$, $V_{SS} - 0.3$ V
AGND to DGND	 -0.3 V, V_{DD}
Digital Input Voltage to DGND	 -0.3 V to $V_{DD} + 0.3$ V
Power Dissipation (Any Package)	
Up to $+75^\circ\text{C}$	 650 mW
Derates above $+75^\circ\text{C}$	 10 mW/ $^\circ\text{C}$
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$

NOTE

¹ V_{OUT} may be shorted to AGND provided that the power dissipation of the package is not exceeded.

1.3.1 Recommended Operating Conditions.

$V_{DD} = +15$ V $\pm 5\%$, $V_{SS} = -15$ V $\pm 5\%$, $V_{REF} = +10$ V, AGND = DGND = 0 V, V_{OUT} connected to R_{FB} , V_{OUT} load = 2 k Ω , and 100 pF.

AD7845 – SPECIFICATIONS

Test	Symbol	Device	Limits Min Max		Sub Group	Test Condition ¹	Units
Resolution	RES	–1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	–1, 2	–1	+1	1	1 LSB = $V_{REF} = 2.4$ mV	LSB
		–1	–2	+2	2, 3		
		–2	–1	+1	2, 3		
		–2	–0.5	+0.5	4		
Differential Nonlinearity	DNL	–1, 2	–1	+1	1, 2, 3	All Devices Type Are Guaranteed Monotonic over Temperature	LSB
Zero Code Offset Error	Z_E	–1, 2	–2	+2	1		mV
		–1	–5	+5	2, 3		
		–2	–4	+4	2, 3		
		–2	–1	+1	4		
Gain Error	A_E	–1	–6	+6	1, 2, 3	R_{FB} , V_{OUT} Connected	LSB
		–2	–3	+3	1, 2, 3		
		–1	–9	+9	1, 2, 3	R_C , V_{OUT} Connected	
		–2	–6	+6	1, 2, 3	$V_{REF} = +5$ V	
		–1	–9	+9	1, 2, 3	R_B , V_{OUT} Connected	
		–2	–6	+6	1, 2, 3	$V_{REF} = +5$ V	
		–1	–10	+10	1, 2, 3	R_A , V_{OUT} Connected	
		–2	–8	+8	1, 2, 3	$V_{REF} = 2.5$ V	
Reference Input Resistance	R_{REFIN}	–1, 2	8	16	1, 2, 3		k Ω
Application Resistor Matching	$R_{MATCH RATIO}$	–1, 2		0.5	1, 2, 3	Matching Between R_A , R_B , R_C	%
Digital Input High Voltage	V_{INH}	–1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V_{INL}	–1, 2		0.8	1, 2, 3		V
Digital Input Current	I_{IN}	–1, 2	–1	+1	1, 2, 3	Digital Inputs at 0 V and V_{DD}	μ A
Digital Input Capacitance	C_{IN}	–1, 2		7	13 ³ , 14 ³ , 15 ³		pF
Power Supply Current	I_{DD}	–1, 2		10	1, 2, 3	V_{OUT} Unloaded	mA
	I_{SS}	–1, 2		4	1, 2, 3		
Power Supply Rejection Gain/ ΔV_{DD}	$A/\Delta V_{DD}$	–1, 2	–0.2	+0.2	1, 2, 3	$V_{DD} = 15$ V $\pm 5\%$, $V_{REF} = -10$ V	%/%
Gain/ ΔV_{SS}	$A/\Delta V_{SS}$	–1, 2	–0.2	+0.2	1, 2, 3	$V_{SS} = -15$ V $\pm 5\%$	%/%
Output Voltage Settling Time	t_{SL}	–1, 2		5	13, 14, 15	To 0.01% of FSR	μ s
Open Loop Gain ²		–1, 2	85		13, 14, 15		dB
Output Voltage Swing		–1, 2	–10	+10	13, 14, 15	$R_L = 2$ k Ω , $C_L = 100$ pF	V
Chip Select to Write Setup Time	t_{CS}	–1, 2	100		9	See Timing Diagram	ns
			140		10 ³ , 11 ³		
Chip Select to Write Hold Time	t_{CH}	–1, 2	0		9, 10, 11		ns
Write Pulse Width	t_{WR}	–1, 2	100		9		ns
			140		10, 11		
Data Setup Time	t_{DS}	–1, 2	100		9		ns
			120		10, 11		
Data Hold Time	t_{DH}	–1, 2	20		9, 10, 11		ns

NOTES

¹–55°C to +125°C.

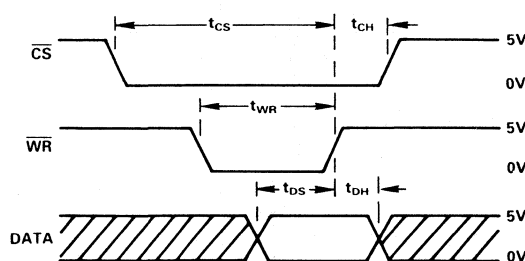
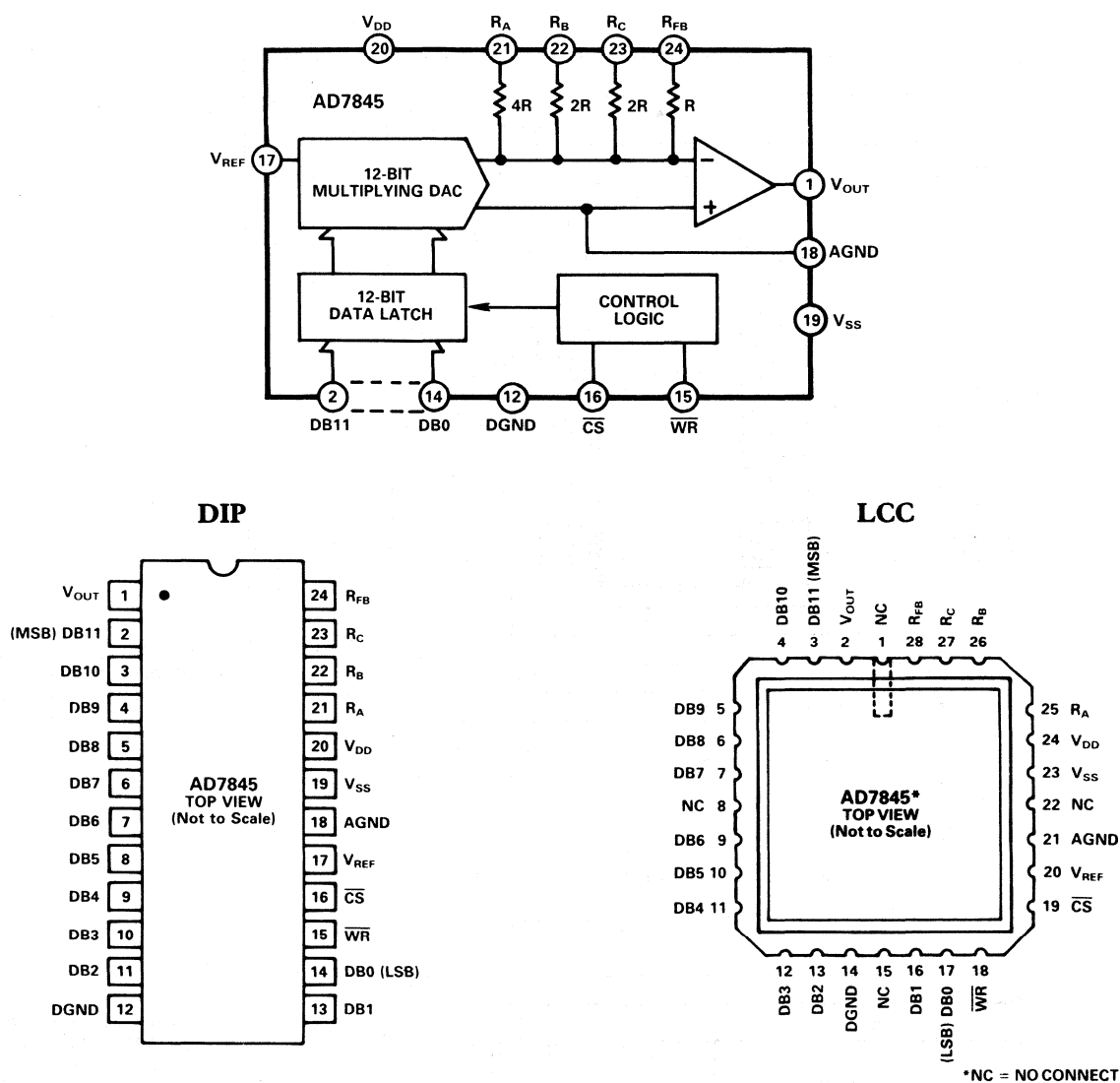
² V_{OUT} , R_{RB} not connect. $V_{OUT} = \pm 10$ V, $R_L = 2$ k Ω . Parameters in subgroups 13, 14, 15 are characterized at initial design and after any subsequent redesigns.

³Subgroups 10, 11, 13, 14, 15 are characterized at initial design and after subsequent design changes and are not production tested.

Table 1.

REV. A

3.2.1 Functional Block Diagram and Terminal Assignments.



- NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_R = t_F = 20\text{ns}$.
 2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Timing Diagram

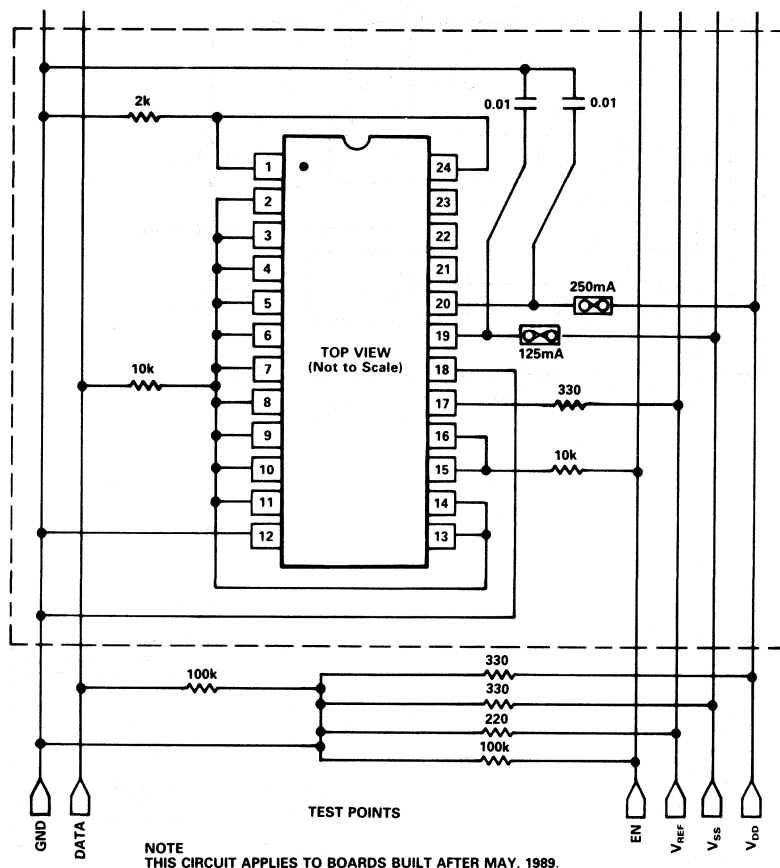
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

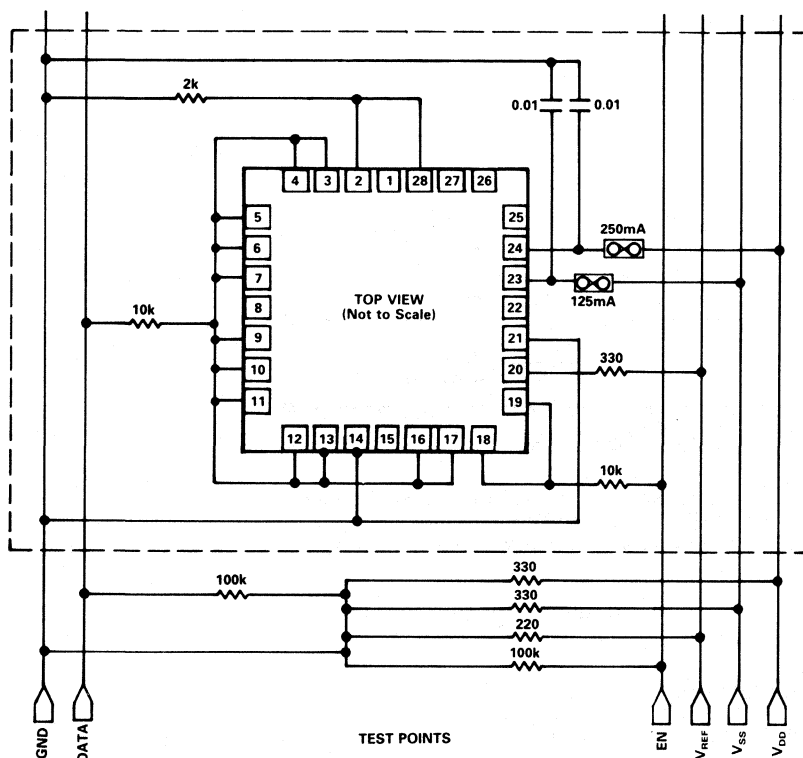
AD7845

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7845 Edge Connections



AD7845 Edge Connections

STATIC BURN-IN CONDITIONS APPLY VOLTAGES IN THE FOLLOWING SEQUENCE:

1. V_{SS} -15V (V2)
2. V_{DD} +15V (V5)
3. V_{REF} -10 V (V4)
4. ENABLE GND (V1)
5. DATA +15 V

DYNAMIC BURN-IN CONDITIONS APPLY VOLTAGES IN THE FOLLOWING SEQUENCE:

1. V_{SS} -15V (V2)
2. V_{DD} +15V (V5)
3. V_{REF} -10 V (V4)
4. ENABLE GND (V1)
5. DATA 0 To +15 V @ 1kHz, CONTINUOUS

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16-bit, voltage output, multiplying DAC, with a readback facility.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD7846S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

D	D-28	28-Pin Side-Brazed Ceramic
E	E-28A	28-Terminal Leadless Ceramic Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	-0.3 V to +17 V
V_{CC} to DGND	-0.3 V to +7 V
V_{SS} to DGND	+3 V to -17 V
V_{REF+} to DGND	± 25 V
V_{REF-} to DGND	± 25 V
V_{OUT} to DGND ¹	± 25 V
R_{IN} to DGND	± 25 V
Digital Input Voltage to DGND	-0.3 V to V_{CC} to +0.3 V
Digital Output Voltage to DGND	-0.3 V to V_{CC} to +0.3 V
Power Dissipation (Any Package)	
to +75°C	1000 mW
Derates Above +75°C	10 mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTE

¹ V_{OUT} may be shorted to DGND, V_{DD} , V_{SS} , V_{CC} provided that the power dissipation of the package is not exceeded.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for D-28 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for D-28 and E-28A

AD7846 – SPECIFICATIONS

Test	Symbol	Device	Design Limits $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 7, 8	Sub Group 9	Sub Group 10, 11	Sub Group 13, 14, 15	Test Condition ¹	Units
Relative Accuracy	R_A	1, 2	16	16	16					Unipolar Output ²	±LSB
Differential Nonlinearity ³	DNL	1, 2	1	1	1						±LSB
Gain Error ⁴	A_E	1, 2	16	16	24						±LSB
Offset Error	O_E	1, 2	16	16	24						±LSB
Relative Accuracy	R_A	1, 2	8	8	8					Bipolar Output ⁵	±LSB
Differential Nonlinearity ³	DNL	1, 2	1	1	1						±LSB
Gain Error ⁴	A_E	1, 2	8	16	16						±LSB
Offset Error	O_E	1, 2	8	16	16						±LSB
Bipolar Zero Error	BIP_E	1, 2	8	16	16						±LSB
Reference Input Resistance	V_{REFIN}	1, 2	20/40	20/40	20/40					Resistance from V_{REF-} to V_{REF+}	kΩ min/ max
V_{REF+} Range	V_{REF+}	1, 2	6						6		±V
V_{REF-} Range	V_{REF-}	1, 2	6						6		±V
Output Voltage Swing	V_{SWING}	1, 2	+4						+4	$V_{SS} + 4.0$	V
			-3						-3	$V_{DD} - 3.0$	
Input Voltage High Level	V_{IH}	1, 2	2.4	2.4	2.4						V
Input Voltage Low Level	V_{IL}	1, 2	0.8	0.8	0.8						V
Logical Input Current	I_{IN}	1, 2	10	10	10						±μA
Logical Input Capacitance	C_{IN}	1, 2	10						10		pF max
Output Voltage High Level	V_{OH}	1, 2	4.0	4.0	4.0					$I_{SOURCE} = 400 \mu A$	V min
Output Voltage Low Level	V_{OL}	1, 2	0.4	0.4	0.4					$I_{SINK} = 1.6 mA$	V max
Floating State Leakage Current		1, 2	10	10	10					DB0-DB15 = 0 to V_{CC}	±μA
Floating State Output Capacitance		1, 2	10						10		pF max
Positive Power Supply Current	I_{DD}	1, 2	5	5	5					V_{OUT} Unloaded ⁶	mA max
Negative Power Supply Current	I_{SS}	1, 2	5	5	5						mA max
Positive Logic Supply Current	I_{CC}	1, 2	1	1	1						mA max
Power Supply Sensitivity ⁷	PSS	1, 2	2	2	2						LSB/V
Functional Test R/W to $\overline{CS}$ Setup Time	t_1	1, 2	50				40	50		See Figure 2 ⁸	ns
$\overline{CS}$ Pulse Width (Write Cycle)	t_2	1, 2	140				150	190			ns
R/W to $\overline{CS}$ Hold Time	t_3	1, 2	50				40	50			ns
Data Setup Time	t_4	1, 2	120				110	120			ns
Data Hold Time	t_5	1, 2	0				0	0			ns
Data Access Time ⁹	t_6	1, 2	320				230	320			ns
Bus Relinquish ¹⁰	t_7	1, 2	90				80	90			ns
$\overline{CLR}$ Setup Time	t_8	1, 2	20				20	20		See Figure 2	ns
$\overline{CLR}$ Pulse Width	t_9	1, 2	150				150	150			ns
$\overline{CLR}$ Hold Time	t_{10}	1, 2	0				0	0			ns
$\overline{LDAC}$ Pulse Width	t_{11}	1, 2	100				80	100			ns
$\overline{CS}$ Pulse Width (Read Cycle)	t_{12}	1, 2	330				240	330			ns

Table 1. (Continued on next page)

Terminal Connections

Device Type Case Outline Terminal Number	01 X Terminal Symbol	Device Type Case Outline Terminal Number	01 X Terminal Symbol
1	DB2	15	DB10
2	DB1	16	DB9
3	DB0	17	DB8
4	V_{DD}	18	DB7
5	V_{OUT}	19	DB6
6	R_{IN}	20	DGND
7	V_{REF+}	21	V_{CC}
8	V_{REF-}	22	$\overline{R/W}$
9	V_{SS}	23	$\overline{CS}$
10	DB15	24	$\overline{CLR}$
11	DB14	25	$\overline{LDAC}$
12	DB13	26	DB5
13	DB12	27	DB4
14	DB11	28	DB3

Pin Descriptions

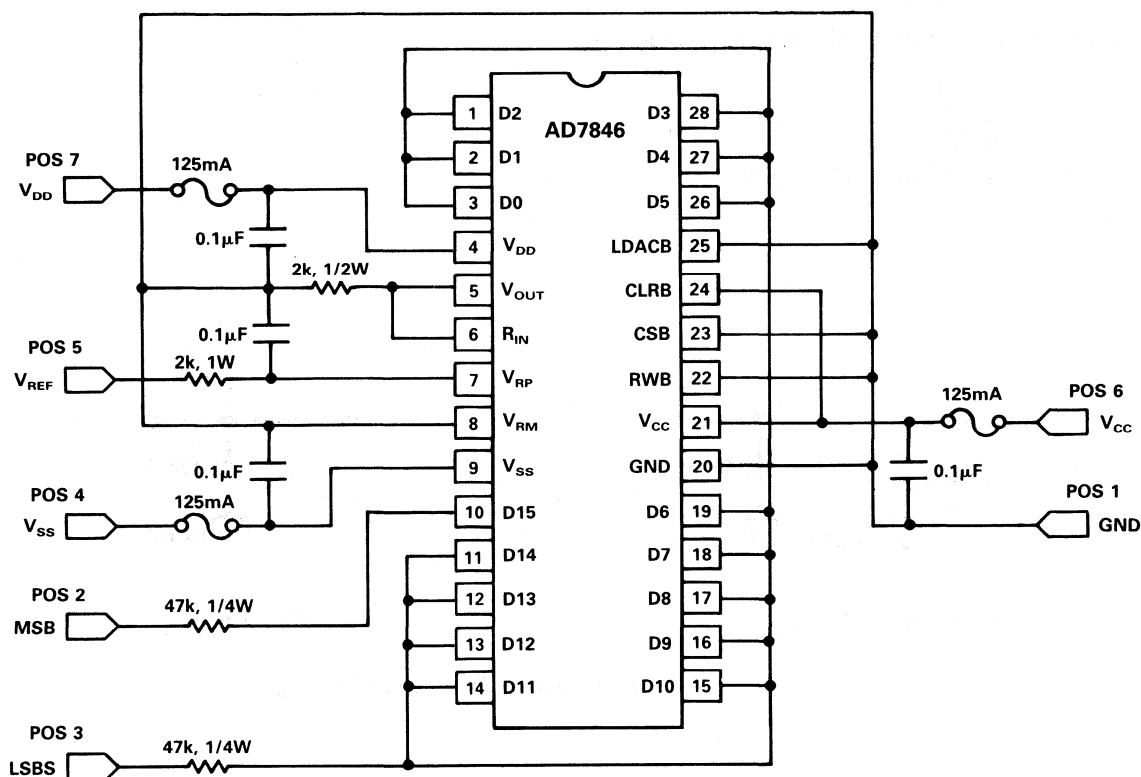
Pin	Description
DB2–DB0	Data I/O pins. DB0 is LSB.
V_{DD}	Positive supply for analog circuitry. This is a +15 V nominal.
V_{OUT}	DAC output voltage pin.
R_{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See Tables 2 and 3.
V_{REF+}	V_{REF+} input. The DAC is specified for $V_{REF+} = 5.0$ V.
V_{REF-}	V_{REF-} input. For unipolar operation connect it to -5.0 V. The device is specified for both conditions.
V_{SS}	Negative supply for analog circuitry. This is -15 V nominal.
DB15–DB6	Data I/O pins. DB15 is MSB.
DGND	Ground pin for logic circuitry.
V_{CC}	Positive supply for logic circuitry. This is +5.0 V nominal.
$\overline{R/W}$	$\overline{R/W}$ input. This can be used to load data to the DAC or read back the DAC latch contents.
$\overline{CS}$	Chip select input. This selects the device.
$\overline{CLR}$	Clear input. The DAC can be cleared to 000 . . . 000 or 100 . . . 000. See Tables 2 and 3.
$\overline{LDAC}$	Asynchronous load input to DAC.
DB5–DB3	Data I/O pins.

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

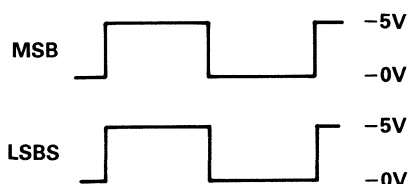
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



- Each AD7846 socket has associated with it the four resistors shown, four 0.1 μ F ceramic type capacitors and three 125 mA pico fuses.
- Each burn-in board has the following seven external signals supplied:

Signal	Voltage
V_{DD}	+15 V
V_{REF}	+0 V
V_{CC}	+5 V
GND	0 V
V_{SS}	-15 V
MSB	See Below
LSBs	See Below

- For static burn-in MSB and LSBs are both tied to +5 V.
- For dynamic burn-in MSB and LSBs are driven with 20 kHz square waves as shown:

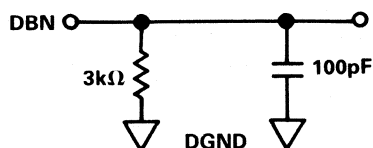


5. For static burn-in and power-up sequences is

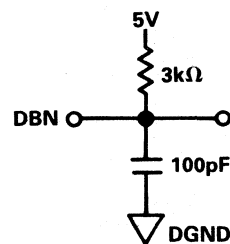
1. V_{DD}
2. V_{SS}
3. V_{CC} , MSB, LSBs (together)
4. V_{REF}

6. For dynamic burn-in the power sequence is

1. V_{DD}
2. V_{SS}
3. V_{CC}
4. MSB, LSBs (together)
5. V_{REF}

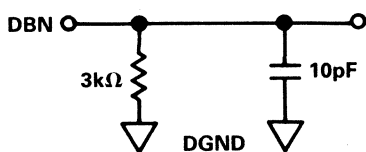


High-Z to V_{OH}

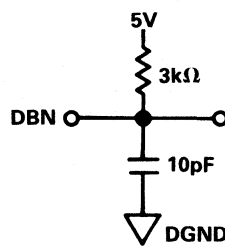


High-Z to V_{OL}

Figure 1a. Load Circuits for Access Time (t_6)



V_{OH} to High-Z



V_{OL} to High-Z

Figure 1b. Load Circuits for Bus Relinquish Time (t_7)

Figure 1. Load Circuits

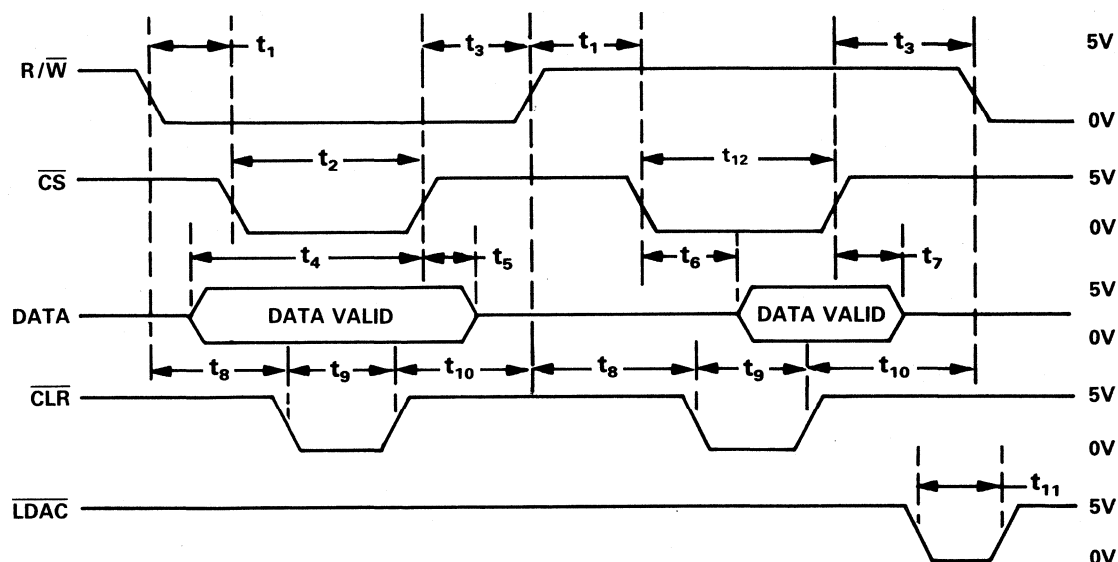


Figure 2. Switching Characteristics

$\overline{CS}$	$\overline{R/W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-State DAC I/O Latch in High Z-State
0	0	X	X	DAC I/O Latch Loaded with DB15–DB0
0	1	X	X	Contents of DAC I/O Latch Available on DB15–DB0
X	X	0	1	Contents of DAC I/O Latch Transferred to DAC Latch
X	0	X	0	DAC Latch Loaded with 000 . . . 000
X	1	X	0	DAC Latch Loaded with 100 . . . 000

0 = Low
1 = High
X = Don't Care

Table 2. Truth Table

Output Range	V_{REF+}	V_{REF-}	R_{IN}
0 V to +5 V	+5 V	0 V	V_{OUT}
0 V to +10 V	+5 V	0 V	0 V
+5 V to –5 V	+5 V	–5 V	V_{OUT}
+5 V to –5 V	+5 V	0 V	+5 V
+10 V to –10 V	+5 V	–5 V	0 V

Table 3. Output Voltage Ranges

1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 12-bit sampling analog-to-digital converter. It features 100 KSPS throughput, on board buried Zener reference and specified dynamic parameters.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7870S(X)/883B
-2	AD7870T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V_{DD} to AGND	-0.3 V, +7 V
V_{SS} to AGND	+0.3 V, -7 V
AGND to DGND	-0.3 V, $V_{DD} + 0.3$ V
V_{IN} to AGND	-15 V, +15 V
REF OUT to AGND	0 V, V_{DD}
Digital Inputs to DGND	-0.3 V, $V_{DD} + 0.3$ V
Digital Outputs to DGND	-0.3 V, $V_{DD} + 0.3$ V
Power Dissipation (to $+75^\circ\text{C}$)	450 mW
Derates above $+75^\circ\text{C}$	6 mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-24 and E-28A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-24 and E-28A

AD7870 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ /Comments	Units
Resolution	RES	-1, 2	12				Resolution for Which No Missing Codes Are Guaranteed	Bits
Signal to Noise ² Ratio	SNR	-1, 2	70	70	70		$V_{IN} = 10$ kHz Sine Wave $f_{SAMPLE} = 100$ kHz	dB min
Total Harmonic Distortion	THD	-1, 2	-80	-80	-80		$V_{IN} = 10$ kHz Sine Wave $f_{SAMPLE} = 100$ kHz	dB max
Peak Harmonic or Spurious Noise		-1, 2	-80	-80	-80		$V_{IN} = 10$ kHz Sine Wave $f_{SAMPLE} = 100$ kHz	dB max
Intermodulation Distortion (2nd Order Terms)	IMD ²	-1, 2	-80	-80	-80		$f_a = 9$ kHz; $f_b = 9.5$ kHz; $f_{SAMPLE} = 50$ kHz	dB max
Intermodulation Distortion (3rd Order Terms)	IMD ³	-1, 2	-80	-80	-80		$f_a = 9$ kHz; $f_b = 9.5$ kHz; $f_{SAMPLE} = 50$ kHz	dB max
Track/Hold Acquisition Time	t_{ACQ}	-1, 2	2					μs max
Integral Nonlinearity	INL	-2	1	1	1			$\pm$ LSB max
Differential Nonlinearity	DNL	-2	1	1	1			$\pm$ LSB max
Bipolar Zero Error		-1, 2	5	5	5			$\pm$ LSB max
Positive Full Scale Error ³		-1, 2	5	5	5			$\pm$ LSB max
Negative Full Scale Error ³		-1, 2	5	5	5			$\pm$ LSB max
Analog Input Current		-1, 2	500	500	500			$\pm \mu A$ max
Analog Input Voltage Range		-1, 2	± 3					V
Reference Voltage	V_{REF}	-1, 2	2.99				$T_{AMB} = +25^{\circ}C$	V min
			3.01					V max
Reference Tempco		-1	60		60			$\pm ppm/^{\circ}C$ max
		-2	35		35			
Reference Load Sensitivity		-1, 2	1	1	1		Reference Load Should Not Be Changed During Conversion.	$\pm mV$ max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Current	I_{IN}	-1, 2	10	10	10			$\pm \mu A$ max
Input Capacitance	C_{IN}	-1, 2	10					pF max
Digital Output High Voltage	V_{OH}	-1, 2	4.0	4.0	4.0		$I_{SOURCE} = 40 \mu A$	V min
Digital Output Low Voltage	V_{OL}	-1, 2	0.4	0.4	0.4		$I_{SINK} = 1.6$ mA	V max
Floating State Leakage Current	I_{OUT}	-1, 2	10	10	10			$\pm \mu A$ max
Floating State Output Capacitance	C_{OUT}	-1, 2	1.5					pF max
Conversion Time (External Clock)	t_{CONV}	-1, 2	7.0				$f_{CLK} = 2.5$ MHz	μs min
			8					μs max
Conversion Time (Internal Clock)	t_{CONV}	-1, 2	7					μs min
			9					μs max
Supply Current from V_{DD}	I_{DD}	-1, 2	13	13	13			mA max
Supply Current from V_{SS}	I_{SS}	-1, 2	6	6	6			mA max

NOTES

¹ $V_{DD} = +5$ V $\pm 5\%$, $V_{SS} = -5$ V $\pm 5\%$, AGND = DGND = 0 V, $f_{CLK} = 2.5$ MHz external unless otherwise stated.

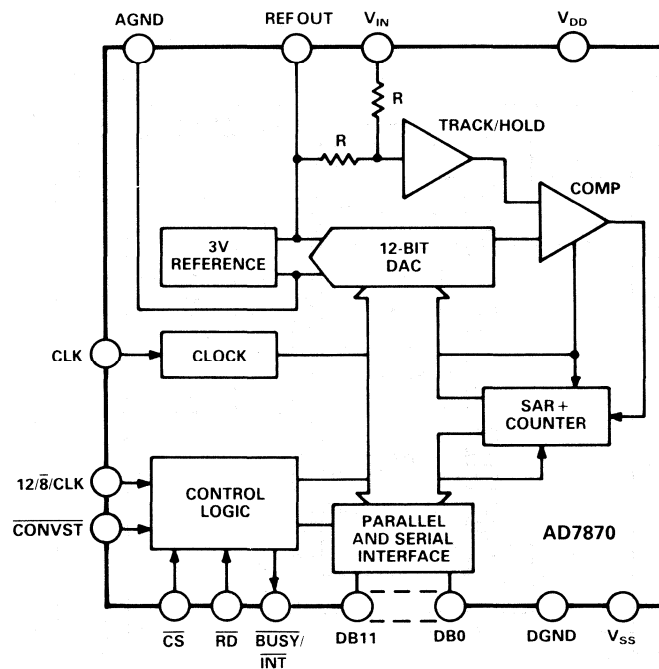
²SNR calculation includes distortion and noise components.

³Measured with respect to internal reference and includes bipolar offset error.

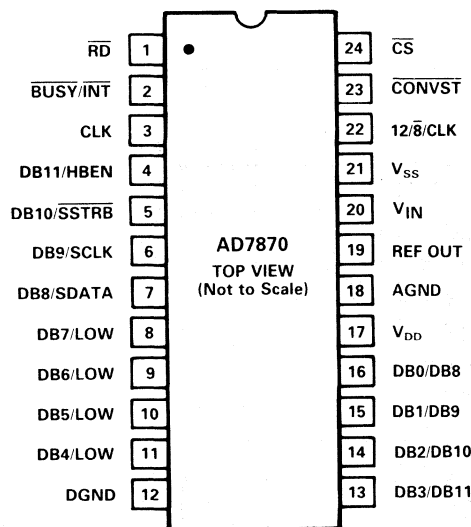
Table 1.

REV. A

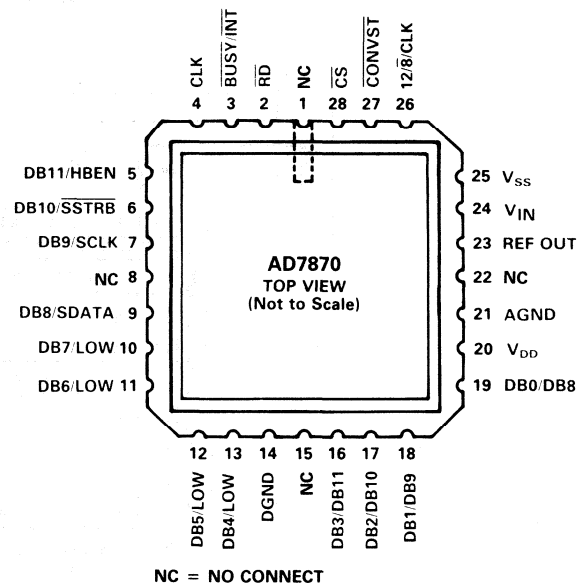
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)



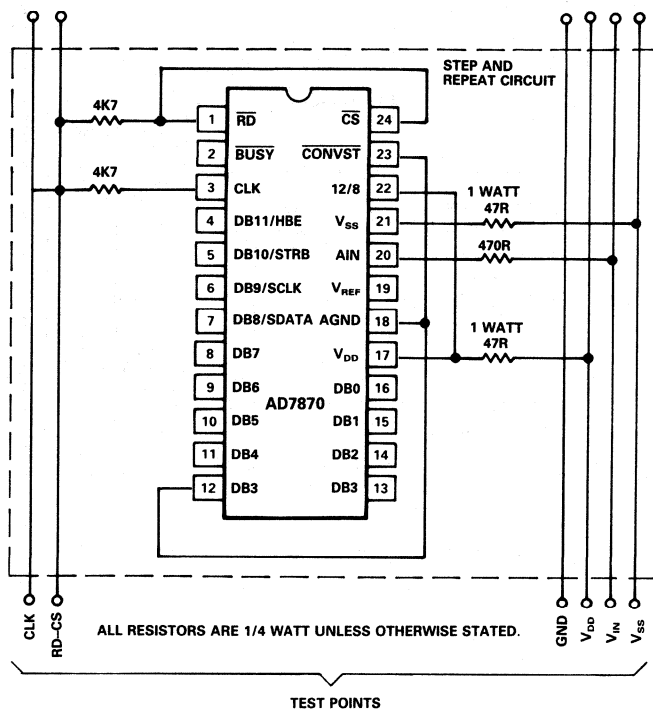
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

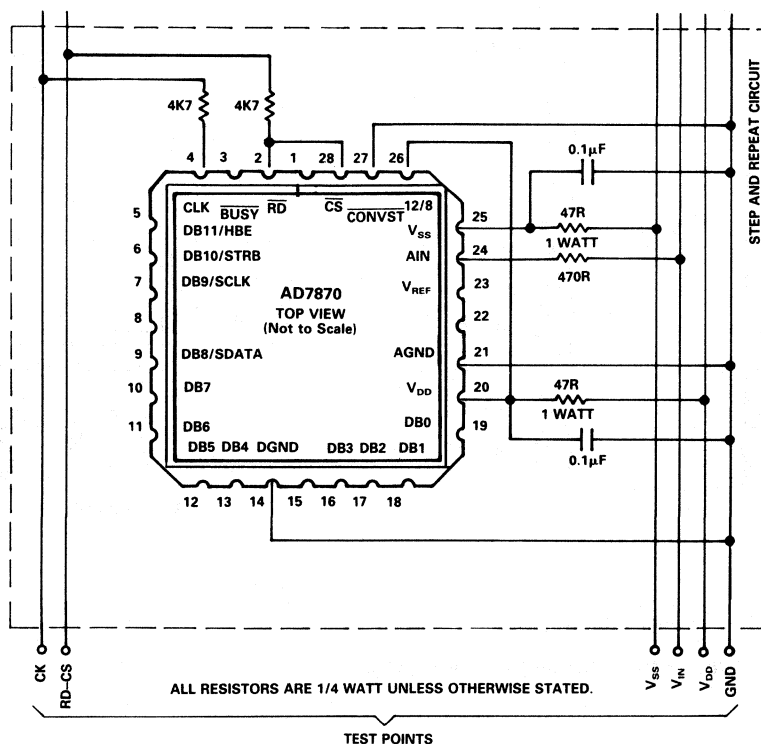
AD7870

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7870 Edge Connections (DIP)



AD7870 Edge Connections (LCC)

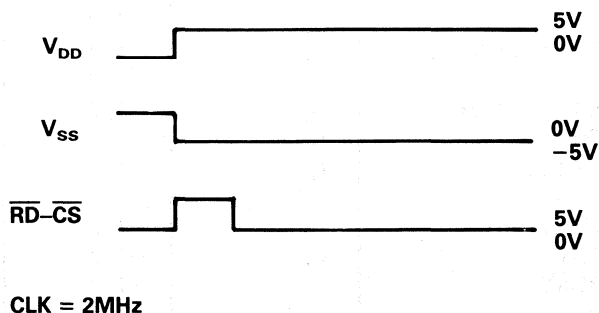
AD7870 Burn-In Philosophy

The AD7870 can be "burned in" under either static or dynamic conditions.

Static Burn-In

In this mode the circuit is subjected to maximum dc stress.

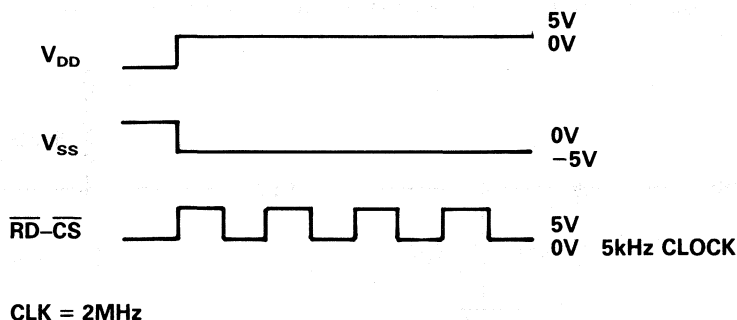
V_{IN} is tied to V_{SS} . After power-up a conversion is begun by pulling $\overline{CS}$ -RD low. When the conversion is complete, the output tri-state cells are loaded with result (1000 0000 0000) thus stressing the n-channels of the output buffers.



Dynamic Burn-In

In this mode all the AD7870 switching circuitry is subjected to dynamic stress.

V_{IN} is tied to a low frequency sine wave (100 Hz), ± 3.2 V. An asynchronous conversion start command on $\overline{CS}$ -RD performs a continuous stream of conversions. The output tri-state cells are enabled while $\overline{CS}$ -RD stays low.



NOTE

THE AD7870 MAY BE DRIVEN BY AN EXTERNAL TTL CLOCK (2MHz) OR THE INTERNAL CLOCK IS ENABLED WHEN CLK IS TIED TO V_{SS} .

V_{DD} AND V_{SS} SHOULD POWER-UP FIRST (APPROXIMATELY AT THE SAME TIME). CONTROL SIGNALS SHOULD THEN BE APPLIED.

ALL VOLTAGE TOLERANCES ARE $\pm 5\%$.

AD7870 TIMING^{1, 2}

Test	Symbol	Device	Design Limit T _{min} to T _{max}	Units
$\overline{\text{CONVST}}$ Pulse Width	t ₁	-1, 2	50	ns min
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time (Mode 1)	t ₂	-1, 2	0	ns min
$\overline{\text{RD}}$ Pulse Width	t ₃	-1, 2,	75	ns min
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time (Mode 1)	t ₄	-1, 2	0	ns min
$\overline{\text{RD}}$ to $\overline{\text{INT}}$ Delay	t ₅	-1, 2	70	ns max
Data Access Time after $\overline{\text{RD}}$	t ₆ ³	-1, 2	70	ns max
Bus Relinquish Time after $\overline{\text{RD}}$	t ₇ ⁴	-1, 2	5	ns min
			50	ns max
HBEN to $\overline{\text{RD}}$ Setup Time	t ₈	-1, 2	0	ns min
HBEN to $\overline{\text{RD}}$ Hold Time	t ₉	-1, 2	0	ns min
$\overline{\text{SSTRB}}$ to SCLK Falling Edge Setup Time	t ₁₀	-1, 2	100	ns min
SCLK Cycle Time	t ₁₁ ⁵	-1, 2	370	ns min
SCLK to Valid Data Delay, C _L = 35 pF	t ₁₂ ⁶	-1, 2	135	ns max
SCLK Rising Edge to $\overline{\text{SSTRB}}$	t ₁₃	-1, 2	100	ns min
Bus Relinquish Time after SCLK	t ₁₄	-1, 2	10	ns min
			100	ns max
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time (Mode 2)	t ₁₅	-1, 2	60	ns min
$\overline{\text{CS}}$ to $\overline{\text{BUSY}}$ Propagation Delay	t ₁₆	-1, 2	120	ns max
Data Setup Time Prior to $\overline{\text{BUSY}}$	t ₁₇	-1, 2	200	ns min
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time (Mode 2)	t ₁₈	-1, 2	0	ns min
HBEN to $\overline{\text{CS}}$ Setup Time	t ₁₉	-1, 2	0	ns min
HBEN to $\overline{\text{CS}}$ Hold Time	t ₂₀	-1, 2	0	ns min

NOTES

¹All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

²Serial timing is measured with a 4.7 k Ω pull-up resistor on SDATA and $\overline{\text{SSTRB}}$ and a 2 k Ω pull-up on SCLK. The capacitance on all three outputs is 35 pF.

³t₆ is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

⁴t₇ is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

⁵SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

⁶SDATA will drive higher capacitive loads but this will add to t₁₂ since it increases the external RC time constant (4.7 k Ω || C_L) and hence the time to reach 2.4 V.

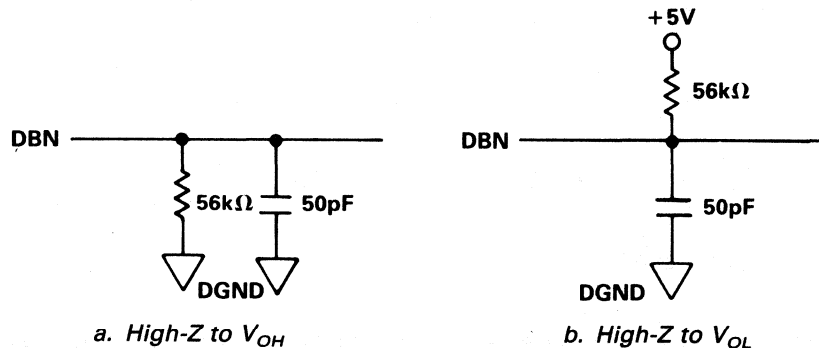


Figure 1. Load Circuits for Access Time

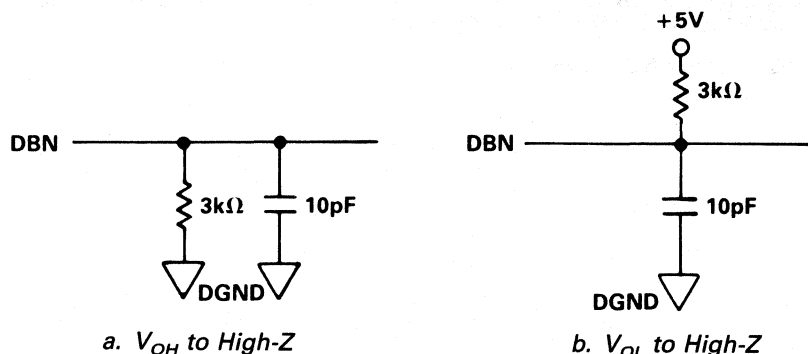


Figure 2. Load Circuits for Output Float Delay

6.0 Unipolar Operation.

A typical unipolar circuit is shown in Figure 3. The AD7870 REF OUT is used to offset the analog input by 3 V. The analog input range is determined by the ratio of R3 to R4. The minimum range with which the circuit will work is 0 to +3 V ($R3 = 0$, $R4 = \text{O/C}$). The resistor values are given in Figure 3 for input ranges of 0 to +5 V and 0 to +10 V. R5 and R6 are included for offset and full scale adjust only and should be omitted if adjustment is not required.

The output can be converted to natural binary by inverting the MSB.

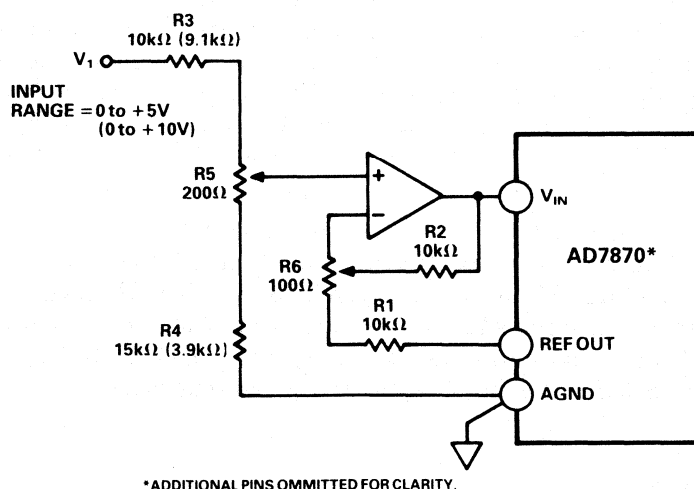


Figure 3. AD7870 Unipolar Circuit

6.1 Timing and Control.

The AD7870 is capable of two basic operating modes. In the first mode (Mode 1), the $\overline{\text{CONVST}}$ line is used to start conversion and drive the track/hold into its hold mode. At the end of conversion the track/hold returns to its tracking mode. It is intended principally for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases, the $\overline{\text{CONVST}}$ line is driven by a timer or some precise clock source.

The second mode is achieved by hard-wiring the $\overline{\text{CONVST}}$ line low. This mode (Mode 2) is intended for use in systems where the microprocessor has total control of the ADC, both initiating the conversion and reading the data. $\overline{\text{CS}}$ starts conversion and the microprocessor will normally be driven into a WAIT state for the duration of conversion by $\overline{\text{BUSY/INT}}$.

6.2 Data Output Formats.

In addition to the two operating modes, the AD7870 also offers a choice of three data output formats, one serial and two parallel. The parallel data formats are a single, 12-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the $12/\overline{8}/\text{CLK}$ input. A logic high on this pin selects the 12-bit parallel output format only. A logic low or -5 V applied to this pin allows the user access to either serial or byte formatted data. Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data. The three possible data output formats can be selected in either of the modes of operation.

Parallel Output Format

The two parallel formats available on the AD7870 are a 12-bit wide data word and a two-byte data word. In the first, all 12 bits of data are available at the same time on DB11 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB11/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the AD7870.

When HBEN is low, the lower 8 bits of data are placed on the data bus during a read operation; with HBEN high, the upper 4 bits of the 12-bit word are placed on the data bus. These 4 bits are right justified and thereby occupy the lower nibble of data while the upper nibble contains four zeros.

Serial Output Format

Serial data is available on the AD7870 when the $12/\overline{8}/\text{CLK}$ input is at 0 V or -5 V and in this case the DB10/ $\overline{\text{SSTRB}}$, DB9/SCLK and DB8/SDATA pins assume their serial functions. Serial data is available during conversion with a word length of 16 bits; four leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and is framed by the serial strobe ($\overline{\text{SSTRB}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{SSTRB}}$ output is low. $\overline{\text{SSTRB}}$ goes low within three clock cycles after $\overline{\text{CONVST}}$, and the first serial data bit (which is the first leading zero) is valid on the first falling edge of SCLK. All three serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC clock source which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases, it can be shut down at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7870 using the $12/\overline{8}/\text{CLK}$ input. With this input at -5 V, the serial clock (SCLK) runs continuously; when $12/\overline{8}/\text{CLK}$ is at 0 V, SCLK is turned off at the end of transmission.

6.3 Mode 1 Interface.

Conversion is initiated by a low going pulse on the $\overline{\text{CONVST}}$ input. The rising edge of this $\overline{\text{CONVST}}$ pulse starts conversion and drives the track/hold amplifier into its hold mode. The $\text{BUSY}/\overline{\text{INT}}$ status output assumes its $\overline{\text{INT}}$ function in this mode. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. This $\overline{\text{INT}}$ line can be used to interrupt the microprocessor. A read operation to the AD7870 accesses the data, and the $\overline{\text{INT}}$ line is reset high on the falling edge of CS and RD. The $\overline{\text{CONVST}}$ input must be high when CS and RD are brought low for the AD7870 to operate correctly in this mode. Trying to read parallel data during a conversion can cause errors to the conversion in progress. In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor $\overline{\text{WR}}$ line OR-gated with a decoded address.

Figure 4 shows the Mode 1 timing diagram for a 12-bit parallel data output format ($12/\overline{8}/\text{CLK} = +5$ V). A read to the AD7870 at the end of conversion accesses all 12 bits of data at the same time. Serial data is not available for this data output format.

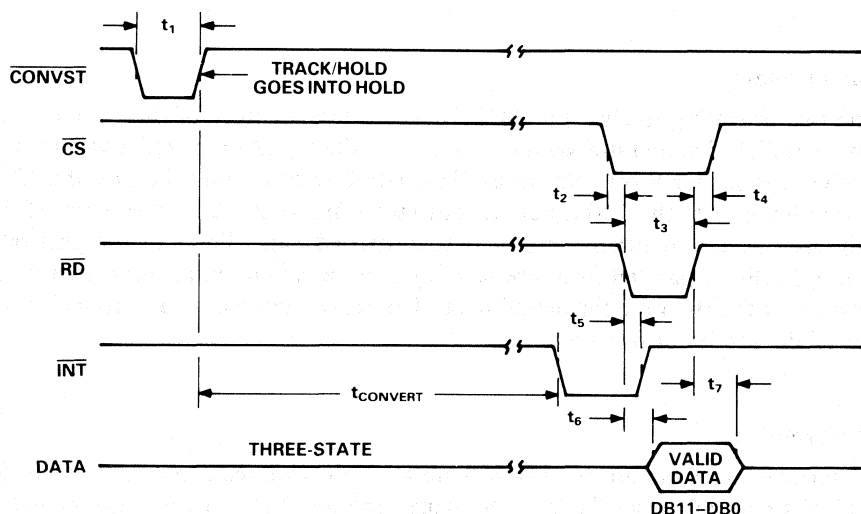


Figure 4. Mode 1 Timing Diagram, 12-Bit Parallel Read

The Mode 1 timing diagram for byte and serial data is shown in Figure 5. $\overline{\text{INT}}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. This first read at the end of conversion can either access the low byte or high byte of data depending on the status of HBEN (Figure 5 shows low byte only for example). The diagram shows both a noncontinuously and a continuously running clock (dashed line).

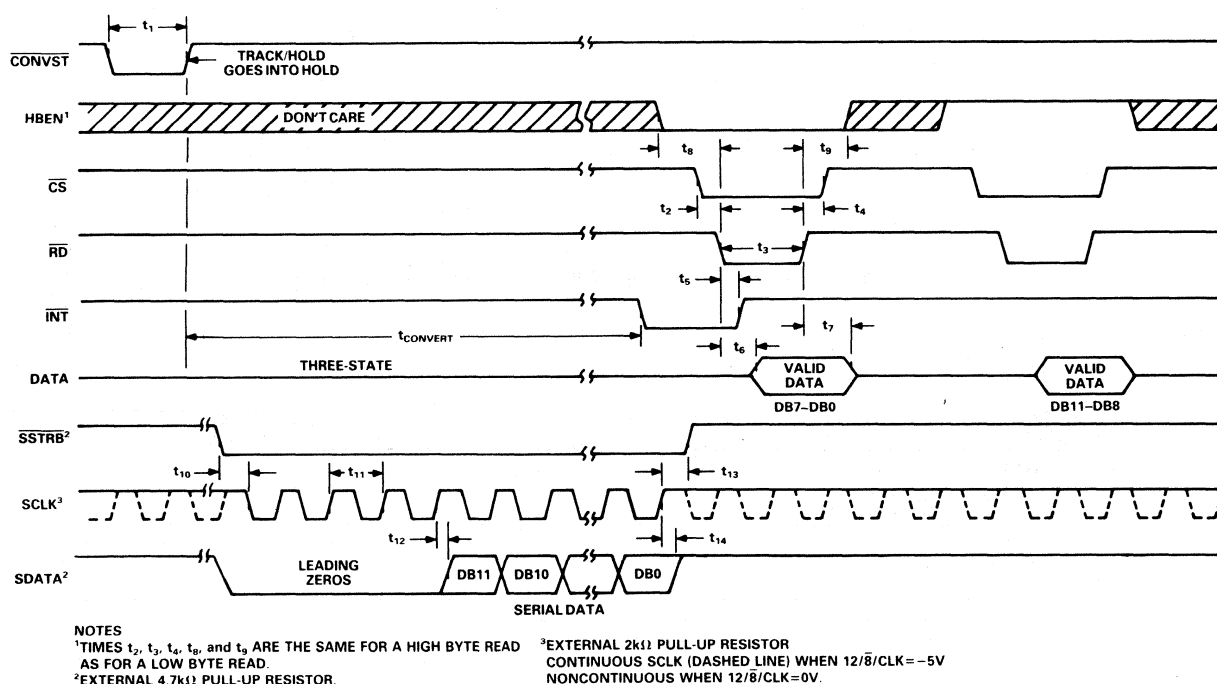


Figure 5. Mode 1 Timing Diagram, Byte or Serial Read

6.4 Mode 2 Interface.

The second interface mode is achieved by hard wiring $\overline{\text{CONVST}}$ low and conversion is initiated by taking $\overline{\text{CS}}$ low while HBEN is low. The track/hold amplifier goes into the hold mode on the falling edge of $\overline{\text{CS}}$. In this mode, the $\overline{\text{BUSY}}/\overline{\text{INT}}$ pin assumes its $\overline{\text{BUSY}}$ function. $\overline{\text{BUSY}}$ goes low at the start of conversion, stays low during the conversion and returns high when the conversion is complete. It is normally used in parallel interfaces to drive the microprocessor into a WAIT state for the duration of conversion.

Figure 6 shows the Mode 2 timing diagram for the 12-bit parallel data output format ($12/\bar{8}/\text{CLK} = +5\text{V}$). In this case, the ADC behaves like slow memory. The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then read data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion.

The Mode 2 timing diagram for byte and serial data is shown in Figure 7. For two-byte data read, the lower byte (DB0-DB7) has to be accessed first since HBEN must be low to start conversion. The ADC behaves like slow memory for this first read, but the second read to access the upper byte of data is a normal read. Operation of the serial functions is identical between Mode 1 and Mode 2. The timing diagram of Figure 7 shows both a noncontinuously and a continuously running SCLK (dashed line).

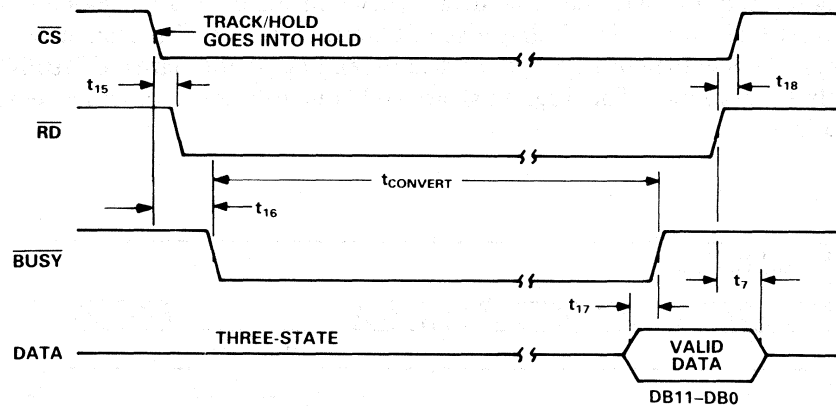
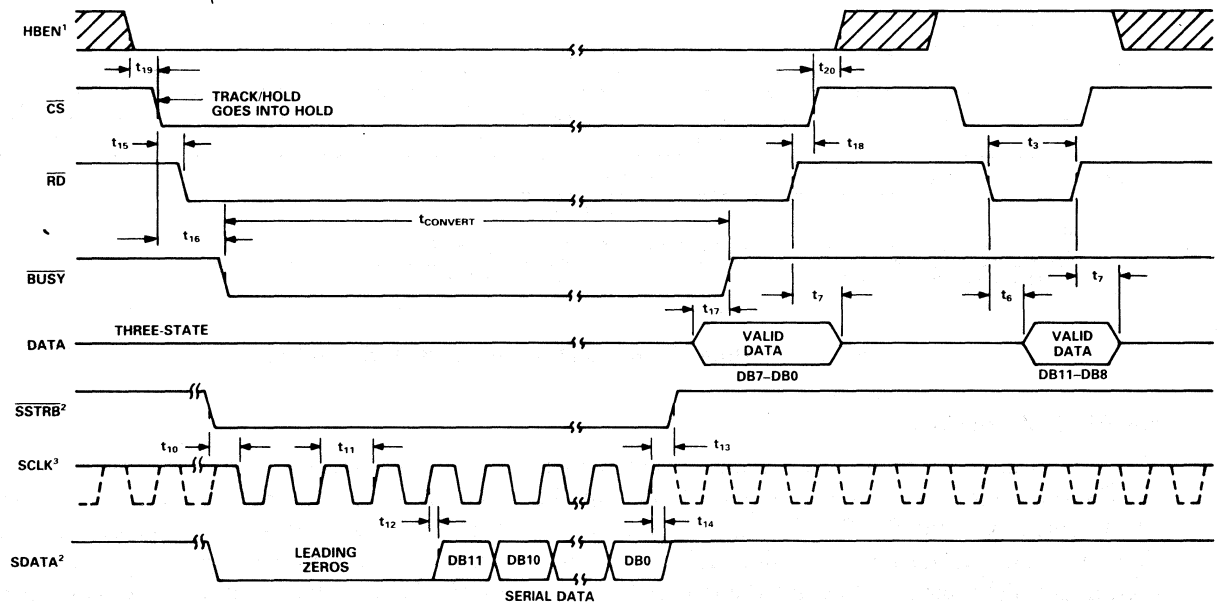


Figure 6. Mode 2 Timing Diagram, 12-Bit Parallel Read



NOTES

¹TIMES t_{15} , t_{16} , and t_{20} ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.

²EXTERNAL 4.7k Ω PULL-UP RESISTOR.

³EXTERNAL 2k Ω PULL-UP RESISTOR
CONTINUOUS SCLK (DASHED LINE) WHEN 12/8/CLK = -5V
NONCONTINUOUS WHEN 12/8/CLK = 0V.

Figure 7. Mode 2 Timing Diagram, Byte or Serial Read

1.1 Scope.

This specification covers the requirements for a 6-bit, high speed analog-to-digital converter with ECL compatible outputs and a bipolar input stage.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD9000S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-20A	28-Contact LCC
Q	Q-16	16-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage ($+V_S$)	0.3 V to +6.0 V
Negative Supply Voltage ($-V_S$)	-6.0 V to +0.3 V
Power Dissipation	1.1 W
Analog Input Voltages ($A_{IN}, +V_{REF}, -V_{REF}$) ¹	± 3 V
Analog-to-Digital Ground Voltage Differential	0.5 V
ENCODE Input Voltage	$-V_S$ to 0 V
HYSTERESIS Control Voltage	0 V to +3.0 V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$) ²	6.0 V
Digital Output Current	20 mA
Junction Temperature	+165°C
Operating Temperature Range (Ambient)	-55°C to +125°C
Storage Temperature Range (Case)	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTES

¹Under normal operating conditions, the analog input voltages should not exceed -2.0 V to +2.0 V.

²Under normal operating conditions the differential reference voltage may range from ± 0.5 V to ± 2.0 V, $+V_{REF} \geq -V_{REF}$.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA}	$= 67^\circ\text{C/W}$ for Cerdip
θ_{JC}	$= 7^\circ\text{C/W}$ for Cerdip
θ_{JA}	$= 62^\circ\text{C/W}$ for LCC
θ_{JC}	$= 23^\circ\text{C/W}$ for LCC

AD9000 – SPECIFICATIONS

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions ¹	Units
Input Bias Current Sampling	I _B	All	800	800	800					A _{IN} = +V _{REF}	μA max
Latched			20	20	20					-55°C ≤ T _A ≤ +125°C	
Conversion Time		All	13.3			13.3				See Note 4	ns max
Reference Ladder Resistance	R _R	All	80	80						See Notes 2, 3	Ω min
			200	200							Ω max
High Level Output Voltage	V _{OH}	All	-1.1	-1.1	-1.1					See Note 4 -55°C ≤ T _A ≤ +125°C	V min
Low Level Output Voltage	V _{OL}	All	-1.5	-1.5	-1.5					See Note 4 -55°C ≤ T _A ≤ +125°C	V max
Positive Supply Current (+5.0 V)	+I _{CC}	All	70	70	75					See Note 7 -55°C ≤ T _A ≤ +125°C	mA max
Negative Supply Current (-5.2 V)	-I _{CC}	All	80	80	85					See Note 7 -55°C ≤ T _A ≤ +125°C	mA max
Conversion Rate		All	75			75				See Note 4	MSPS min
Encode Pulse Width Low	t _{PW} (L)	All	6.6			6.6					ns min
High	t _{PW} (H)	All	6.6			6.6					ns min
Differential Linearity	DNL	All	0.5				0.5	1.0		Measured from 50% to 50% Transition -55°C ≤ T _A ≤ +125°C Measured from 50% to 50% Transition	LSB max
Integral Linearity	INL	All	0.5				0.5	1.0		Measured from 50% to 50% Transition -55°C ≤ T _A ≤ +125°C Measured from 50% to 50% Transition	LSB max
Top of Reference Ladder			28				28	48		Measured at 50% First Transition from A _{IN} = V _{REF} -55°C ≤ T _A ≤ +125°C Measured at 50% First Transition from A _{IN} = V _{REF}	mV max
Bottom of Reference Ladder			28				28	48		-55°C ≤ T _A ≤ +125°C	mV max
High Level Input Voltage	V _{IH}	All	-1.1				-1.1	-1.1		-55°C ≤ T _A ≤ +125°C	V min
Low Level Input Voltage	V _{IL}	All	-1.5				-1.5	-1.5		-55°C ≤ T _A ≤ +125°C	V min
High Level Input Current	I _{IH}	All	100				100	100		Measured at Input Logic Threshold -55°C ≤ T _A ≤ +125°C	μA max
Low Level Input Current	I _{IL}	All	100				100	100		Measured at Input Logic Threshold -55°C ≤ T _A ≤ +125°C	μA max
Output Hold Time	t _{OH}		8						8	See Notes 4, 6	ns min
			14						14		ns max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions ¹	Units
Output Delay	t_{PD}	All	8						8	See Notes 4, 5	ns min
			12						12		ns max
Output Rise Time	t_R	All	4.5						4.5	See Note 4	ns max
Output Fall Time	t_F	All	4.5						4.5	See Note 6	ns max

NOTES

¹Supply voltages = -5.2 V and +5.0 V; $R_1 = 100\ \Omega$ to -2.0 V; differential reference voltage = 2.0 V; $T_A = +25^\circ\text{C}$, unless otherwise specified.

²Under normal operating conditions, the analog input voltages should not exceed -2.0 V to +2.0 V.

³Under normal operating conditions, the differential reference voltage may range from $\pm 0.5\ \text{V}$ to $\pm 2\ \text{V}$; $+V_{REF} \geq -V_{REF}$.

⁴Output terminated to -2.0 V through $100\ \Omega$ resistors, or equivalent.

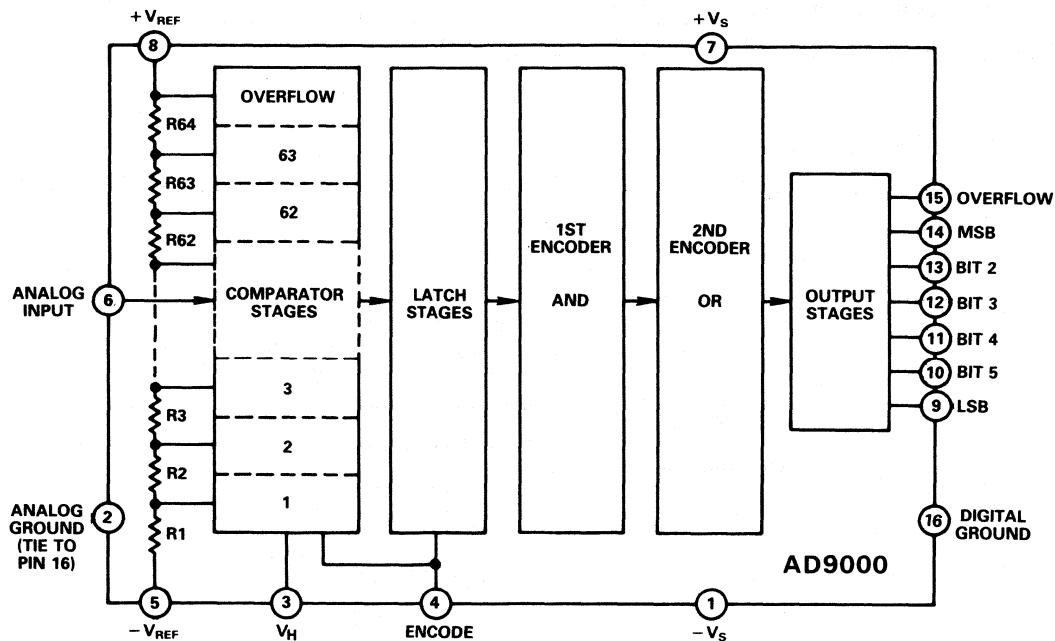
⁵Measured from leading edge of ENCODE to data out on most significant bit (MSB).

⁶Measured from trailing edge of ENCODE to data out on MSB.

⁷Supply voltages should remain stable within $\pm 5\%$ for normal operation.

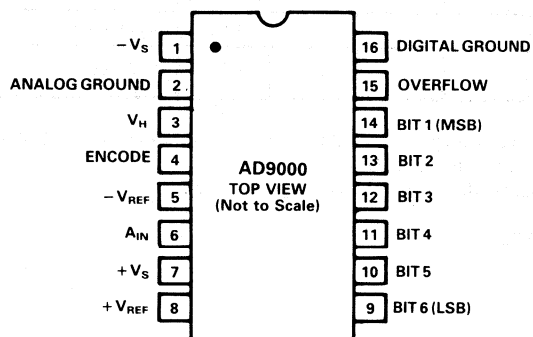
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

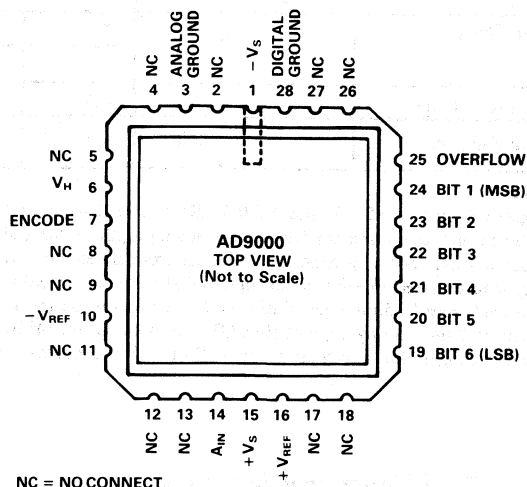


Pin Assignments

Cerdip (Q Package)



LCC (E Package)

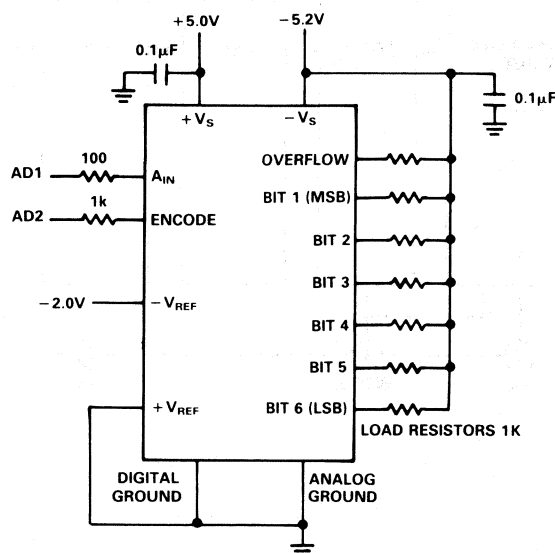


3.2.4 Microcircuit Technology Group.

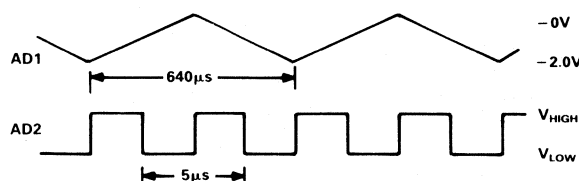
This microcircuit is covered by technology group D57.

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS $\pm 5\%$
ALL CAPACITORS $\pm 20\%$
ALL SUPPLY VOLTAGES $\pm 5\%$
OPTION #1: (STATIC) AD1=0.0V, AD2=LOGIC HIGH
OPTION #2: (DYNAMIC) SEE WAVEFORMS



1.1 Scope.

This specification covers the requirements for an 8-bit, high speed, analog-to-digital converter. The AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD9002S(X)/883B
-2	AD9002T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage ($-V_S$)	-6.0 V
Power Dissipation	1.2 W
Digital Input Voltage	$-V_S$ to 0 V
Reference Input Voltage ($+V_{REF}$, $-V_{REF}$) ¹	-3.5 V to +0.1 V
Differential Reference Voltage	2.1 V
Reference Midpoint Current	± 4 mA
Digital Output Current	20 mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage	4.0 V
Analog Input Voltage	$-V_S$ to +0.5 V
Junction Temperature ²	+175°C
Operating Temperature Range (Ambient)	-55°C to +125°C
Storage Temperature Range (Case)	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTES

¹ $+V_{REF} \geq -V_{REF}$ under all circumstances.

²Maximum Junction temperature should not exceed +175°C.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA}	= 56°C/W for Q-28
θ_{JC}	= 20°C/W for Q-28
θ_{JA}	= 69°C/W for E-28A
θ_{JC}	= 23°C/W for E-28A

AD9002 – SPECIFICATIONS

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions ¹	Units
Input Bias Current	I_B	All	100	100						$A_{IN} = 0\text{ V}$	$\mu\text{A max}$
			100		200					$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $A_{IN} = 0\text{ V}$	
Reference Ladder Resistance	R_R	All	64	64							$\Omega\text{ min}$
			110	110							$\Omega\text{ max}$
0 V Input Current	I_{IN}	All	300	300	300					$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\mu\text{A max}$
High Level Output Voltage	V_{OH}	All	-1.1	-1.1	-1.1					See Note 2 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	V min
Low Level Output Voltage	V_{OL}	All	-1.5	-1.5	-1.5					See Note 2 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	V max
Negative Supply Current (-5.2 V)	$-I_{CC}$		175	175						$A_{IN} = 0\text{ V}$, See Note 4	mA max
					200					$A_{IN} = 0\text{ V}$, See Note 4 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	
Conversion Rate		All	125			125					MSPS min
Encode Pulse Width (Low)	$t_{PW}(L)$	All	1.5			1.5				See Note 3	ns min
Encode Pulse Width (High)	$t_{PW}(H)$	All	1.5			1.5				See Note 3	ns min
Signal-to-Noise Ratio	SNR	All	46			46				Encode Rate = 125 MSPS RMS Signal to RMS Noise	dB min
Differential Linearity	DNL	-1	0.75				0.75			$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	LSB max
		-2	0.5				0.5	1.0		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	
Integral Linearity	INL	-1	1.0				1.0			$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	LSB max
		-2	0.5				0.5	1.2		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	
Top of Reference Ladder		All	14				14	17		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	LSB max
Bottom of Reference Ladder		All	10				10	12		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	mV max
High Level Input Voltage	V_{IH}	All	-1.1				-1.1	-1.1		See Note 2 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	V min
Low Level Input Voltage	V_{IL}	All	-1.5				-1.5	-1.5		See Note 2 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	V max
High Level Input Current	I_{IH}	All	150				150	150		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\mu\text{A max}$
Low Level Input Current	I_{IL}	All	120				120	120		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\mu\text{A max}$
Power Supply Rejection	PSRR	All	1.5				1.5			Measured at $-5.2\text{ V} \pm 5\%$	mV/V max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions ¹	Units
Output Delay	t_{PD}	All	2.5						2.5	Measured from 50% Point of Rising ENCODE to 50% Point of LSB Transition; See Note 2	ns min
			5.5						5.5		ns max
Output Rise Time	t_R	All	3.0						3.0	Measured from 10% to 90% Points LSB Only; See Note 2	ns max
Output Fall Time	t_F	All	2.5						2.5	Measured from 10% to 90% Points LSB Only; See Note 2	ns max
In-Band Harmonics		All	48			48					dB min

NOTES

¹ $V_{EE} = -5.2$ V; $+V_{REF} = 0$ V; $-V_{REF} = -2.0$ V; digital outputs terminated to -2.0 V through $100\ \Omega$ or equivalent; $T_A = +25^\circ\text{C}$, unless otherwise specified.

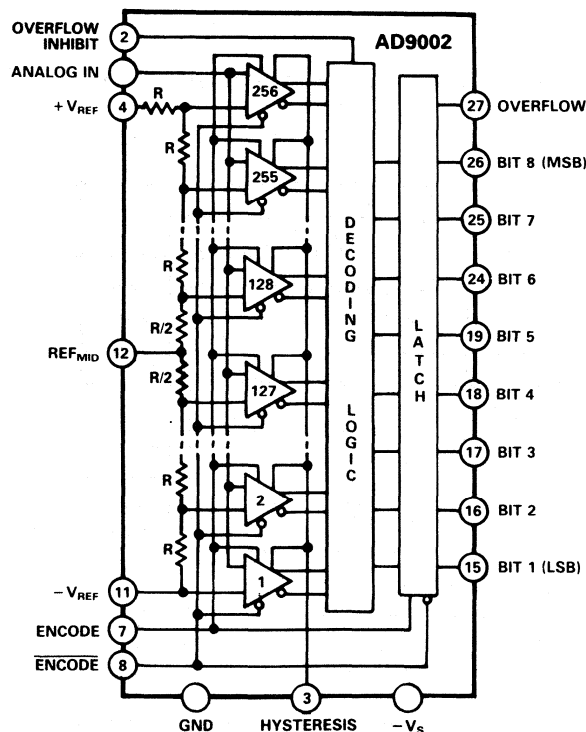
²Outputs terminated to -2.0 V through $100\ \Omega$ resistors or equivalent.

³ENCODE signal rise/fall times should be less than 10 ns for normal operation.

⁴Supply voltages should remain stable within $\pm 5\%$ for normal operation.

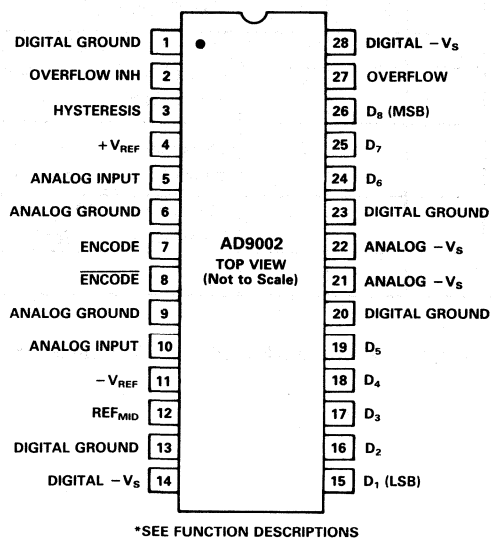
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

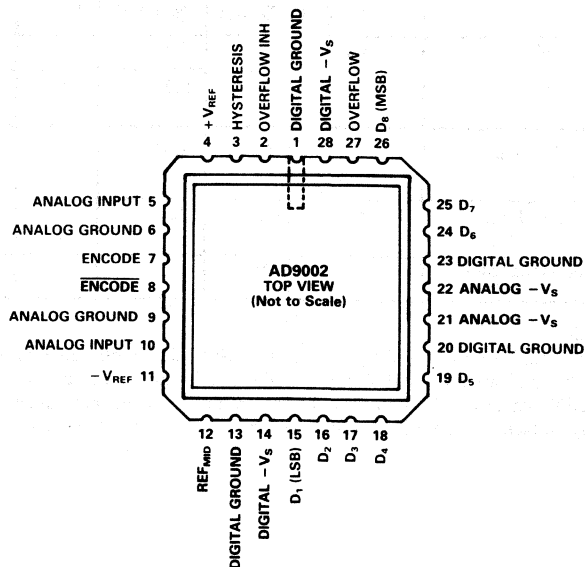


Pin Assignments

DIP (Q Package)



LCC (E Package)

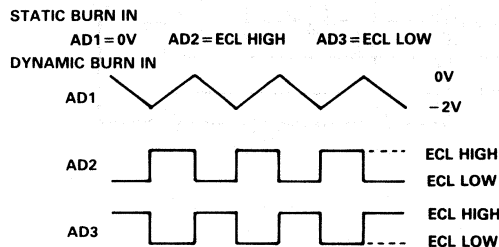
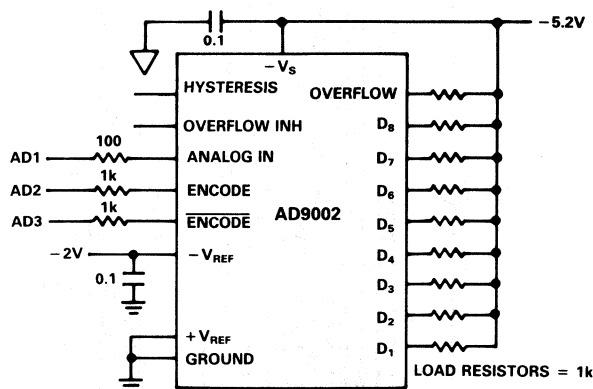


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group D57.

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS $\pm 5\%$, Ω
 ALL CAPACITORS $\pm 20\%$, μF
 ALL SUPPLIES $\pm 5\%$

1.1 Scope.

This specification covers the requirements for an 8-bit, ultrahigh speed TTL analog-to-digital converter.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD9012S(X)/883B
-2	AD9012T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000 package outline:

(X)	Package	Description
E	E-20A	20-Contact LCC
Q	Q-28	28-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage ($+V_S$)	+6.0 V
Negative Supply Voltage ($-V_S$)	-6.0 V
Power Dissipation	1.6 W
Analog Input Voltage	$-V_S$ to +0.5 V
Analog-to-Digital Supply Voltage Differential	0.5 V
ENCODE Input Voltage	-0.5 V to +5.0 V
OVERFLOW INH Input Voltage	-5.2 V to 0 V
Reference Input Voltage ($+V_{REF} - V_{REF}$) ¹	-3.5 V to 0.1 V
Differential Reference Voltage	2.1 V
Reference Midpoint Current	± 4 mA
Digital Output Current	30 mA
Junction Temperature	+165°C
Operating Temperature Range (Ambient)	-55°C to +125°C
Storage Temperature Range (Case)	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTE

¹ $+V_{REF} \geq -V_{REF}$ under all circumstances.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA}	$= 56^\circ\text{C/W}$ for Q-28
θ_{JC}	$= 20^\circ\text{C/W}$ for Q-28
θ_{JA}	$= 69^\circ\text{C/W}$ for E-20A
θ_{JC}	$= 23^\circ\text{C/W}$ for E-20A

AD9012 – SPECIFICATIONS

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions ¹	Units
Input Bias Current	I_B	All	100	100	200					$A_{IN} = 0\text{ V}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $A_{IN} = 0\text{ V}$	$\mu\text{A max}$
Input Resistance	R_I	All	150	150							$\text{k}\Omega\text{ min}$
Reference Ladder Resistance	R_R	All	64/110	64/110							$\Omega\text{ min/max}$
0 V Input Current	I_{IN}	All	250	250	250						$\mu\text{A max}$
High Level Output Voltage	V_{OH}	All	+2.4	+2.4	+2.4					See Note 2	V min
Low Level Output Voltage	V_{OL}	All	+0.4	+0.4	+0.4					See Note 2	V max
Positive Supply Current (+5.0 V)	$+I_{CC}$	All	45	45.0	48					See Note 3 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mA max
Negative Supply Current (-5.2 V)	$-I_{CC}$	All	179	179	191					See Note 3 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mA max
Conversion Rate		All	75			75					MSPS min
Encode Pulse Width (Low)	$t_{PW}\text{ (L)}$	All	2.5			2.5				See Note 4	ns min
Encode Pulse Width (High)	$t_{PW}\text{ (H)}$	All	2.5			2.5				See Note 4	ns min
Signal-to-Noise Ratio (5)	SNR	All	46			46				Analog Input = 1.23 MHz RMS Signal to RMS Noise	dB min
Differential Linearity	DNL	-1	0.75				0.75	1.0		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	LSB max
		-2	0.5				0.5	0.75		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	
Integral Linearity	INL	-1	1.0				1.0	1.2		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	LSB max
		-2	0.5				0.5	1.2		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	
Top of Reference Ladder		All	10				10	13		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mV max
Bottom of Reference Ladder		All	15				15	18		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mV max
High Level Input Voltage	V_{IH}	All	2.0				2.0	2.0		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	V min
Low Level Input Voltage	V_{IL}	All	0.8				0.8	0.8		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	V max
High Level Input Current	I_{IH}	All	250				250	250		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	$\mu\text{A max}$
Low Level Input Voltage	I_{IL}	All	220				220	220		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	$\mu\text{A max}$
Power Supply Rejection Ratio	PSRR	All	2.5				2.5			Measured at -5.2 V $\pm 5\%$ and +5.0 V $\pm 5\%$ See Note 3	mV/V max
Output Delay	t_{PD}	All	5						5.0	Measured from 50% Point of Rising ENCODE to 50% of Point of LSB Transition, See Note 2	ns min
			11						11.0		ns max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions ¹	Units
Output Rise Time	t_R	All	8.0						8.0	See Note 2	ns max
Output Fall Time	t_F	All	4.3						4.3	See Note 2	ns max
In-Band Harmonics		All	48			48				Analog Input = 1.23 MHz See Note 5	dB min

NOTES

¹— $V_S = -5.2$ V; $+V_S = +5.0$ V; Differential reference voltage = 2.0 V; $T_A = +25^\circ\text{C}$, unless otherwise specified.

²Outputs terminated with two equivalent 'LS00-type loads.

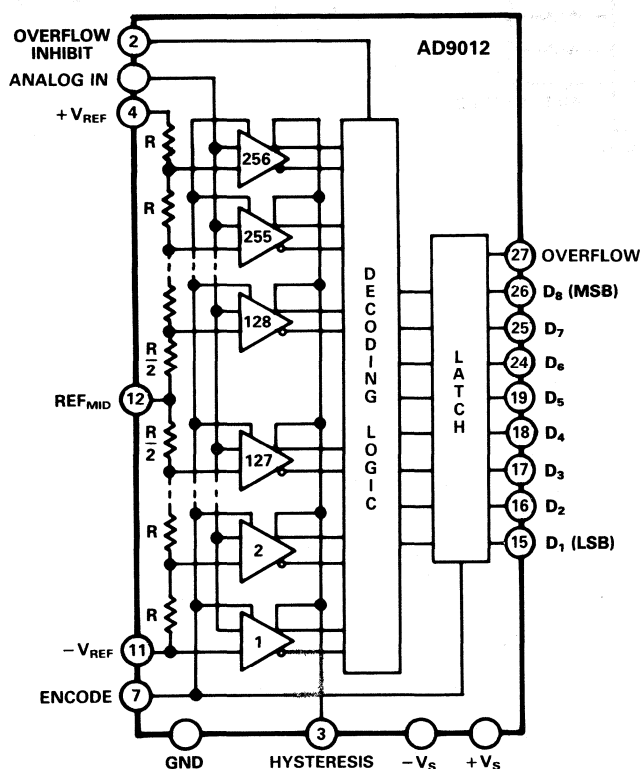
³Supply voltages should remain stable within $\pm 5\%$ for normal operation.

⁴ENCODE signal rise/fall times should be less than 30 ns for normal operation.

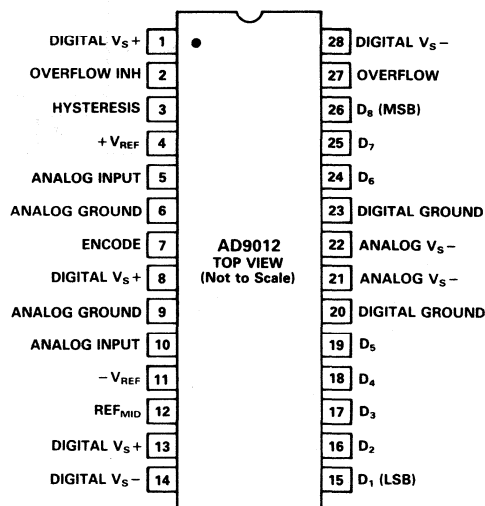
⁵Measured at 75 MSPS encode rate. Harmonic data based on worst case harmonics.

Table 1.

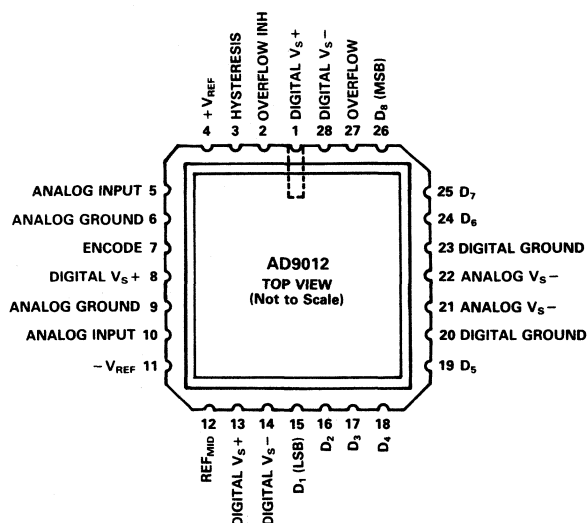
3.2.1 Functional Block Diagram and Terminal Assignments.



DIP (Q) Package



LCC (E) Package



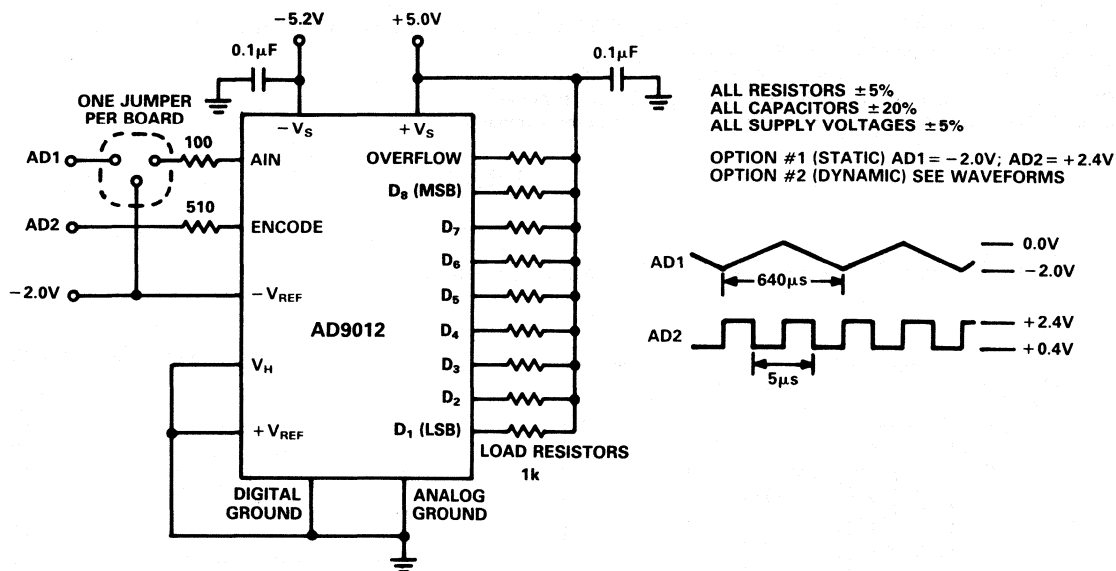
AD9012

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the requirements for an 8-bit, 35 MSPS flash converter.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
–1	AD9048S(X)/883B
–2	AD9048T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to DGND	–0.5 V to +7.0 V
AGND to DGND	–0.5 V to +0.5 V
V_{EE} to AGND	+0.5 V to –7.0 V
V_{IN} , V_{RT} or V_{RB} to AGND	+0.5 V to V_{EE}
V_{RT} to V_{RB}	–2.2 V to +2.2 V
CONV, NMINV or NLINV to DGND	–0.5 V to +5.5 V
Applied Output Voltage to DGND ¹	–0.5 V to +5.5 V
Applied Output Current, Externally Forced ^{2, 3}	–1.0 mA to +6.0 mA
Output Short Circuit Duration ⁴	1.0 sec
Junction Temperature	+175°C
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range (Case)	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTES

¹Applied voltage must be current limited to specific range.

²Forcing voltage must be limited to specified range.

³Current is specified as negative when flowing into the device.

⁴Output High; one pin to ground; one second duration.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA}	= 49°C/W for Q-28
θ_{JC}	= 15°C/W for Q-28
θ_{JA}	= 69°C/W for E-28A
θ_{JC}	= 21°C/W for E-28A

AD9048 – SPECIFICATIONS

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Condition ¹	Units
Input Bias Current	I_B	All	36	60	100					$V_{CC} = +5.5\text{ V}$ $V_{EE} = 5.5\text{ V}$	$\mu\text{A max}$
Input Resistance	R_I	All	300	200							$\text{k}\Omega\text{ min}$
Reference Ladder Resistance	R_R	All	90	50							$\Omega\text{ min}$
				125							$\Omega\text{ max}$
Input Current	I_{IN}	All		200	200					$+0.4; V_{CC} = +5.5\text{ V};$ $V_{EE} = -4.9\text{ V}$	$\mu\text{A max}$
				10	10					$+2.4\text{ V}; V_{CC} = +5.5\text{ V};$ $V_{EE} = -4.9\text{ V}$	
				10	10					$+5.5\text{ V}; V_{CC} = +5.5\text{ V};$ $V_{EE} = -4.9\text{ V}$	
High Level Output Voltage	V_{OH}	All		2.4	2.4					$V_{CC} = +4.5\text{ V};$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	V min
Low Level Output Voltage	V_{OL}	All		0.5	0.5					$V_{CC} = +4.5\text{ V};$ $V_{EE} = -4.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	V max
Positive Supply Current +5.5 V	$+I_{CC}$	All	34	46	48					$V_{EE} = -5.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	mA max
Negative Supply Current -5.5 V	$-I_{CC}$	All	90	110	120					$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	mA max
Conversion Rate		All	38			35				$V_{CC} = +4.5\text{ V};$ $V_{EE} = -4.9\text{ V}$	MSPS min
Encode Pulse Width (Low)	$t_{PW} (L)$	All				18					ns min
Pulse Width (Low)	$t_{PW} (H)$	All				10					ns min
Signal-to-Noise Ratio	SNR	-1	44			43.5				See Notes 5 and 6, Input = 1.248 MHz.	dB min
			44			43				See Notes 5 and 6, Input = 2.438 MHz.	
			53			52.5				See Notes 5 and 7, Input = 1.248 MHz.	
			53			52				See Notes 5 and 7, Input = 2.438 MHz.	
		-2	46			45				See Notes 5 and 6, Input = 1.248 MHz.	
			46			44				See Notes 5 and 6, Input = 2.438 MHz.	
			55			54				See Notes 5 and 7, Input = 1.248 MHz.	
			55			53				See Notes 5 and 7, Input = 2.438 MHz.	
		-1	44			43.5				See Note 8, Input = 1.248 MHz.	
		-2	46			43				See Note 8, RMS Signal to RMS Noise.	

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Condition ¹	Units
Differential Linearity	DNL	-1	0.4				0.75	1.0		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	LSB max
		-2	0.3				0.5	0.5		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	
Reference Ladder Current		All	23	40	40					$V_{EE} = -4.9\text{ V};$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mA max
Output Hold Time	t_{OH}	All	8						5	See Note 2	
Integral Linearity	INL	-1	0.6				0.75	1.0		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	LSB max
		-2	0.4				0.5	0.5		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	
Top of Reference Ladder Offset Error		All	5				12	12		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mV max
Bottom of Reference Ladder Offset Error		All	4				10	10		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	mV max
High Level Input Voltage	V_{IH}	All					2.0	2.0		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	V min
Low Level Input Voltage	V_{IL}	All	4				0.8	0.8		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	V max
High Level Input Current	I_{IH}	All		15	15					$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $+2.4\text{ V}; V_{CC} = +5.5\text{ V}$ $V_{EE} = -4.9\text{ V}$	$\mu\text{A max}$
		All		15	15					$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $+5.5\text{ V}; V_{CC} = +5.5\text{ V}$ $V_{EE} = -4.9\text{ V}$	$\mu\text{A max}$
Low Level Input Current	I_{IL}	All		500	500					$V_{CC} = +5.5\text{ V};$ $V_{EE} = -4.9\text{ V}$	$\mu\text{A max}$
Output Time Skew		All	4.5						7	See Note 3	ns max
Short Circuit Current	I_{SC}	All		30	30					$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C};$ See Note 4	mA max
Output Delay	t_{PD}	All	9						12	$V_{CC} = +5.5\text{ V};$ $V_{EE} = -4.9\text{ V}$	ns max
Output Rise Time	t_R	All							9		ns max
Output Fall Time	t_F	All							14		ns max
In-Band Harmonics		-1	50			47				See Note 5	dBc
		-2	55			49					

NOTES

¹ $V_S = -5.2\text{ V}; +V_S = +5.0\text{ V}$; differential reference voltage = 2.0 V; $T_A = +25^{\circ}\text{C}$, unless otherwise specified.

² Interval from 50% point of leading edge of convert pulse to change in output data.

³ Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

⁴ Output high; one pin to ground; one-second duration.

⁵ Measured at 20 MSPS encode rate with analog input 1 dB below full scale.

⁶ RMS signal to rms noise.

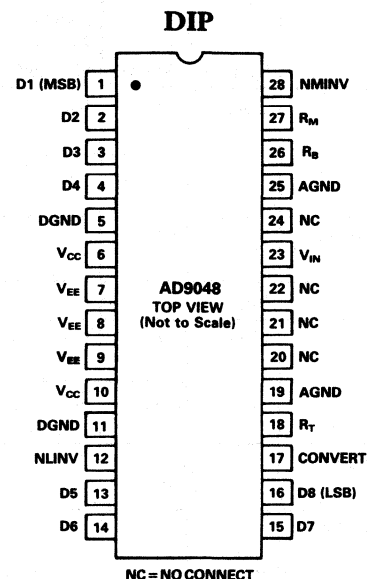
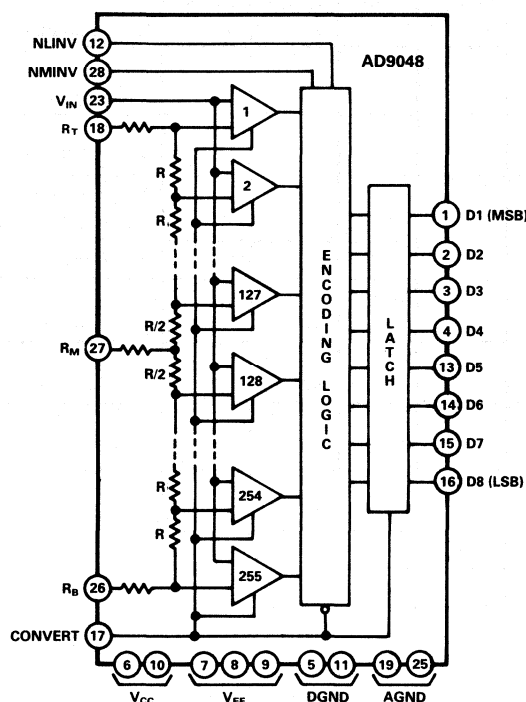
⁷ Peak signal to rms noise.

⁸ Measured at 35 MSPS encode rate with analog input 1 dB below full scale.

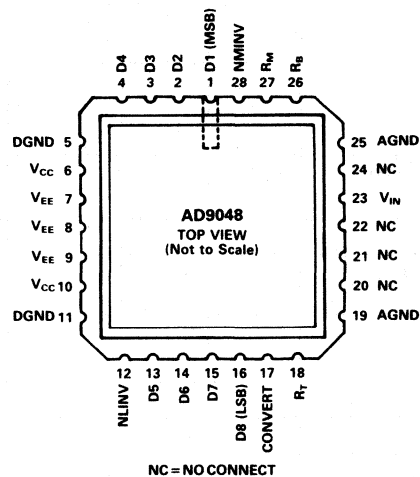
Table 1.

AD9048

3.2.1 Functional Block Diagram and Terminal Assignments.



LCC

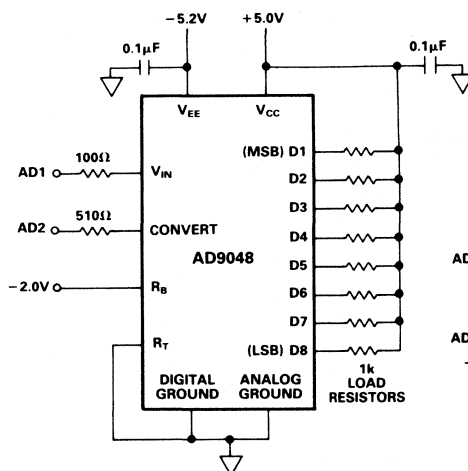


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group D-57.

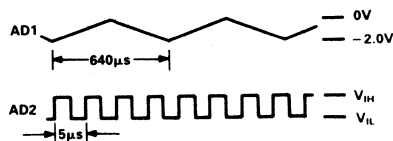
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTOR $\pm 5\%$
ALL CAPACITORS $\pm 20\%$
ALL SUPPLY VOLTAGES $\pm 5\%$

OPTION #1 (STATIC): AD1 = -2.0V; AD2 = +2.4V
OPTION #2 (DYNAMIC): SEE WAVEFORMS



1.1 Scope.

This specification covers the requirements for an ultrafast voltage comparator. The AD96685 is a single comparator with a 2.5 ns propagation delay, and the AD96687 is an equally fast dual comparator.

1.2 Part Number.

The complete part number per Table 1 this specification is as follows:

Device	Part Number
-1	AD96685T(X)/883B
-2	AD96687T(Y)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	(Y)	Package	Description
E	E	E-20A	20-Contact LCC
Q	Q	Q-16	16-Pin Ceramic DIP
H		H-10A	10-Pin TO-100 Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 6.5\text{ V}$
Power Dissipation	AD96685 = 500 mW; AD96687 = 600 mW
Input Voltage Range	$\pm 5\text{ V}$
Differential Input Voltage	5.5 V
Output Current	30 mA
Latch Enable Voltage	$-V_S$ to 0 V
Junction Temperature	$+175^\circ\text{C}$
Operating Temperature Range (Case)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range (Case)	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 31^\circ\text{C}$ for E-20A (AD96687)
θ_{JA}	$= 82^\circ\text{C/W}$ for E-20A (AD96687)
θ_{JC}	$= 65^\circ\text{C/W}$ for E-20A (AD96685)
θ_{JA}	$= 172^\circ\text{C/W}$ for E-20A (AD96685)
θ_{JC}	$= 52^\circ\text{C/W}$ for H-10A
θ_{JA}	$= 172^\circ\text{C/W}$ for H-10A
θ_{JC}	$= 57^\circ\text{C/W}$ for Q-16
θ_{JA}	$= 115^\circ\text{C/W}$ for Q-16

AD96685/AD96687 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group ² 2, 3	Sub Group 4	Sub Group ^{2, 3, 4, 5} 5, 6	Sub Group 9	Test Condition ¹	Units
Input Offset Current	I _{IO}	-1	±1	±1	±1.6				V _{CM} = +0.5 V	μA max
		-2	±1	±1	±1.2				V _{CM} = 0 V; +0.5 V -V _{CM} = -0.5 V	
Input Offset Voltage	V _{OS}	-1	±2	±2.0	±3.0				R _S = 100 Ω	mV max
		-2	±2	±2.0	±3.0				V _{CM} = 0 V	
Input Offset Voltage Tempco	ΔV _{OS} /ΔT	-1	±20	±20	±20				R _S = 100 Ω V _{CM} = 0 V	μV/°C max
		-2	±20	±20	±20					
Input Bias Current	I _{IB}	-1	10	10	16				+V _{CM} = +0.5 V -V _{CM} = -0.5 V	μA max
		-2	10	10	16				R _S = 100 Ω V _{CM} = 0 V; ±0.5 V	
Input Voltage Range	V _{CM}	-1, 2	-2.5	-2.5	-2.5					V min
			+5.0	+5.0	+5.0					V max
Common Mode Rejection Ratio	CMRR	-1, 2	90			80	80		-2.5 V ≤ V _{CM} ≤ +5.0 V	dB min
Power Supply Rejection Ratio	PSRR	-1	70			60	60		R _S = 100 Ω	dB min
		-2				60	60		ΔV _S = ±5%	
High Level Output Voltage	V _{OH}	-1, 2		-1.10	-1.10					V min
Low Level Output Voltage	V _{OL}	-1, 2		-1.50	-1.50					V max
Positive Supply Current	+I _{CC}	-1	9	9	9					mA max
		-2	18	18	18					
Negative Supply Current	-I _{CC}	-1	18	18	18					mA max
		-2	36	36	36					
Propagation Delay Time	t _{PD} ±	-1	2.5					9	See Note 6	ns max
		-2	2.5					1.5		ns min
								3.5		ns max
Propagation Delay Time Latch Enable to Output	t _{PD} ±(E)	-1	2.5					3.5		ns max
		-2	2.5					3.5		

NOTES

¹Unless otherwise specified, T_A = +25°C; +V_S = +5.0 V; V_S = -5.2 V.

²-55°C ≤ T_A ≤ +125°C.

³+V_S = +5.0 V; V_S = -5.2 V; V_T = -2.0 V; R_L = 50 Ω.

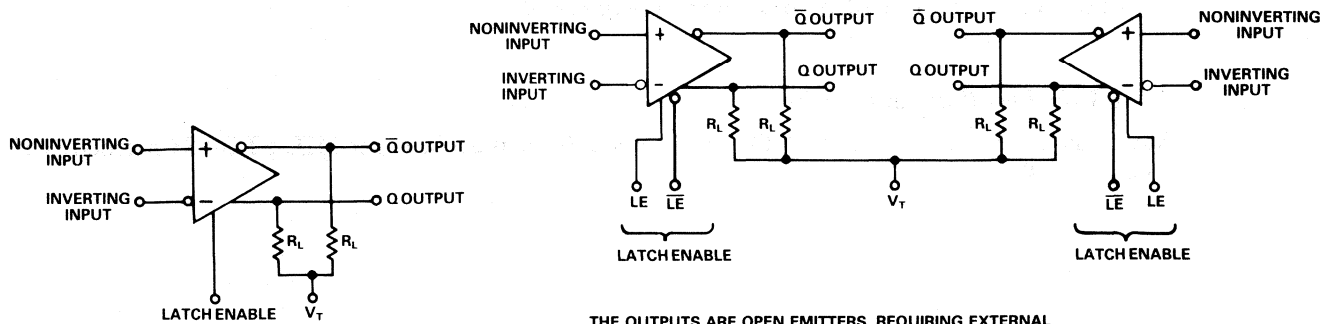
⁴Devices require a thermal equilibrium to be established with a transverse airflow of >500 LFPM.

⁵Production pulse test devices at correlated temperatures of -35°C and +145°C to compensate for high power steadystate operation.

⁶This parameter measured with 100 mV pulse (10 mV overdrive), to 50% of the transition output point.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



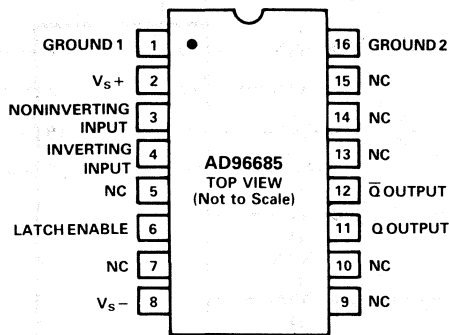
THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50 Ω – 200 Ω CONNECTED TO –2.0V, OR 200 Ω – 2000 Ω

AD96685

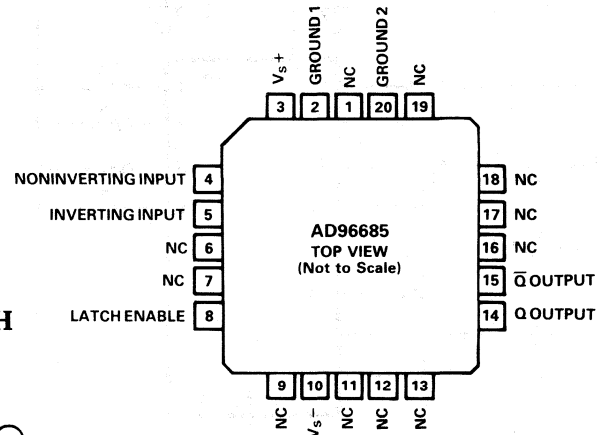
AD96687

Pin Assignments

AD96685TQ



AD96685TE



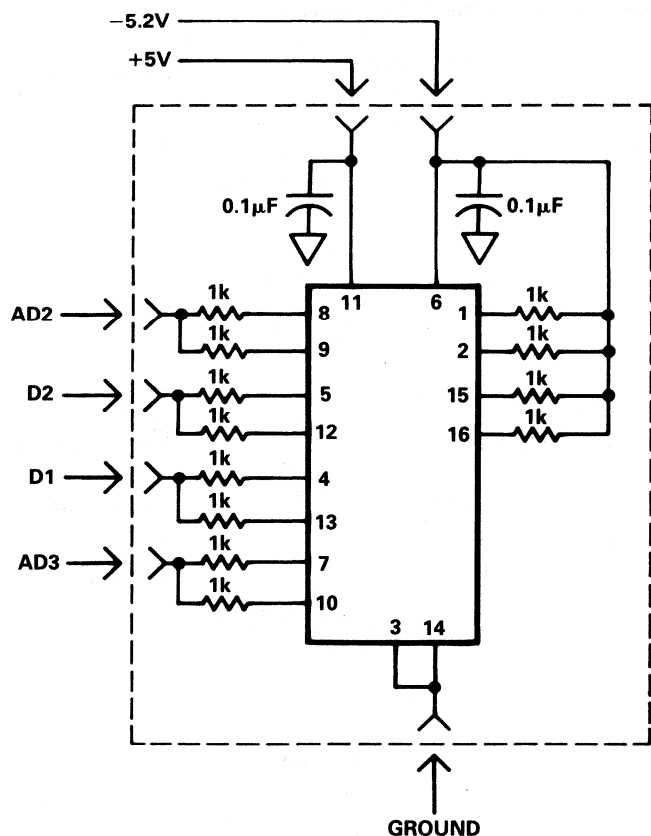
AD96685/AD96687

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-50).

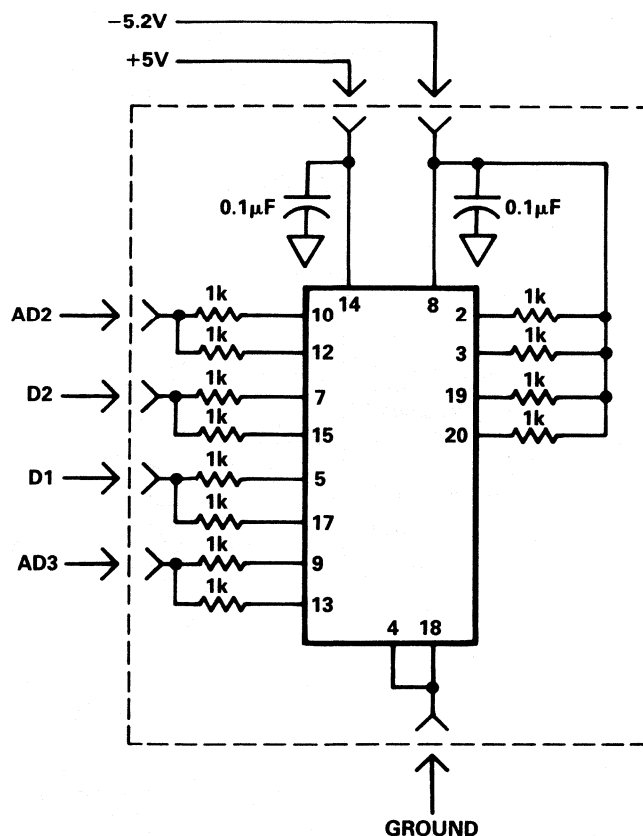
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS $\pm 5\%$
 $+V_s = +5.0V \pm 5\%$
 $-V_s = -5.2V \pm 5\%$

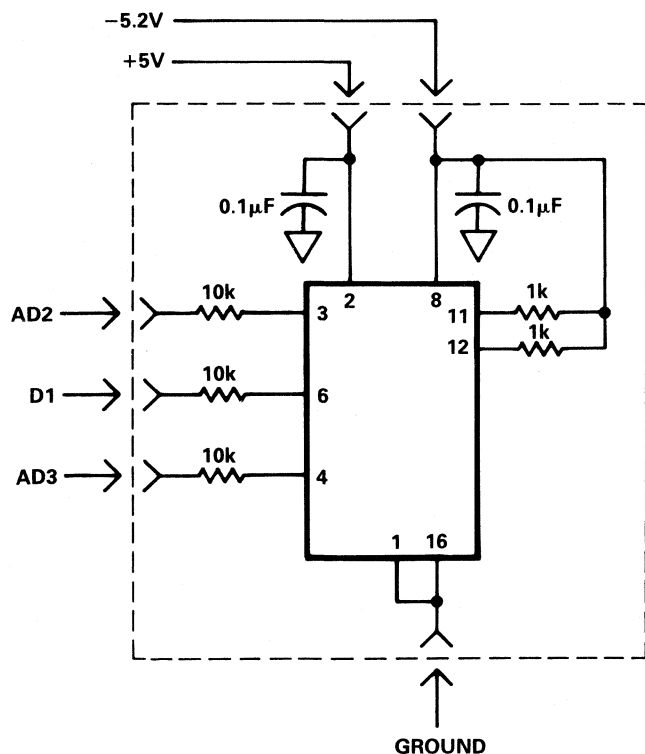
AD96687 (16-Pin DIP)



ALL RESISTORS $\pm 5\%$
 $+V_s = +5.0V \pm 5\%$
 $-V_s = -5.2V \pm 5\%$

AD96687 (20-Pin LCC)

AD96685/AD96687

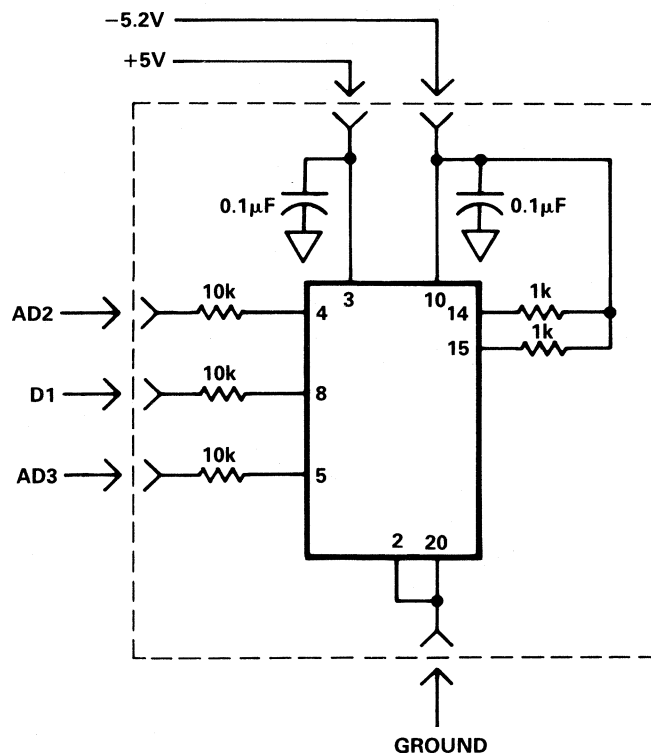


ALL RESISTORS $\pm 5\%$

$+V_s = +5.0V \pm 5\%$

$-V_s = -5.2V \pm 5\%$

AD96685 (16-Pin DIP)

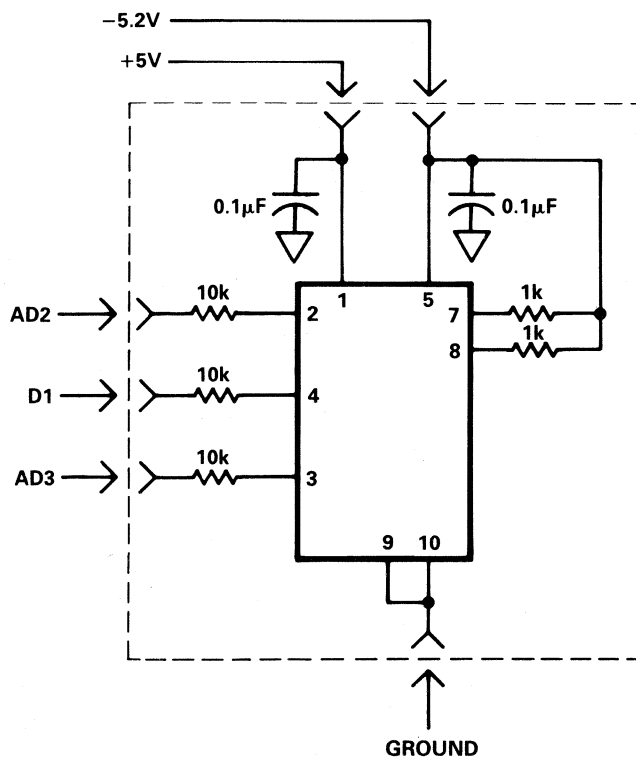


ALL RESISTORS $\pm 5\%$

$+V_s = +5.0V \pm 5\%$

$-V_s = -5.2V \pm 5\%$

AD96685 (20-Pin LCC)



ALL RESISTORS $\pm 5\%$

$+V_s = +5.0V \pm 5\%$

$-V_s = -5.2V \pm 5\%$

AD96685 (TO-100)

REV. A



12-Bit
Monolithic D/A Converter

AD DAC87

1.1 Scope.

This specification covers the detail requirements for a complete monolithic 12-bit voltage output D/A converter. (The hybrid version is detailed on page 979.)

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD DAC87D-CBI-V/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

+ V _S to Power Ground	0V to +18V
– V _S to Power Ground	0V to –18V
Signal Inputs (Pins 1 to Pin 12) to Power Ground	–1.0V to +7V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Ref Out	Indefinite Short-to-Power Ground or + V _S
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W
 θ_{JA} = 48°C/W

AD DAC87 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	– 1	1/2	1/2	3/4		All Bits with Positive Errors On All Bits Negative Errors On	± LSB max
Differential Nonlinearity	DNL	– 1	3/4	3/4	1		Major Transitions	± LSB max
Gain Error	A _E	– 1	0.2	0.2				± % FSR max
Gain Temperature Coefficient	TCA _E	– 1	20		20		Includes Internal Reference	± ppm/°C max
Offset Error	V _{OS}	– 1	0.1	0.1				± % FSR max
Offset Temperature Coefficient	TCV _{OS}	– 1	3		3			± ppm/°C max
Bipolar Offset Error	B _{POE}	– 1	0.1	0.1			Bipolar	± % FSR max
B/P Offset Temperature Coefficient	TCB _{POE}	– 1	10		10		Bipolar	± ppm/°C max
Reference Output Voltage	V _{REF}	– 1	6.23 6.37	6.23 6.37			No External Load and 2.5mA External Load	V min V max
Reference Temperature Coefficient	V _{REFTC}	– 1	20		10		No External Load	± ppm/°C max
Slew Rate	V _{SL}	– 1	10					V/μs min
Settling Time to 0.01% FSR	t _{SL}	– 1	4				FSR Change with 10kΩ Feedback	μs max
			3				5kΩ Feedback	
Output Short Circuit Current	I _{SC}	– 1	40					mA max
Power Supply Rejection	PSR	– 1	0.002	0.002			13.5V ≤ V _{CC} ≤ 16.5V, V _{EE} = – 15V V _{CC} = 15V, – 16.5V ≤ V _{EE} ≤ – 13.5V 11.4V ≤ V _{CC} ≤ 12.6V, V _{EE} = – 12V V _{CC} = 12V, – 12.6V ≤ V _{EE} ≤ – 11.4V	± % FSR/% max
Power Supply Current	I _{CC}	– 1	10	10				mA max
	I _{EE}	– 1	20	20				
Digital Input High Voltage	V _{IH}	– 1	2.0	2.0	2.0			V min
Digital Input Low Voltage	V _{IL}	– 1	0.8	0.8	0.8			V max
Digital Input High Current	I _{IH}	– 1	250	250			V _{IH} = 5.5V	μA max
Digital Input Low Current	I _{IL}	– 1	100	100			V _{IL} = 0.8V	μA max
Output Current	I _{OUT}	– 1	5					± mA min

NOTE

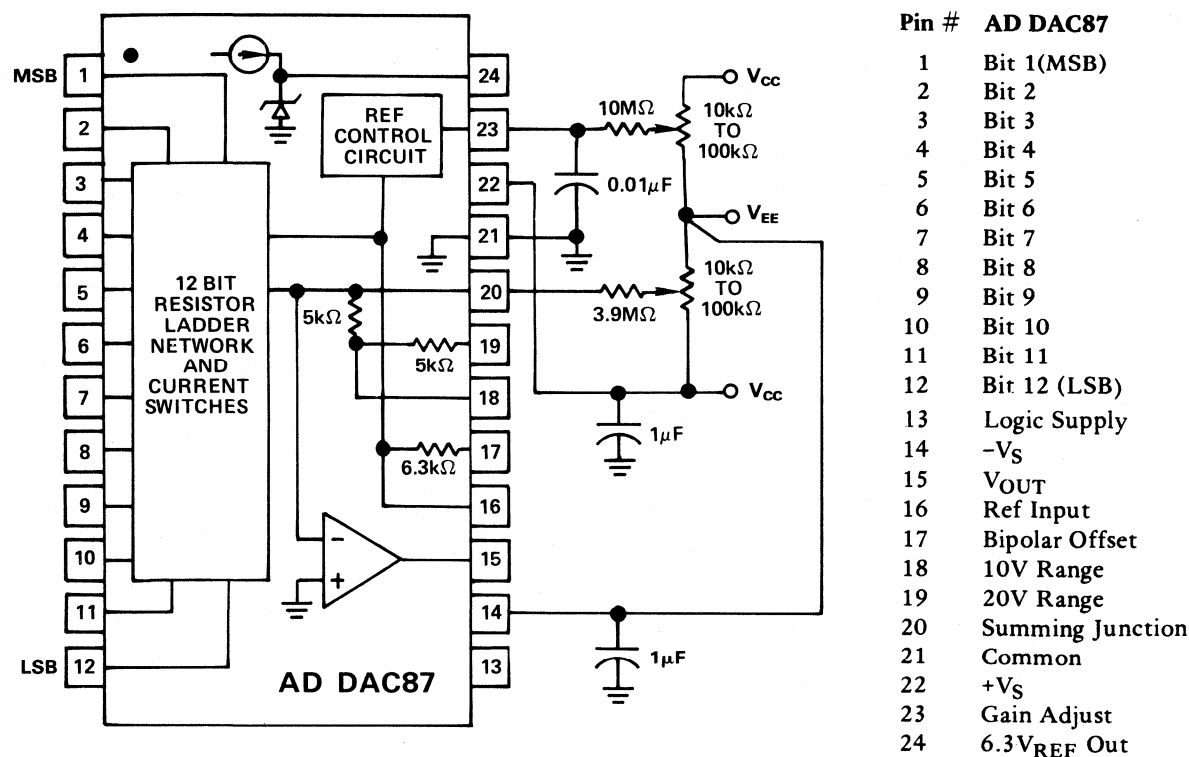
¹V_{CC} = + 15V, V_{EE} = – 15V, Pin 16 to Pin 24. Unipolar configuration unless otherwise noted.

Unipolar – 0 to + 10V: Pin 15 to Pin 18, Pin 17 to Pin 21, Pin 19 open.

Bipolar – ± 10V: Pin 15 to Pin 19, Pin 17 to Pin 20, Pin 18 open.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

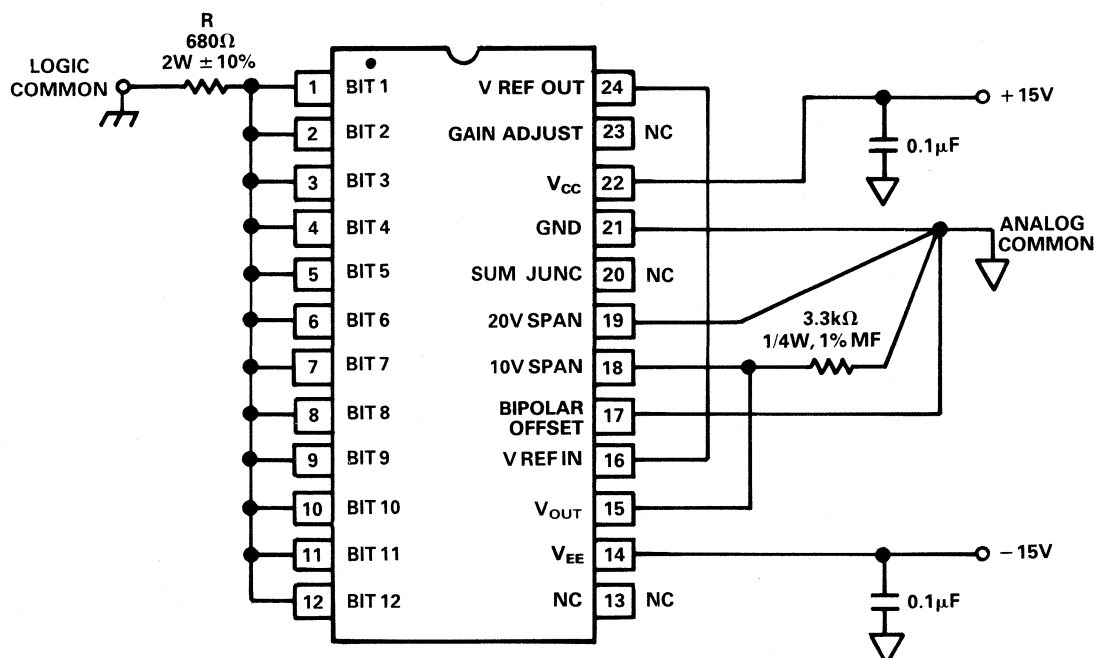


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADG201A/ADG202A
1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS analog switches, each consisting of four independent single-pole, single-throw switches. They differ only in that the digital control logic is inverted.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	ADG201AT(X)/883B
– 2	ADG202AT(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V–	44V
V+ to GND	25V
V– to GND	– 25V
Analog Inputs	
Voltage at S, D	V– to V+
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs	
Voltages at IN	V– – 2V to V+ + 2V or 20mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	900mW/°C
Derates above +75°C by	12mW/°C
Operating Temperature	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C
Junction Temperature (T_J)	+ 175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

ADG201A/ADG202A – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch “ON” Resistance	R_{DS}	– 1, 2	145	90	145	$V_{IN}=0.8V$ for – 1 Device and 2.4V for – 2 Device; $V_D = \pm 10V$, $I_S = \mp 1.0mA$ (See Figure 1)	Ω max
		– 1, 2	200	200	200	$V_+ = 10V$, $V_- = -10V$; $V_D = \pm 7.5V$; $V_{IN} = 0.8V$ for – 1 Device and 2.4V for – 2 Device; $I_S = \mp 1.0mA$ (See Figure 1)	Ω max
Source “OFF” Leakage Current	$I_S(OFF)$	– 1, 2	100	1	100	$V_D = \pm 14V$, $V_S = \mp 14V$; $V_{IN} = 2.4V$ for – 1 Device and 0.8V for – 2 Device, (See Figure 2)	$\pm nA$ max
Drain “OFF” Leakage Current	$I_D(OFF)$	– 1, 2	100	1	100	$V_D = \pm 14V$, $V_S = \mp 14V$; $V_{IN} = 2.4V$ for – 1 Device and 0.8V for – 2 Device, (See Figure 3)	$\pm nA$ max
Channel “ON” Leakage Current	$I_D(ON)$	– 1, 2	200	1	200	$V_D = \pm 14V$, All Other Digital Inputs = 0.8V for – 1 Device and 2.4V for – 2 Device (See Figure 4)	$\pm nA$ max
Digital Input High Voltage	V_{INH}	– 1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	– 1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	– 1, 2	1.0	0.5	1.0	$V_{IN} = 15V$; All Other Digital Inputs = 0.8V (See Figure 5)	$\pm \mu A$ max
Low Level Input Current	I_{INL}	– 1, 2	1.0	0.5	1.0	$V_{IN} = 0.8V$; All Other Digital Inputs = 2.4V (See Figure 5)	$\pm \mu A$ max
Supply Current	$+I_{CC}$	– 1, 2	2.0	1.5	2.0	$V_{IN} = 0V$ or 5V For All Digital Inputs $S1 \dots S4 = D1 \dots D4 =$ Open Circuit (See Figure 6)	mA max
	$-I_{CC}$	– 1, 2	2.0	1.5	2.0	$V_{IN} = 0V$ or 5.0V For All Digital Inputs $S1 \dots S4 = D1 \dots D4 =$ Open Circuit (See Figure 6)	mA max
Subgroup 9, 11 Turn “ON” Time Turn “OFF” Time	$t_{(ON)}$	– 1, 2	600			$T_A = +25^\circ C$ and $-55^\circ C$; $C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
	$t_{(OFF)}$	– 1, 2	500				ns max
Subgroup 10 Turn “ON” Time Turn “OFF” Time	$t_{(ON)}$	– 1, 2	800			$T_A = +125^\circ C$; $C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
	$t_{(OFF)}$	– 1, 2	650				ns max
Subgroup 12 Off Isolation	V_{ISO}	– 1, 2	60			$T_A = +25^\circ C$; $f = 200kHz$ $V_{GEN} = 1V$ p-p; $R_L = 1k$ (See Figure 8)	dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	– 1, 2	60			$T_A = +25^\circ C$; $f = 200kHz$ $V_{GEN} = 1V$ p-p; $R_L = 1k$ (See Figure 9)	dB min
Subgroup 14 Charge Transfer Error	V_{CTE}	– 1, 2	10			$T_A = +25^\circ C$; (See Figure 10)	$\pm mV$ max
Capacitance: Address	C_A	– 1, 2	15			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 0V$	pF max
Capacitance: Input Switch	C_{IS}	– 1, 2	15			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 5V$	pF max
Capacitance: Output Switch	C_{OS}	– 1, 2	20			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 5V$	pF max

NOTE

¹Unless otherwise noted $V_+ = +15V$; $V_- = -15V$.

Table 1.

MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10, 11
Group C End Point Electrical Parameters, Method 5005	1, 10, 11 and Table 3 Delta Limits

*Indicates P.D.A. applies to Subgroup 1.

Table 2. Electrical Test Requirements

Parameters ²	Delta Limits at +25°C ¹ Device Types	
	1	2
R _{DS}	15Ω	15Ω
I _D (ON)	1nA	1nA

NOTES

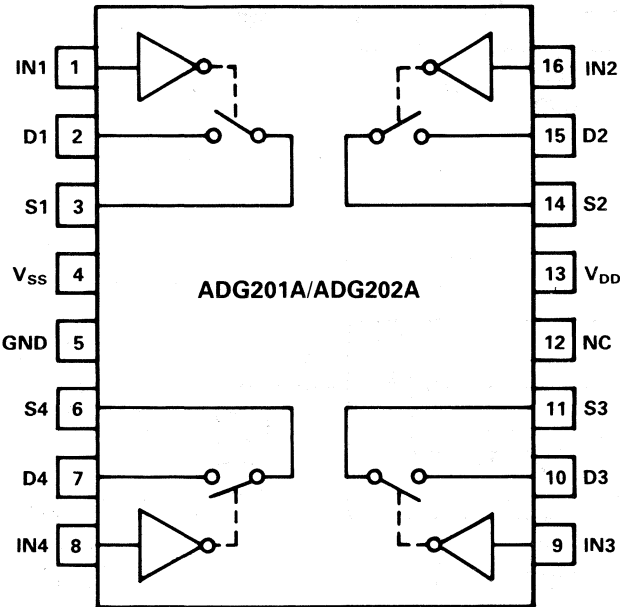
¹Each test applies to every switch in the package.

²Each of the above parameters shall be recorded before and after the required burn-in and life-tests to determine deltas (Δ).

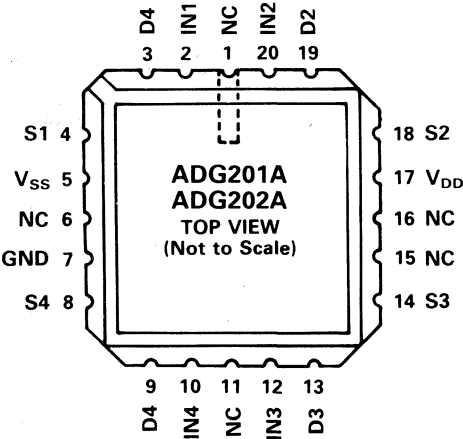
Table 3.

3.2.1 Functional Block Diagram and Terminal Assignments.

Q Package (Cerdip)



E Package (LCC)



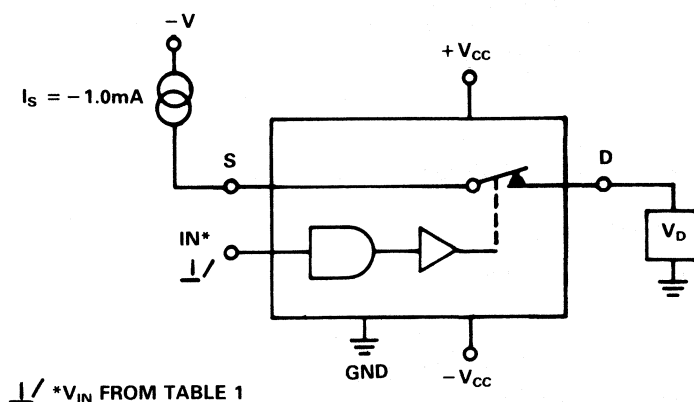
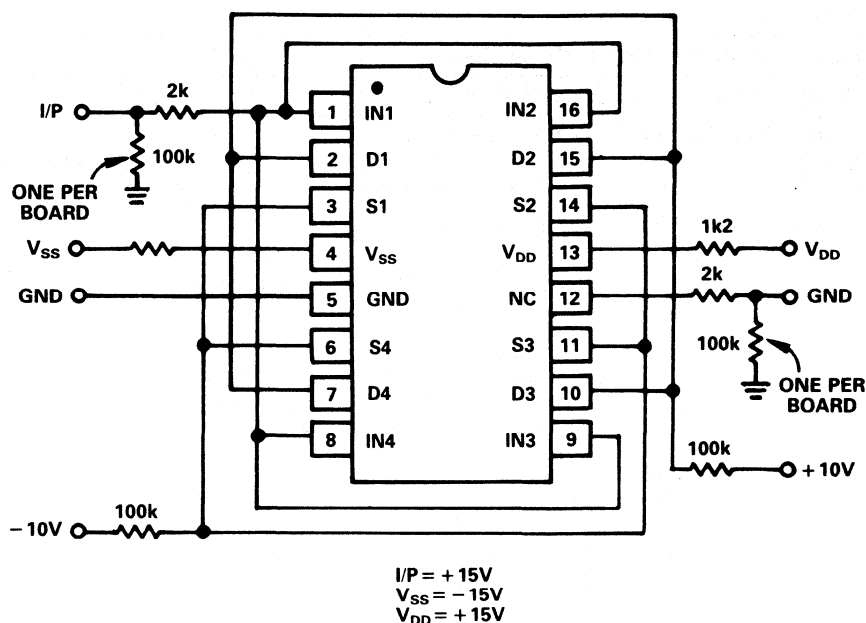
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

ADG201A/ADG202A

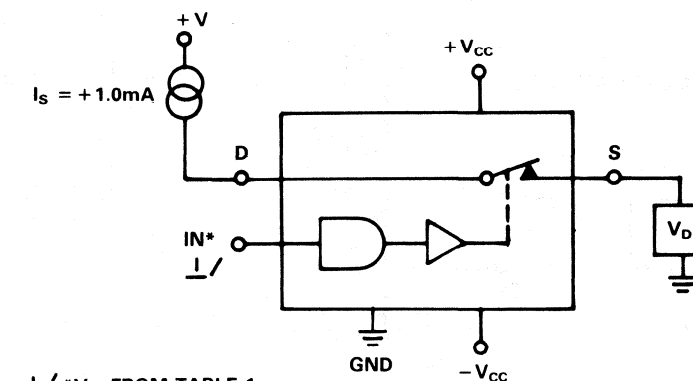
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



$-V_{IN}$ FROM TABLE 1

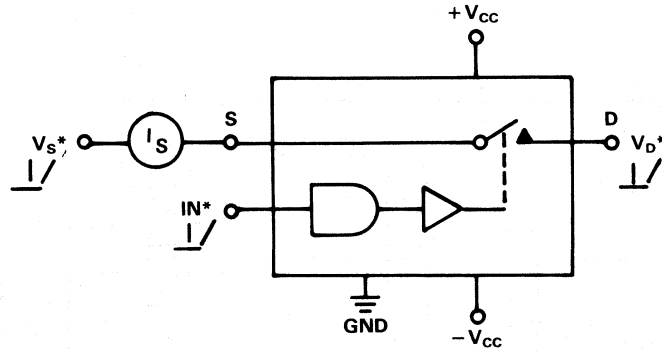
$$R_{DS} = \frac{V_S - V_D}{-1.0\text{mA}}$$



$+V_{IN}$ FROM TABLE 1

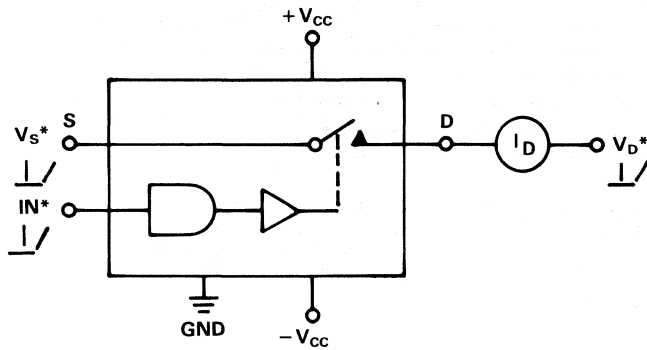
$$R_{DS} = \frac{V_S - V_D}{+1.0\text{mA}}$$

Figure 1. R_{DS} Test Circuits



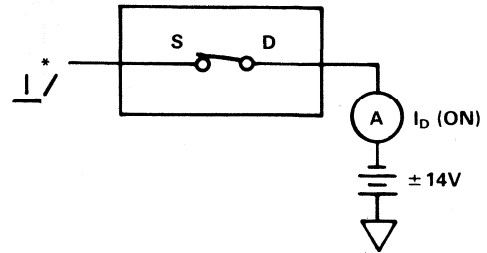
$\perp/\perp$ *TEST CONDITIONS ARE FROM TABLE 1.

Figure 2. I_S (OFF) Test Circuit



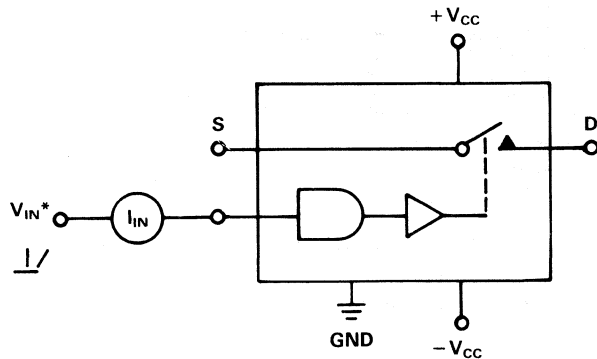
$\perp/\perp$ *TEST CONDITIONS ARE FROM TABLE 1.

Figure 3. I_D (OFF) Test Circuit



$\perp/\perp$ *CONDITIONS ARE FROM TABLE 1.

Figure 4. I_D (ON) Test Circuit



$\perp/\perp$ *CONDITIONS ARE FROM TABLE 1.

Figure 5. I_{INL} , I_{INH} Test Circuit

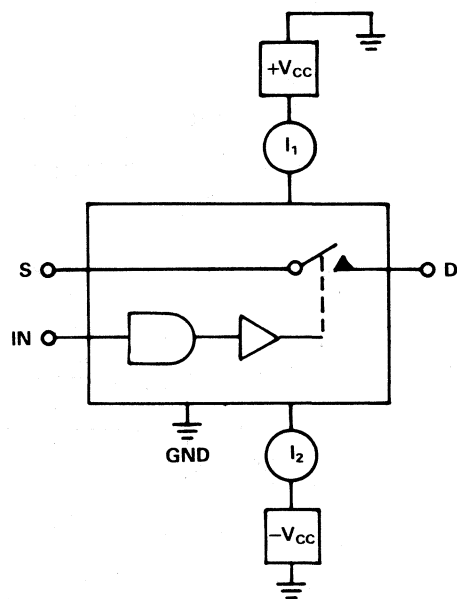
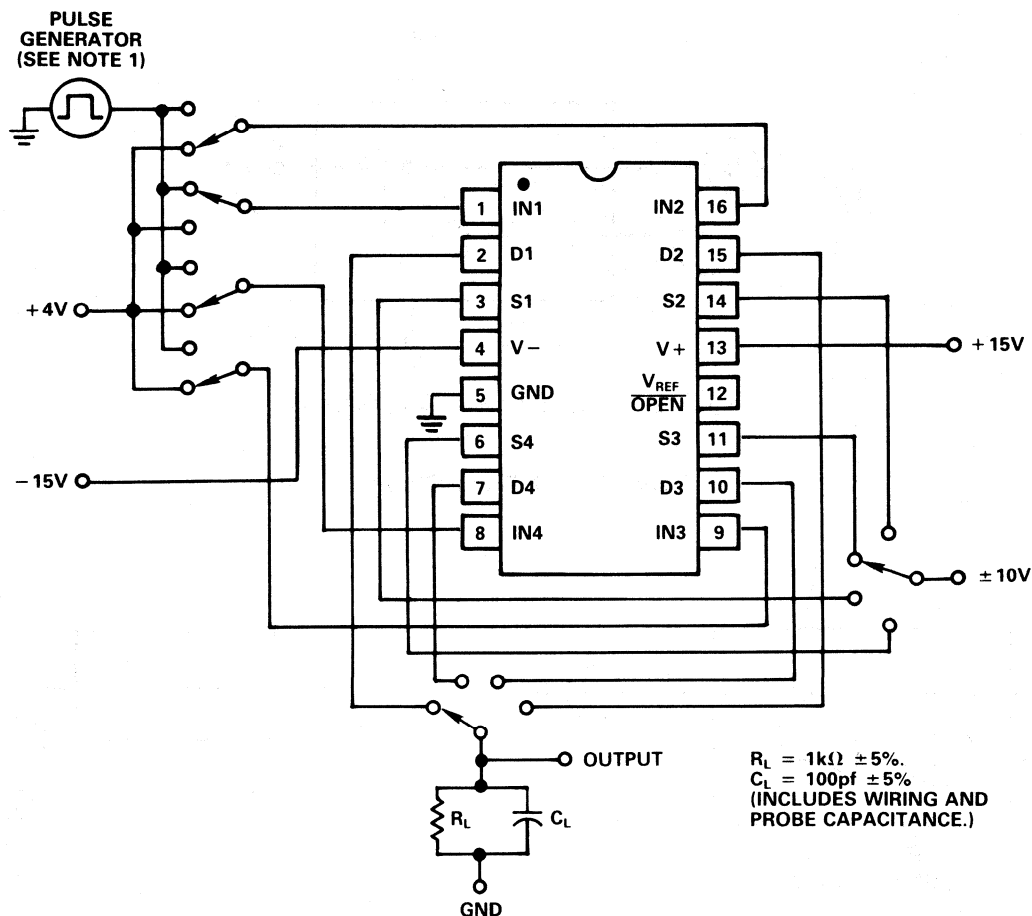


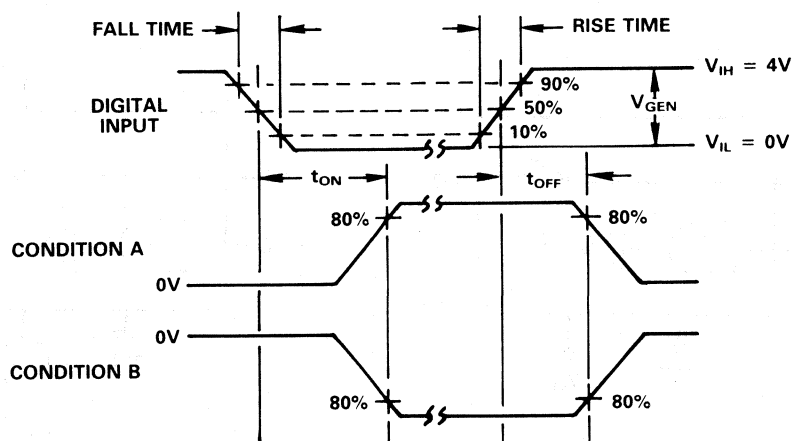
Figure 6. $\pm I_{CC}$ Test Circuit

ADG201A/ADG202A



NOTE
 1. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
 $V_{GEN} = 4V$, $t_{THL} \leq 20ns$.

Figure 7a. Switching Time Circuits



NOTE
 RISE TIME AND FALL TIME $\leq 20ns$.

Figure 7b. Switching Time Waveforms

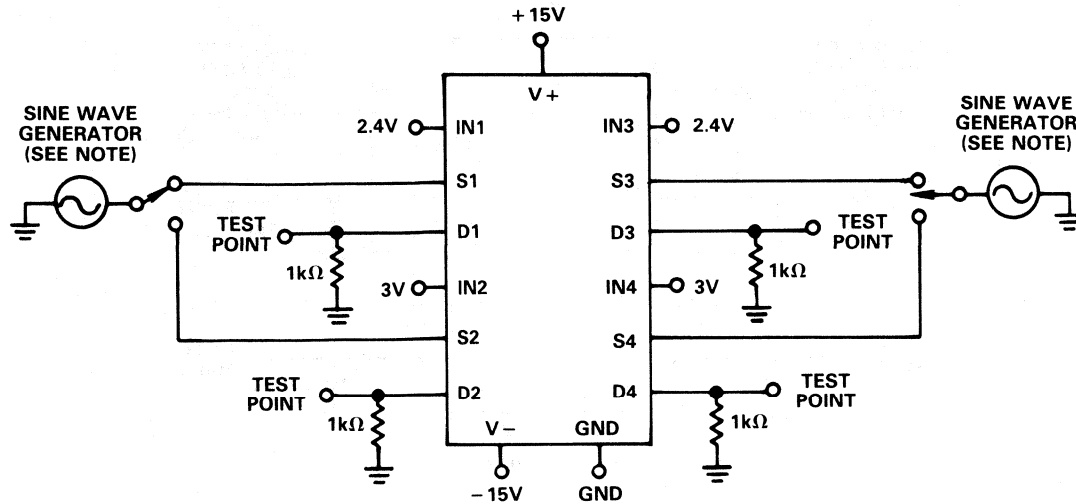


Figure 8. Off Isolation Test Circuits

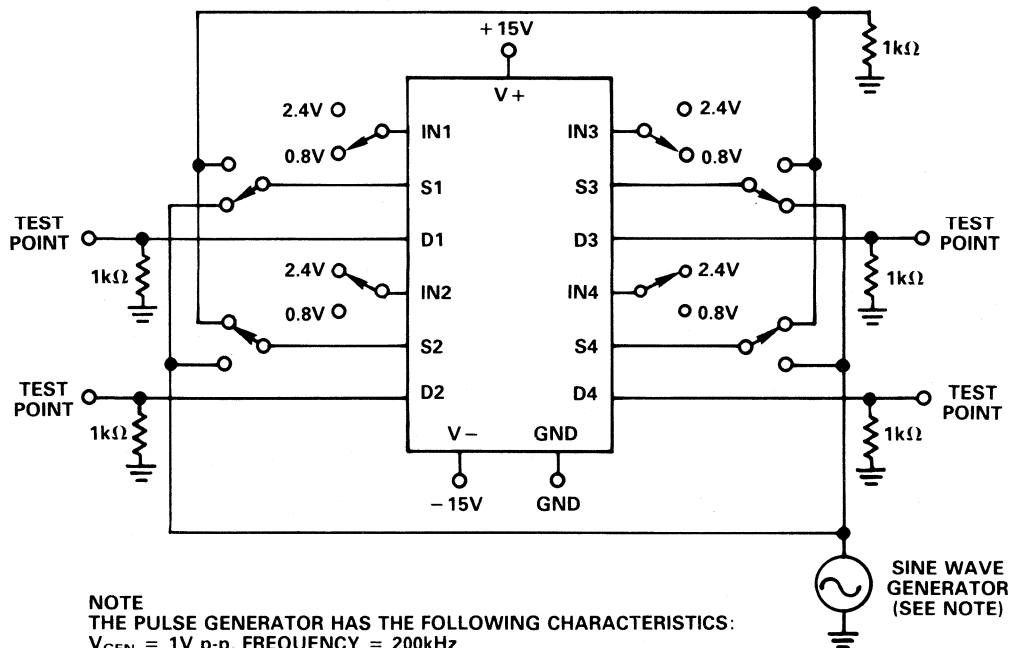
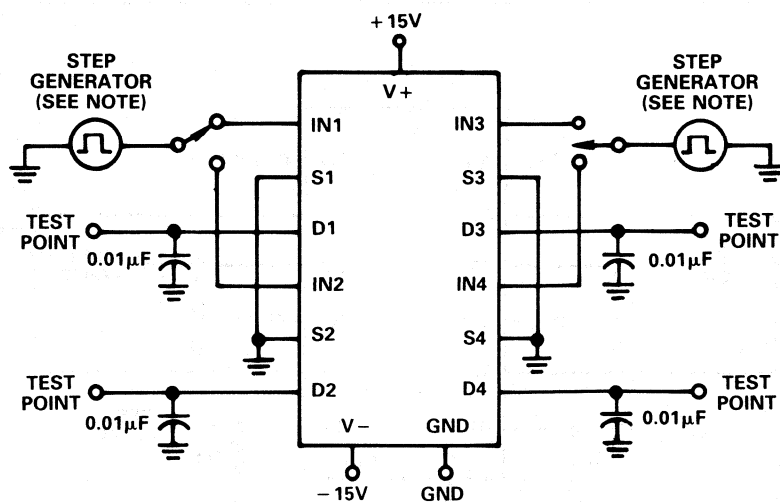


Figure 9. Crosstalk Test Circuit

ADG201A/ADG202A



NOTE
 THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
 $V_{GEN} = 0$ TO $4V$, RISE TIME $\leq 20ns$, FALL TIME $\leq 20ns$, PRR = $200kHz$.

Figure 10. Charge Transfer Error Test Circuits

1.1 Scope.

This specification covers the detail requirements of a monolithic CMOS device consisting of 4 independently selectable SPST switches. It is designed on an enhanced LC²MOS process giving very fast switching speeds and low R_{ON} .

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADG201HST(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44 V
V+ to GND	25 V
V- to GND	-25 V
Analog Inputs	
Voltage at S, D	V+ -2 V to V+ +2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D	20 mA
Pulsed Current S or D	
1 ms Duration, 10% Duty Cycle	70 mA
Digital Inputs	
Voltages at IN	V- -4 V to V+ +4 V or 20 mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	900 mW/°C
Derates above +75°C by	12 mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C
Junction Temperature (T_J)	+175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS analog switches, each consisting of four independent single-pole single-throw switches and latched digital inputs with a WR signal for microprocessor interfacing. They differ only in that the digital control logic is inverted.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
- 1	ADG221T(X)/883B
- 2	ADG222T(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44V
V+ to GND	25V
V- to GND	-25V
Analog Inputs	
Voltage at S, D	V- to V+
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs	
Voltages at IN, WR	V- -2V to V+ +2V or 20mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	900mW/°C
Derates above +75°C by	12mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Junction Temperature (T_J)	+175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

ADG221/ADG222 – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch “ON” Resistance	R_{DS}	-1, 2	145	90	145	$V_{IN}=0.8V$ for -1 Device and 2.4V for -2 Device; $V_D \pm 10V$, $I_S = \mp 1.0mA$ (See Figure 1)	Ω max
		-1, 2	200	200	200	$V_+ = 10V$, $V_- = 10V$; $V_D = \pm 7.5V$; $V_{IN} = 0.8V$ for -1 Device and 2.4V for -2 Device; $I_S = +10.0mA$ (See Figure 1)	Ω max
Source “OFF” Leakage Current	$I_S(OFF)$	-1, 2	100	1	100	$V_D = \pm 14V$, $V_S = \mp 14V$; $V_{IN} = 2.4$ for -1 Device and 0.8V for -2 Device, (See Figure 2)	$\pm nA$ max
Drain “OFF” Leakage Current	$I_D(OFF)$	-1, 2	100	1	100	$V_D = \pm 14V$, $V_S = \mp 14V$; $V_{IN} = 2.4$ for -1 Device and 0.8V for -2 Device, (See Figure 3)	$\pm nA$ max
Channel “ON” Leakage Current	$I_D(ON)$	-1, 2	200	1	200	$V_D = \pm 14V$, All Other Digital Inputs = 0.8V for -1 Device and 2.4V for -2 Device (See Figure 4)	$\pm nA$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1.0	0.5	1.0	$V_{IN} = 15V$; All Other Digital Inputs = 0.8V (See Figure 5)	$\pm \mu A$ max
Low Level Input Current	I_{INL}	-1, 2	1.0	0.5	1.0	$V_{IN} = 0.8V$; All Other Digital Inputs = 2.4V (See Figure 5)	$\pm \mu A$ max
Supply Current	$+I_{CC}$	-1, 2	2.0	1.5	2.0	$V_{IN} = 0V$ or 5V For All Digital Inputs $S1 \dots S4 = D1 \dots D4 =$ Open Circuit (See Figure 6)	mA max
	$-I_{CC}$	-1, 2	2.0	1.5	2.0	$V_{IN} = 0V$ or 5.0V For All Digital Inputs $S1 \dots S4 = D1 \dots D4 =$ Open Circuit (See Figure 6)	mA max
Subgroup 9: $T_A = +25^\circ C$							
Write Pulse Width	t_{WR}	-1, 2	100			(See Paragraph 5.0)	ns min
Digital Input Setup Time	t_{DS}	-1, 2	100			(See Paragraph 5.0)	ns min
Digital Input Hold Time	t_{HS}	-1, 2	20			(See Paragraph 5.0)	ns min
Turn “ON” Time	$t_{(ON)}$	-1, 2	600			$C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
Turn “OFF” Time	$t_{(OFF)}$	-1, 2	500			$C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
Subgroup 10: $T_A = +125^\circ C$							
Write Pulse Width	t_{WR}	-1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Setup Time	t_{DS}	-1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Hold Time	t_{HS}	-1, 2	20			(See Paragraph 5.0)	ns min
Turn “ON” Time	$t_{(ON)}$	-1, 2	800			$C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
Turn “OFF” Time	$t_{(OFF)}$	-1, 2	650			$C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
Subgroup 11: $T_A = -55^\circ C$							
Write Pulse Width	t_{WR}	-1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Setup Time	t_{DS}	-1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Hold Time	t_{HS}	-1, 2	20			(See Paragraph 5.0)	ns min
Turn “ON” Time	$t_{(ON)}$	-1, 2	600			$C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
Turn “OFF” Time	$t_{(OFF)}$	-1, 2	500			$C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns max
Subgroup 12: $T_A = +25^\circ C$							
Off Isolation	V_{ISO}	-1, 2	60			$f = 200kHz$ $V_{GEN} = 1V$ p-p; $R_L = 1k$ (See Figure 8)	dB min
Subgroup 13: $T_A = +25^\circ C$							
Crosstalk between Channels	V_{CT}	-1, 2	60			$f = 200kHz$ $V_{GEN} = 1V$ p-p; $R_L = 1k$ (See Figure 9)	dB min
Subgroup 14: $T_A = +25^\circ C$							
Charge Transfer Error	V_{CTE}	-1, 2	10			(See Figure 10)	$\pm mV$ max
Capacitance: Address	C_A	-1, 2	15			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 0V$	pF max
Capacitance: Input Switch	C_{IS}	-1, 2	15			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 5V$	pF max
Capacitance: Output Switch	C_{DS}	-1, 2	20			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 5V$	pF max

NOTE

¹Unless otherwise noted $V_+ = +15V$; $V_- = -15V$.

Table 1.

REV. A

MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10, 11
Group C End Point Electrical Parameters, Method 5005	1, 10, 11 and Table 3 Delta Limits

*Indicates P.D.A. applies to Subgroup 1.

Table 2. Electrical Test Requirements

Parameters ²	Delta Limits at +25°C ¹ Device Types	
	1	2
R _{DS}	15Ω	15Ω
I _D (ON)	1nA	1nA

NOTES

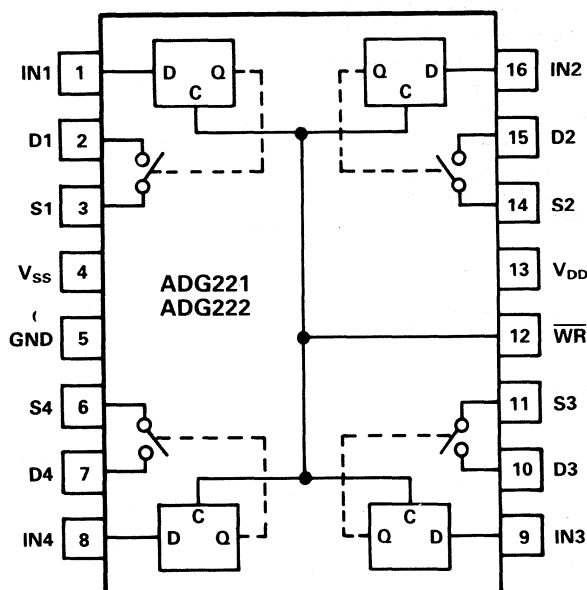
¹Each test applies to every switch in the package.

²Each of the above parameters shall be recorded before and after the required burn-in and life-tests to determine deltas (Δ).

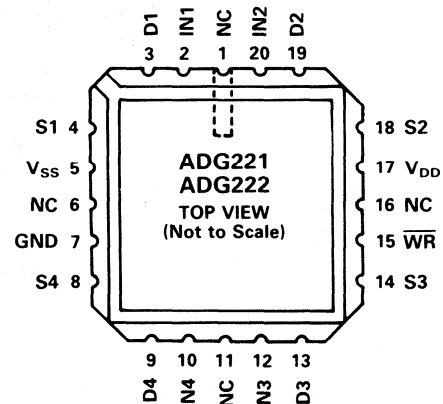
Table 3.

3.2.1 Functional Block Diagram and Terminal Assignments.

Q Package (Cerdip)



E Package (LCC)



3.2.4 Microcircuit Technology Group.

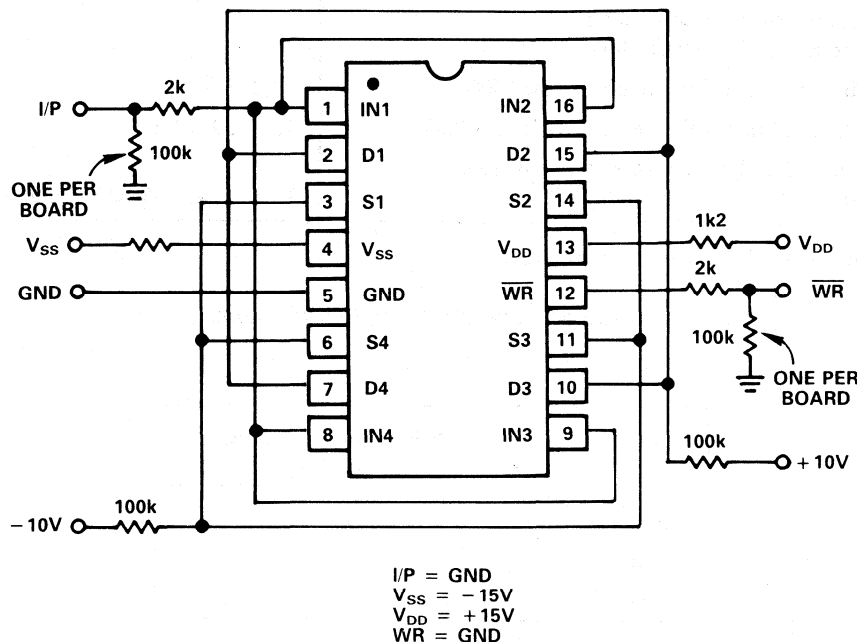
This microcircuit is covered by technology group (82).

REV. A

ADG221/ADG222

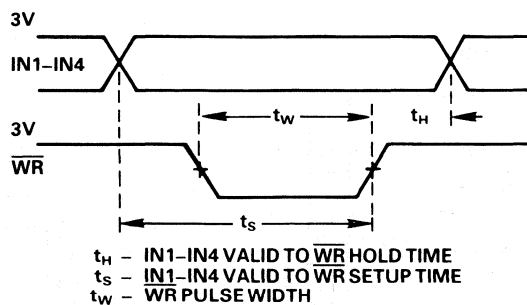
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Timing and Control Sequence

The diagram below shows the timing sequence for latching the switch digital inputs (IN1-IN4). The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.



Timing and Control Sequence

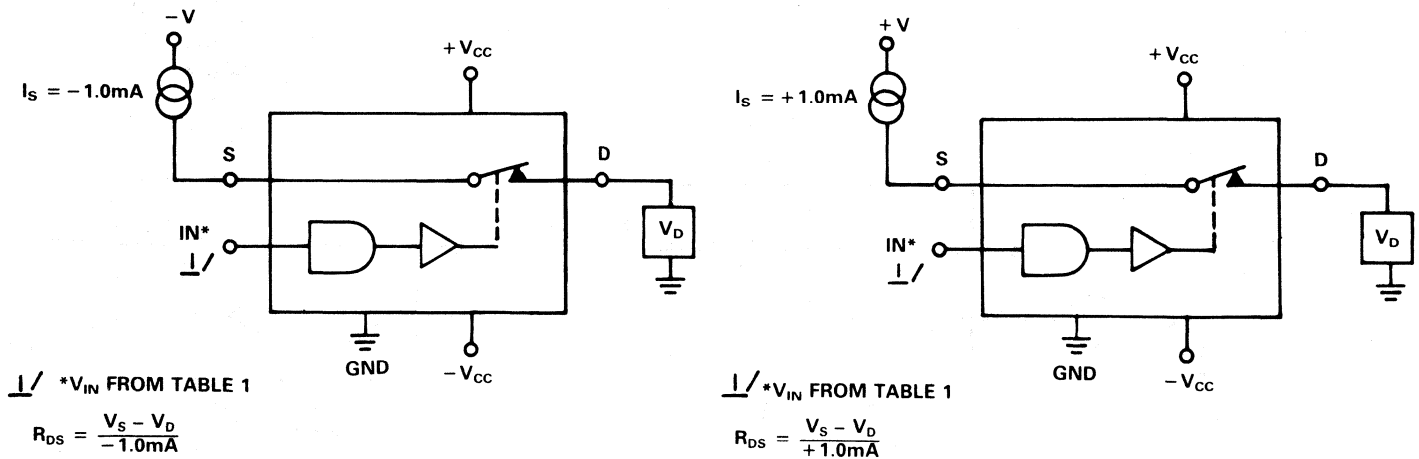
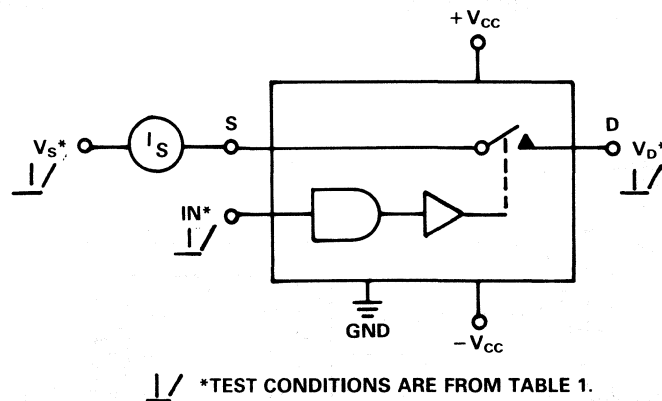
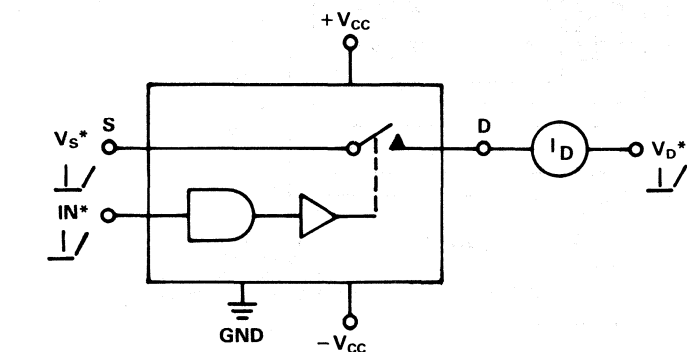


Figure 1. R_{DS} Test Circuits



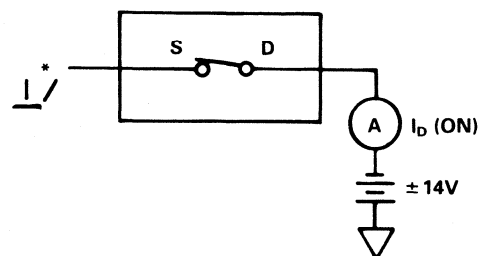
*TEST CONDITIONS ARE FROM TABLE 1.

Figure 2. I_S (OFF) Test Circuit



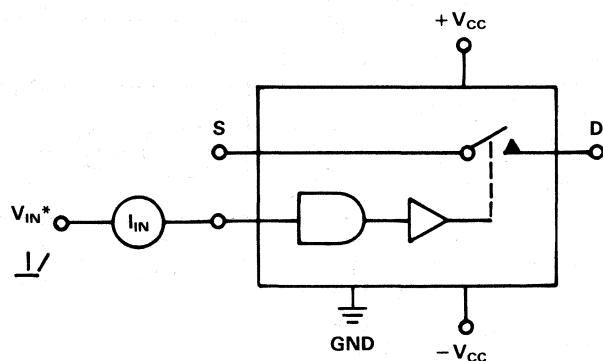
*TEST CONDITIONS ARE FROM TABLE 1.

Figure 3. I_D (OFF) Test Circuit



*CONDITIONS ARE FROM TABLE 1.

Figure 4. I_D (ON) Test Circuit



1/ *CONDITIONS ARE FROM TABLE 1.

Figure 5. I_{INL} , I_{INH} Test Circuit

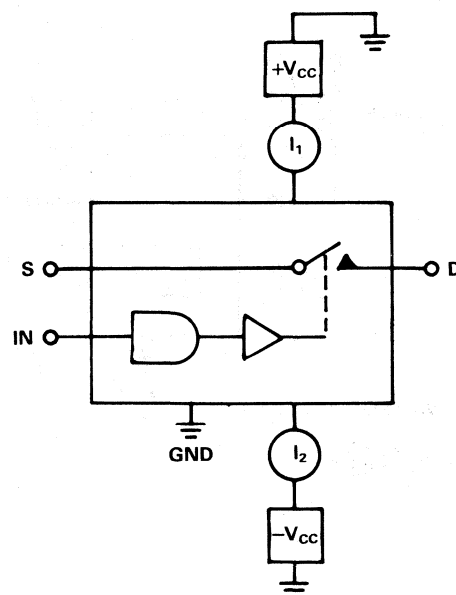
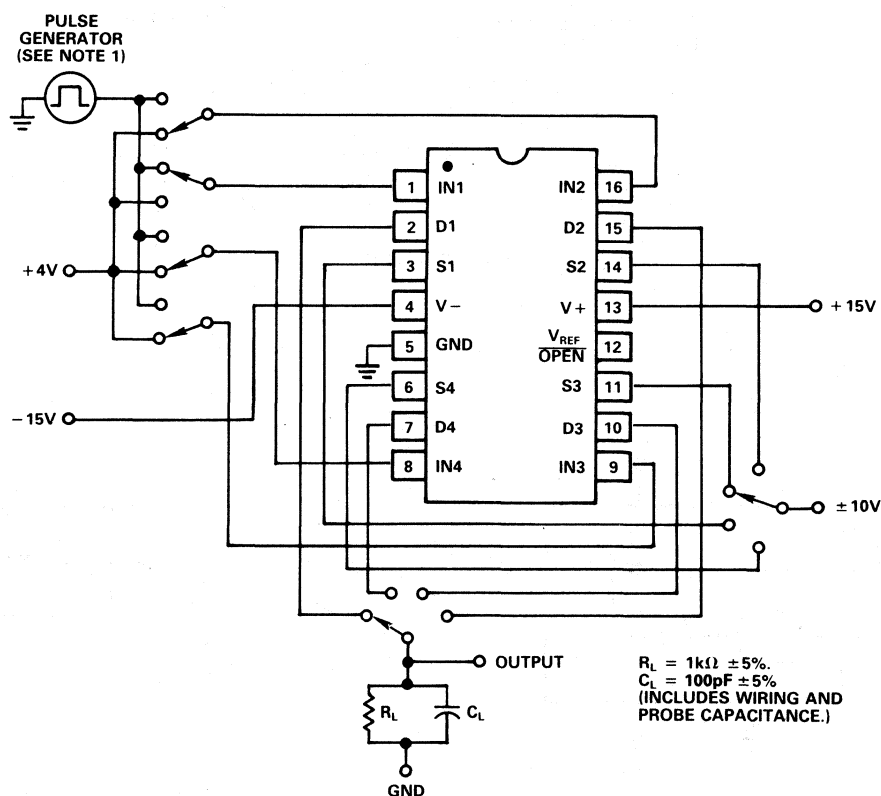


Figure 6. $\pm I_{CC}$ Test Circuit



NOTE
1. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
 $V_{GEN} = 4V$, $t_{THL} \approx 20ns$.

Figure 7a. Switching Time Circuits



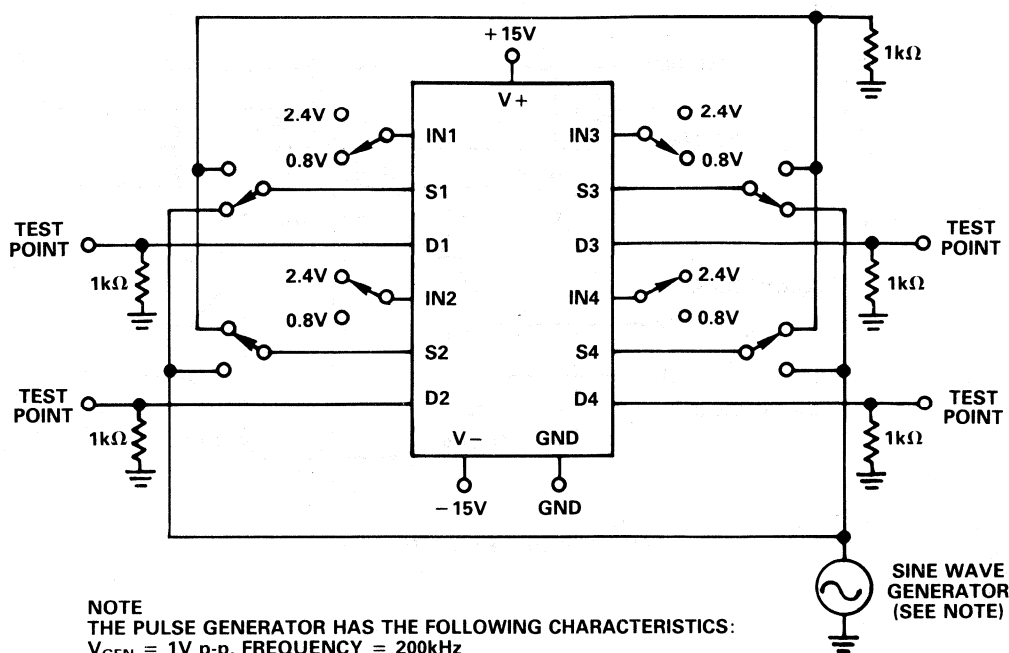


Figure 9. Crosstalk Test Circuit

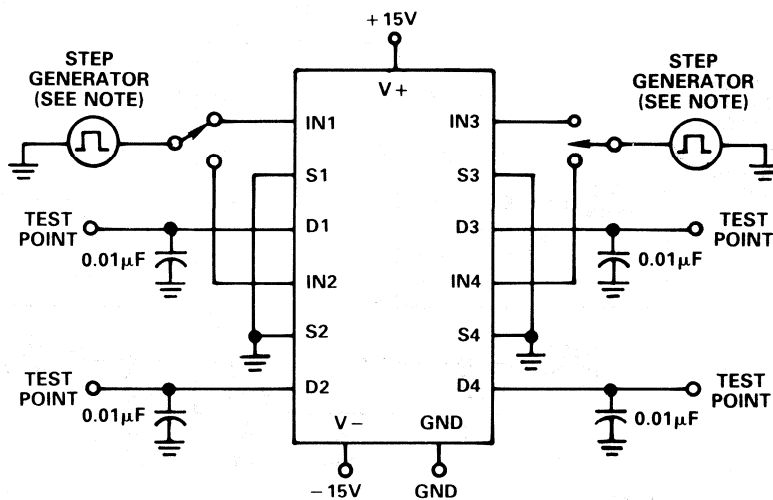


Figure 10. Charge Transfer Error Test Circuits

1.1 Scope.

This specification covers the detail requirements of CMOS monolithic analog multiplexers ADG506A and ADG507A with 16 channels and dual 8 channels, respectively. These multiplexers also feature high switching speeds and low R_{ON} . Break-Before-Make switching is guaranteed.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADG506AT(X)/883B
-2	ADG507AT(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44 V
V+ to GND	25 V
V- to GND	-25 V
Analog Inputs	
Voltage at S, D	V- to V+
Continuous Current, S or D	30 mA
Pulsed Current S or D	
1 ms Duration, 10% Duty Cycle	70 mA
Digital Inputs	
Voltages at IN	V- -4 V to V+ +4 V or 20 mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	470 mW/°C
Derates above +75°C by	6 mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C
Junction Temperature (T_J)	+175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-28 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-28 and E-28A

ADG506A/ADG507A – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch ON Resistance	R_{DS}	-1, 2	400	300	400	$V_D = +10\text{ V}; V_S = -10\text{ V};$ $I_{DS} = 1\text{ mA};$ Test Circuit 1	Ω max
		-1, 2	600	450	600	$V_+ = +10.8\text{ V}; V_- = -10.8\text{ V};$ Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain OFF Leakage Current	I_D (OFF)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$ $V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 3	$\pm\text{nA}$ max
		-2	100	1	100		
Channel ON Leakage Current	I_D (ON)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$ $V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 4	$\pm\text{nA}$ max
		-2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_1 = \pm 10\text{ V}; V_2 = \pm 10\text{ V};$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1	1.5	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
	$-I_{CC}$	-1, 2	0.2	0.1	0.2		
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	400			$V_1 = \pm 10\text{ V}, V_2 = \pm 10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 Turn On Time, ENABLE Turn Off Time, ENABLE	t_{ON} (EN)	-1, 2	400			Test Circuit 7	ns max
	t_{OFF} (EN)	-1, 2	400				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50			$R_L = 1\text{ k}\Omega; C_L = 1\text{ pF};$ Test Circuit 8; $V_{IN} = 20\text{ V pk-pk}, f = 100\text{ kHz};$ $T_A = +25^\circ\text{C}$	dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60			$V_S = 20\text{ V pk-pk}; R_L = 1\text{ k}\Omega;$ $C_L = 12\text{ pF}; T_A = +25^\circ\text{C};$ Test Circuit 9	dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				pF max

NOTE: DUAL SUPPLY OPERATION – $\pm 15\text{ V}$
¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = -15\text{ V}.$

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch ON Resistance	R_{DS}	-1, 2	1000	700	1000	$V_D = +10\text{ V}; V_S = 0\text{ V}; I_{DS} = 0.5\text{ mA}$ $V_+ = +10.8\text{ V}; V_- = 0\text{ V};$ Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain OFF Leakage Current	I_D (OFF)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V}$	$\pm\text{nA}$ max
		-2	100	1	100	$V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V};$ Test Circuit 3	
Channel "ON" Leakage Current	I_D (ON)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$	$\pm\text{nA}$ max
		-2	100	1	100	$V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V}$ Test Circuit 4	
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_+ = +16.5\text{ V}; V_- = 0\text{ V}$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V}$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1.5	1.5	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	600			$V_1 = 10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 Turn On Time, ENABLE	t_{ON} (EN)	-1, 2	600			Test Circuit 7	ns max
Turn Off Time, ENABLE	t_{OFF} (EN)	-1, 2	600				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50				dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60				dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50				pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				pF max

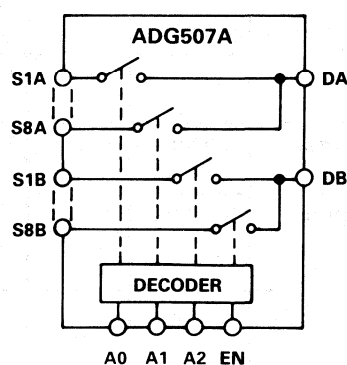
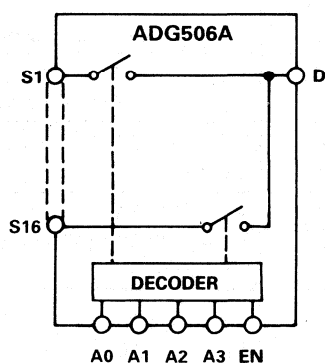
NOTE: SINGLE SUPPLY OPERATION - +15 V

¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = 0\text{ V}.$

Table 2.

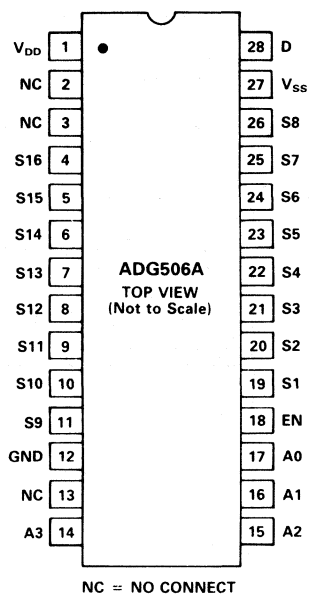
ADG506A/ADG507A

3.2.1 Functional Block Diagram and Terminal Assignments.

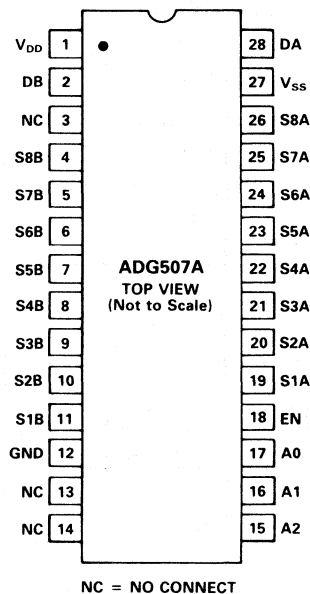


Pin Assignments

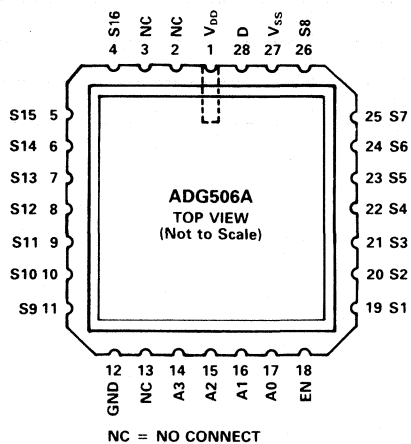
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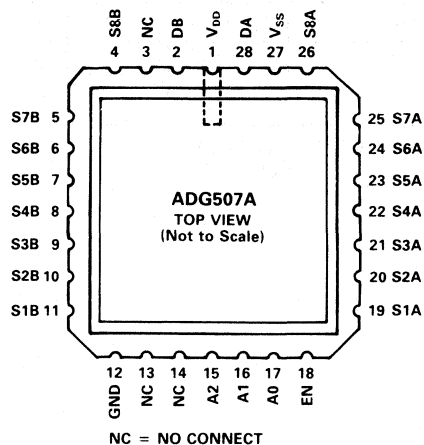
DIP



LCCC



LCCC



MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10**, 11**
Group C End Point Electrical Parameters, Method 5005	1

NOTES

*Indicates PDA applies to Subgroup 1.

**Subgroups 10 & 11, if not tested, shall be guaranteed to the limits in the data sheet.

TRUTH TABLES

A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

X = Don't Care

Table 3. ADG506A Truth Table

A2	A1	A0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table 4. ADG507A Truth Table

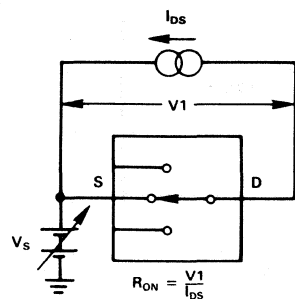
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

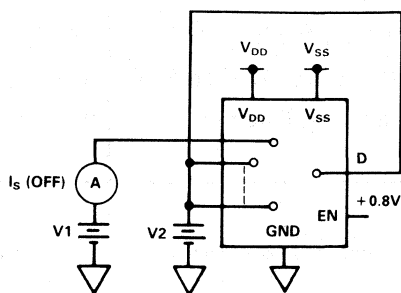
ADG506A/ADG507A

4.2.1 Life Test/Burn-In Circuit.

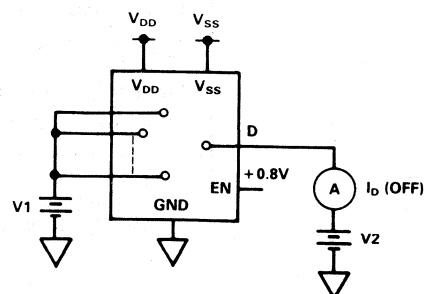
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B). Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.



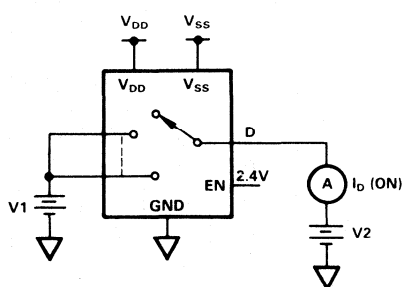
Test Circuit 1
 R_{ON}



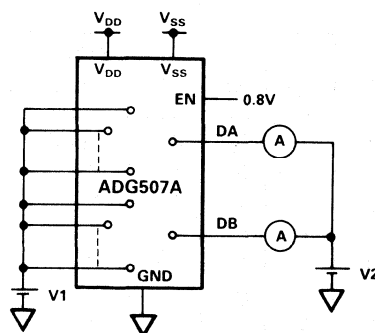
Test Circuit 2
 I_S (OFF)



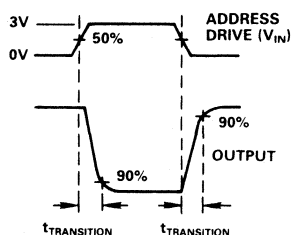
Test Circuit 3
 I_D (OFF)



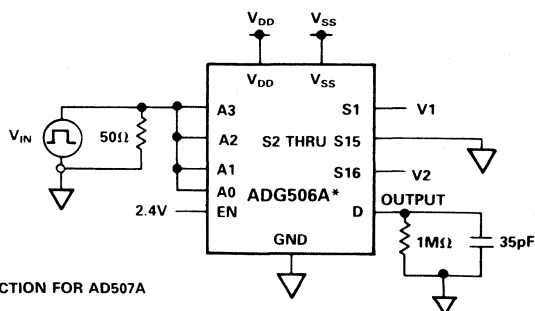
Test Circuit 4
 I_D (ON)



Test Circuit 5
 I_{DIFF}

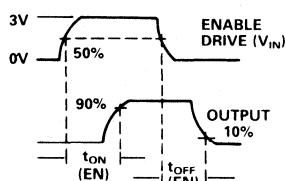


*SIMILAR CONNECTION FOR AD507A

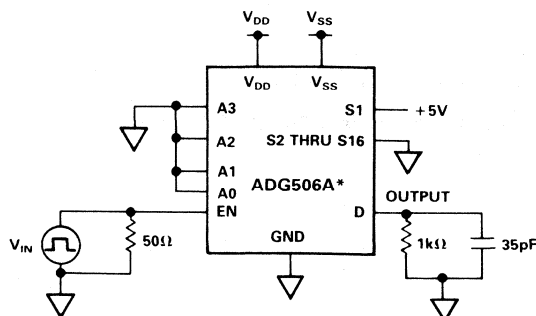


Test Circuit 6

Switching Time of Multiplexer, $t_{TRANSITION}$



*SIMILAR CONNECTION FOR AD507A

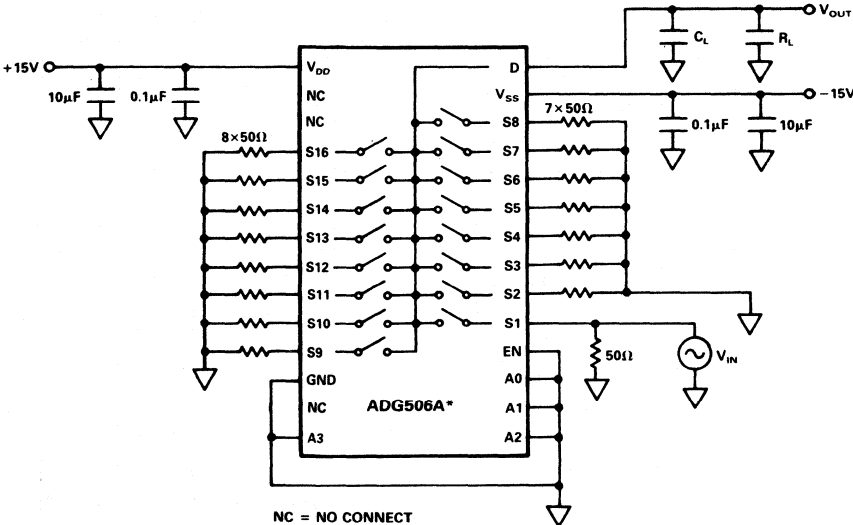


Test Circuit 7

Enable Delay, t_{ON} (EN), t_{OFF} (EN)

REV. A

ADG506A/ADG507A

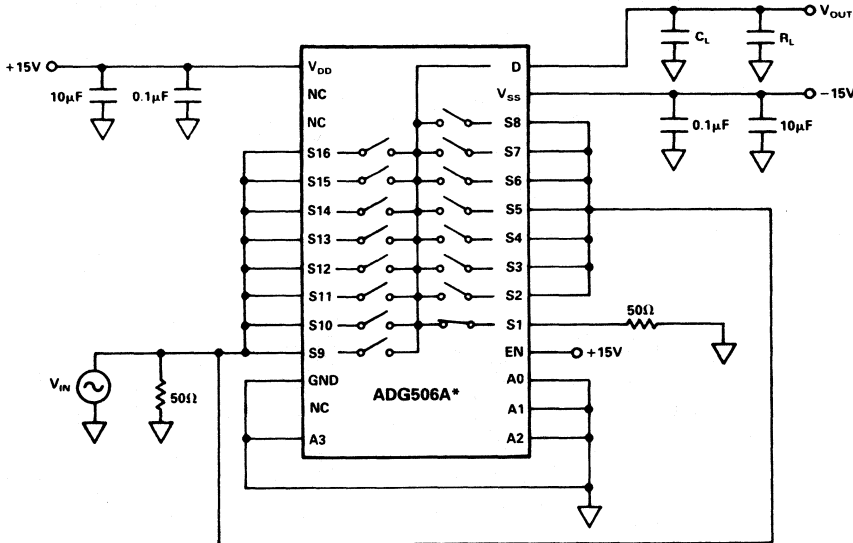


NC = NO CONNECT

ADG506A* OFF ISOLATION TEST CIRCUIT

***SIMILAR TYPE OF CIRCUIT APPLIES FOR ADG507A.**

Test Circuit 8 OFF Isolation



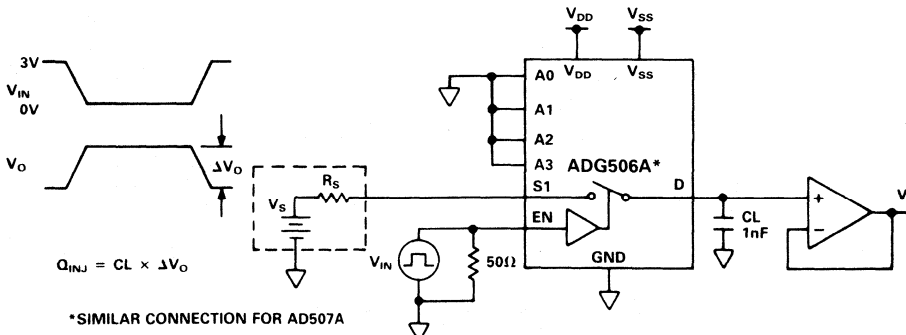
NC = NO CONNECT

ADG506A* CROSSTALK TEST CIRCUIT

***SIMILAR CIRCUIT APPLIES FOR ADG507A**

Test Circuit 9

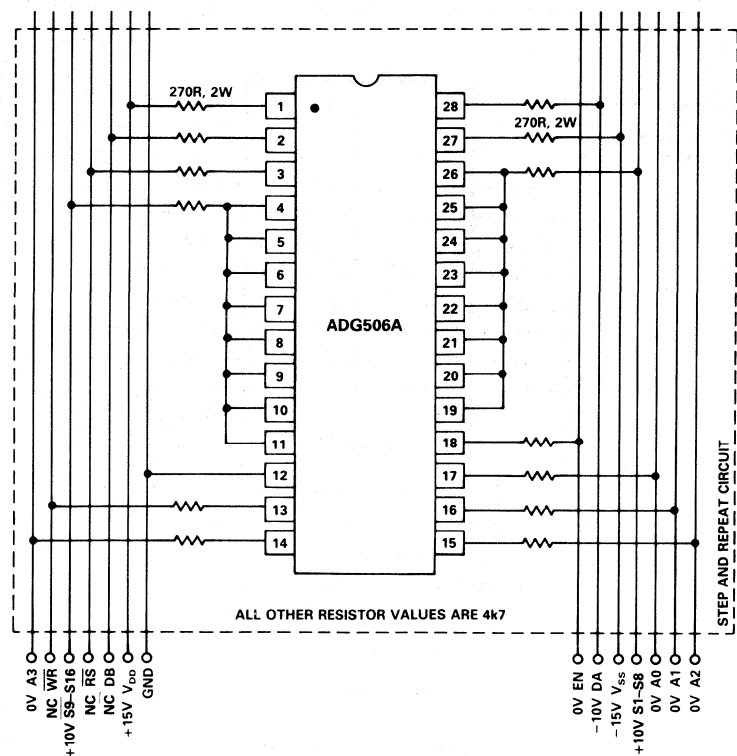
Crosstalk Between Channels



***SIMILAR CONNECTION FOR AD507A**

Test Circuit 10 Charge Injection

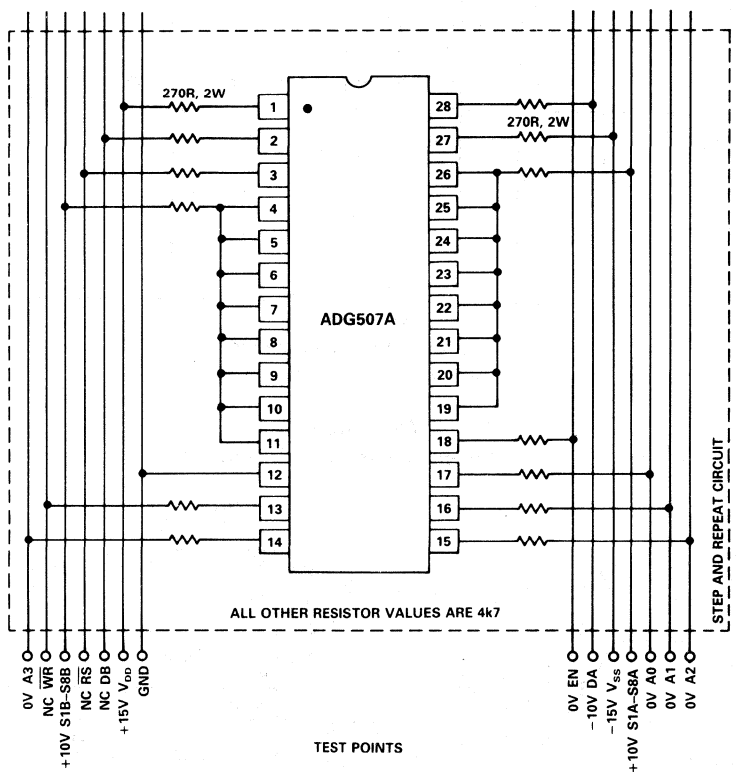
ADG506A/ADG507A



TEST POINTS

NOTES
A0, A1, A2, A3, WR, RS, AND EN EACH HAVE ONE OFF
100k RESISTOR TO GND AT BOARD EDGE.
THE POWER UP SEQUENCE IS AS FOLLOWS: APPLY GND;
A0, A1, A2, A3; EN; VDD; VSS; DA; S1-S16.
NC = NO CONNECT

ADG506A Edge Connections



TEST POINTS

NOTES
A0, A1, A2, A3, WR, RS, AND EN EACH HAVE ONE OFF
100k RESISTOR TO GND AT BOARD EDGE.
THE POWER UP SEQUENCE IS AS FOLLOWS: APPLY GND;
A0, A1, A2, EN; VDD; VSS; DA, DB; S1A-S8A, S1B-S8B.

ADG507A Edge Connections

1.1 Scope.

This specification covers the detail requirements of CMOS monolithic analog multiplexers ADG508A and ADG509A with 8 channels and dual 4 channels, respectively. These multiplexers also feature high switching speeds and low R_{ON} . Break-Before-Make switching is guaranteed.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADG508AT(X)/883B
-2	ADG509AT(X)/883B

NOTE

¹To complete the part number substitute the package identified as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44 V
V+ to GND	25 V
V- to GND	-25 V
Analog Inputs	
Voltage at S, D	V- to V+
Continuous Current, S or D	30 mA
Pulsed Current S or D	
1 ms Duration, 10% Duty Cycle	70 mA
Digital Inputs	
Voltages at IN	V- -4 V to V+ +4 V or 20 mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	470 mW/°C
Derates above +75°C by	6 mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C
Junction Temperature (T_J)	+175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

ADG508A/ADG509A – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch “ON” Resistance	R_{DS}	-1, 2	400	300	400	$V_S = +10\text{ V}; V_S = -10\text{ V};$ $I_{DS} = 1\text{ mA};$ Test Circuit 1	Ω max
		-1, 2	600	450	600	$V+ = +10.8\text{ V}; V- = -10.8\text{ V};$ Test Circuit 1	
Source “OFF” Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V+ = +16.5\text{ V}; V- = -16.5\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain “OFF” Leakage Current	I_D (OFF)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$ $V+ = +16.5\text{ V}; V- = -16.5\text{ V};$ Test Circuit 3	$\pm\text{nA}$ max
		-2	100	1	100		
Channel “ON” Leakage Current	I_D (ON)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$ $V+ = +16.5\text{ V}; V- = -16.5\text{ V};$ Test Circuit 4	$\pm\text{nA}$ max
		-2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V1 = \pm 10\text{ V}; V2 = \pm 10\text{ V};$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V+ = +16.5\text{ V}; V- = -16.5\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V+ = +16.5\text{ V}; V- = -16.5\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1.5	1.5	$V+ = +16.5\text{ V}; V- = -16.5\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
	$-I_{CC}$	-1, 2	0.2	0.2	0.2		
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	400			$V1 = \pm 10\text{ V}, V2 = \pm 10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 Turn ON Time, ENABLE	$t_{ON}(\text{EN})$	-1, 2	400			Test Circuit 7	ns max
Turn OFF Time, ENABLE	$t_{OFF}(\text{EN})$	-1, 2	400				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50			$R_L = 1\text{ k}\Omega; C_L = 1\text{ pF};$ $V_{IN} = 20\text{ V pk-pk}, f = 100\text{ kHz};$ $T_A = +25^\circ\text{C};$ Test Circuit 8	dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60			$V_S = 20\text{ V pk-pk}; R_L = 1\text{ k}\Omega;$ $C_L = 12\text{ pF}; T_A = +25^\circ\text{C};$ Test Circuit 9	dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				pF max

NOTE: DUAL SUPPLY OPERATION – $\pm 15\text{ V}$

¹Unless otherwise noted $V+ = +15\text{ V}; V- = -15\text{ V}.$

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch "ON" Resistance	R_{DS}	-1, 2	1000	700	1000	$V_D = +10\text{ V}; V_S = 0\text{ V}; I_{DS} = 0.5\text{ mA}$ $V_+ = +10.8\text{ V}; V_- = 0\text{ V};$ Test Circuit 1	Ω max
Source "OFF" Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain "OFF" Leakage Current	I_D (OFF)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V}$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V};$ Test Circuit 3	$\pm\text{nA}$ max
		-2	100	1	100		
Channel "ON" Leakage Current	I_D (ON)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V}$ Test Circuit 4	$\pm\text{nA}$ max
		2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_+ = +16.5\text{ V}; V_- = 0\text{ V}$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V}$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1.5	1.5	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	600			$V_1 = 10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 Turn ON Time, ENABLE	t_{ON} (EN)	-1, 2	600			Test Circuit 7	ns max
Turn OFF Time, ENABLE	t_{OFF} (EN)	-1, 2	600				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50				dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60				dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50				pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				pF max

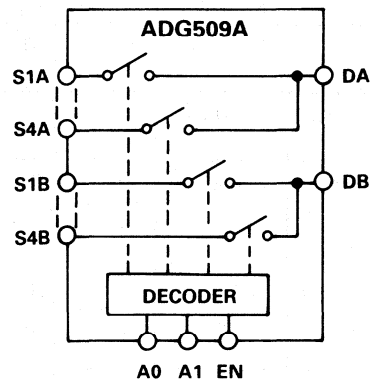
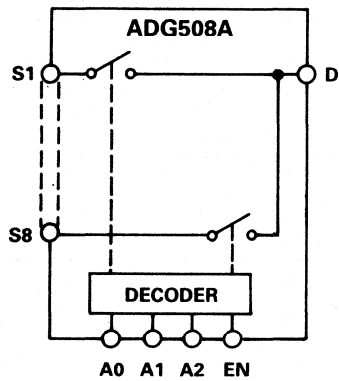
NOTE: SINGLE SUPPLY OPERATION – +15 V

¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = 0\text{ V}$.

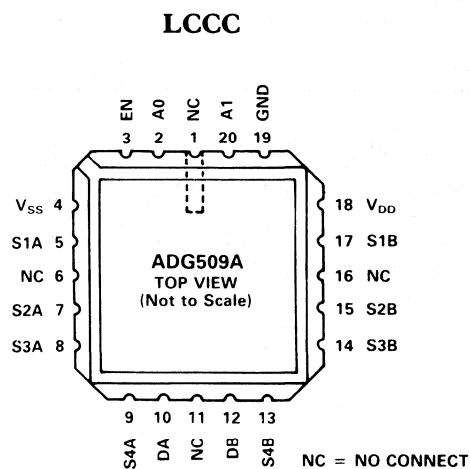
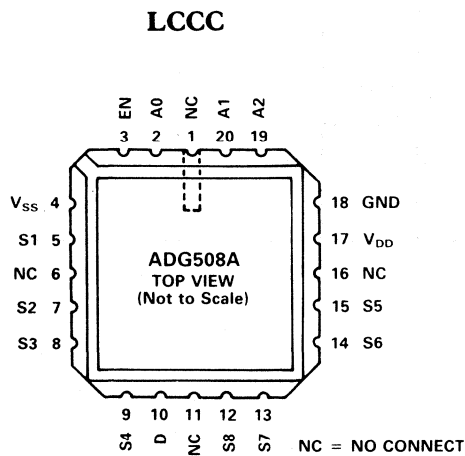
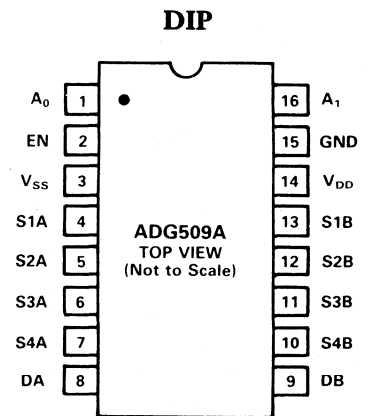
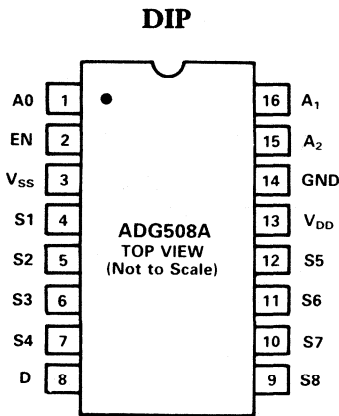
Table 2.

ADG508A/ADG509A

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments



MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10**, 11**
Group C End Point Electrical Parameters, Method 5005	1

NOTES

*Indicates P.D.A. applies to Subgroup 1.

**Subgroups 10 & 11, if not tested, shall be guaranteed to the limits in the data sheet.

TRUTH TABLES

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table 3. ADG508A Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

Table 4. ADG509A Truth Table

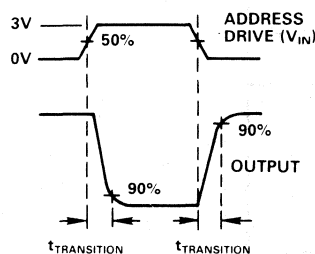
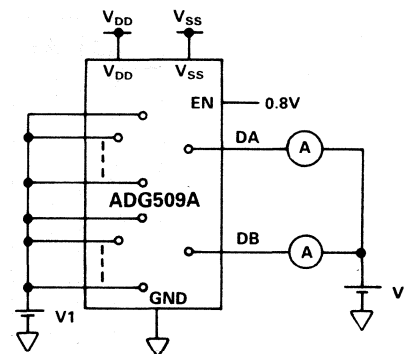
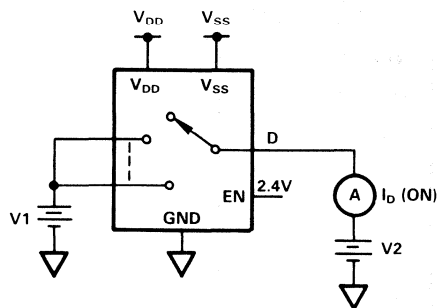
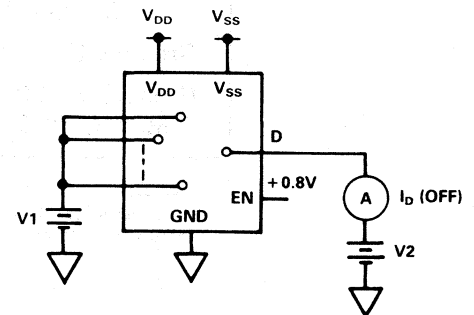
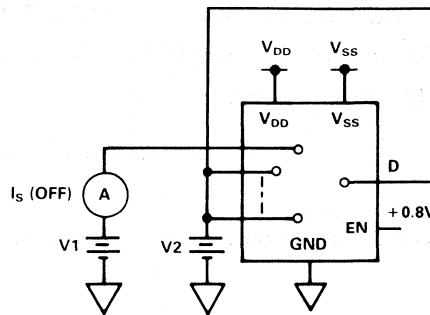
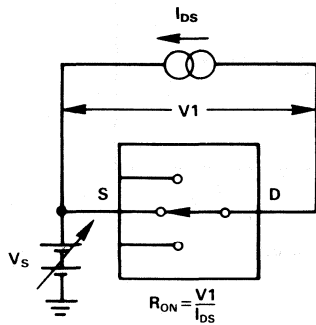
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

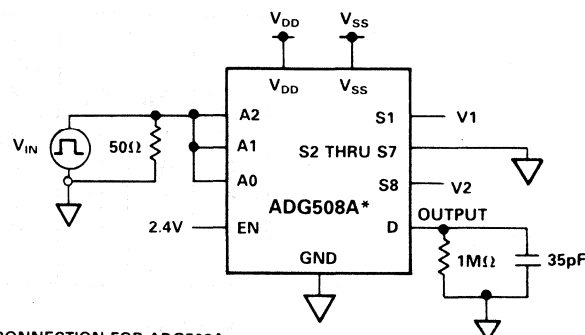
ADG508A/ADG509A

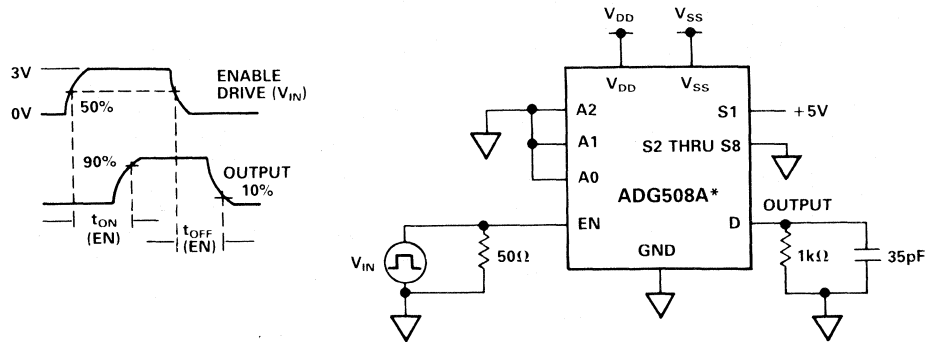
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B). Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.



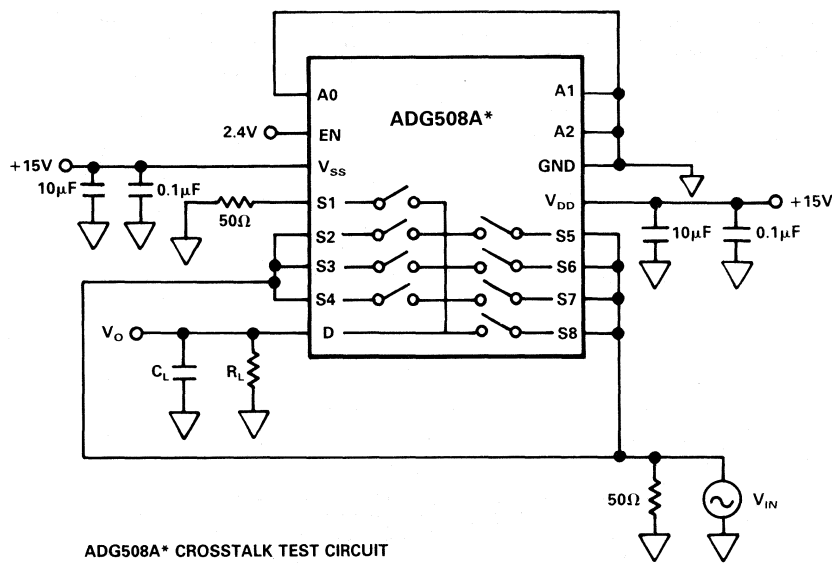
*SIMILAR CONNECTION FOR ADG509A





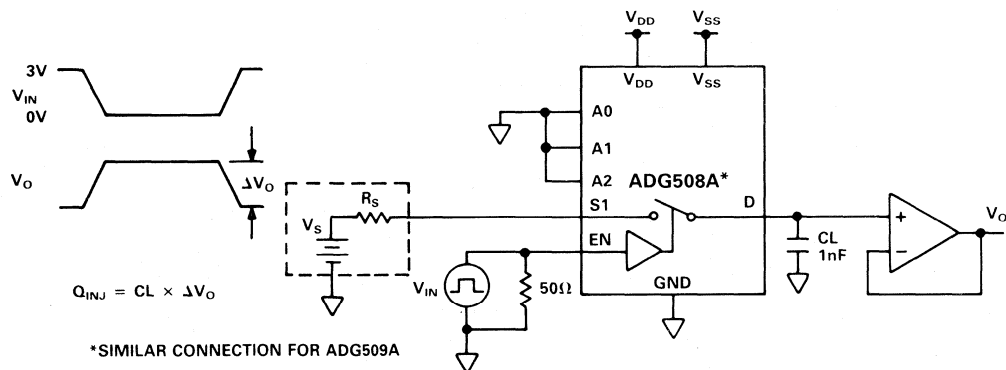
*SIMILAR CONNECTION FOR ADG509A

Test Circuit 7
Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$



ADG508A* CROSSTALK TEST CIRCUIT
*SIMILAR CIRCUIT APPLIES FOR ADG509A

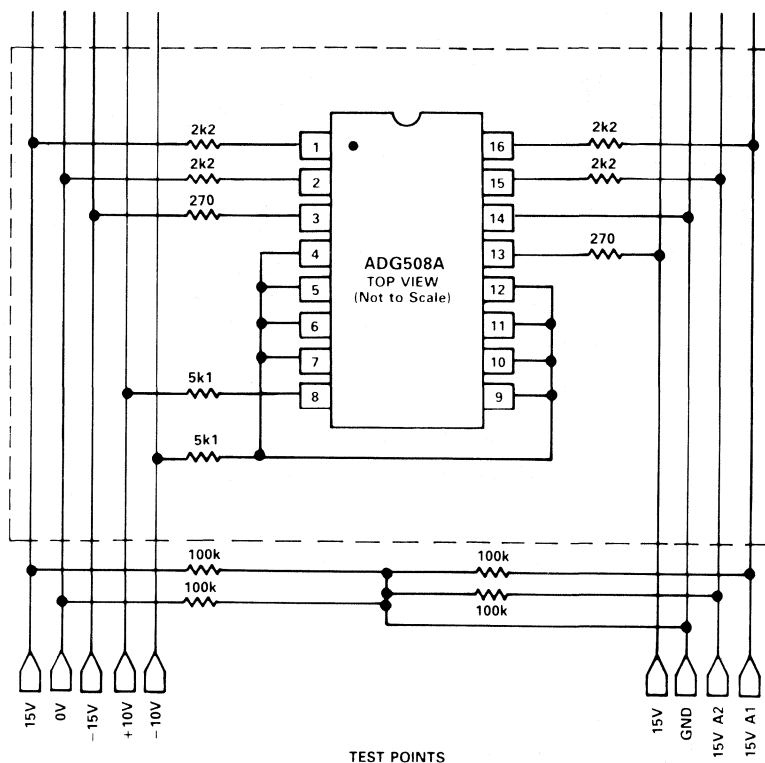
Test Circuit 8
Crosstalk Between Channels



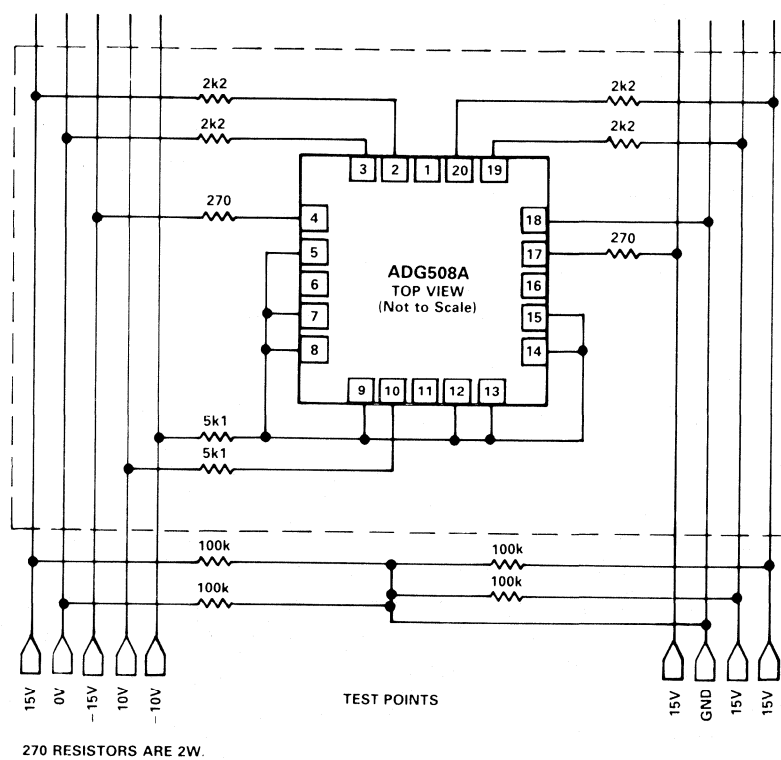
*SIMILAR CONNECTION FOR ADG509A

Test Circuit 9
Charge Injection

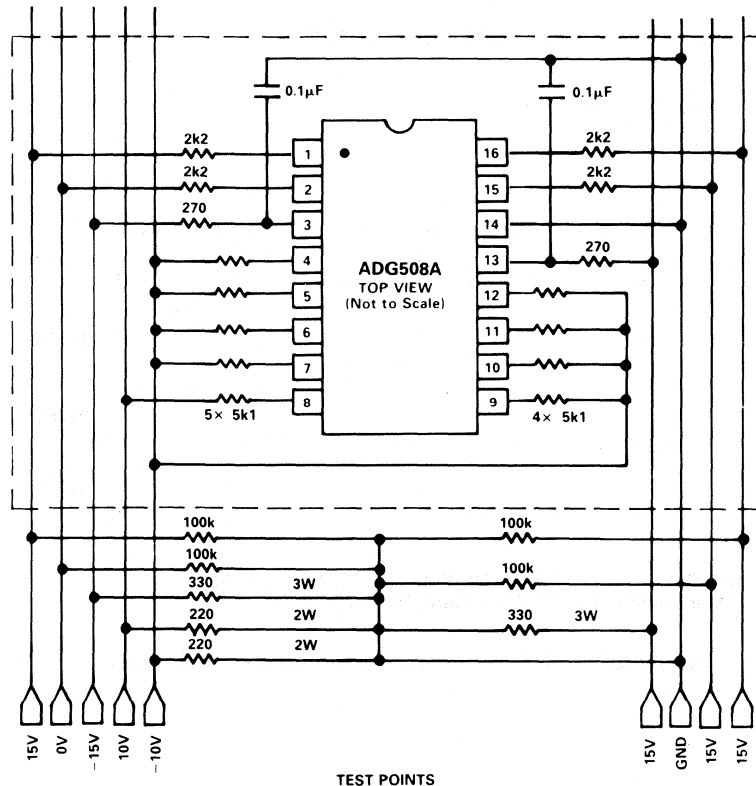
ADG508A/ADG509A



ADG508A (Q) Package Static Burn-In (for Boards Built Before August 1, 1989)

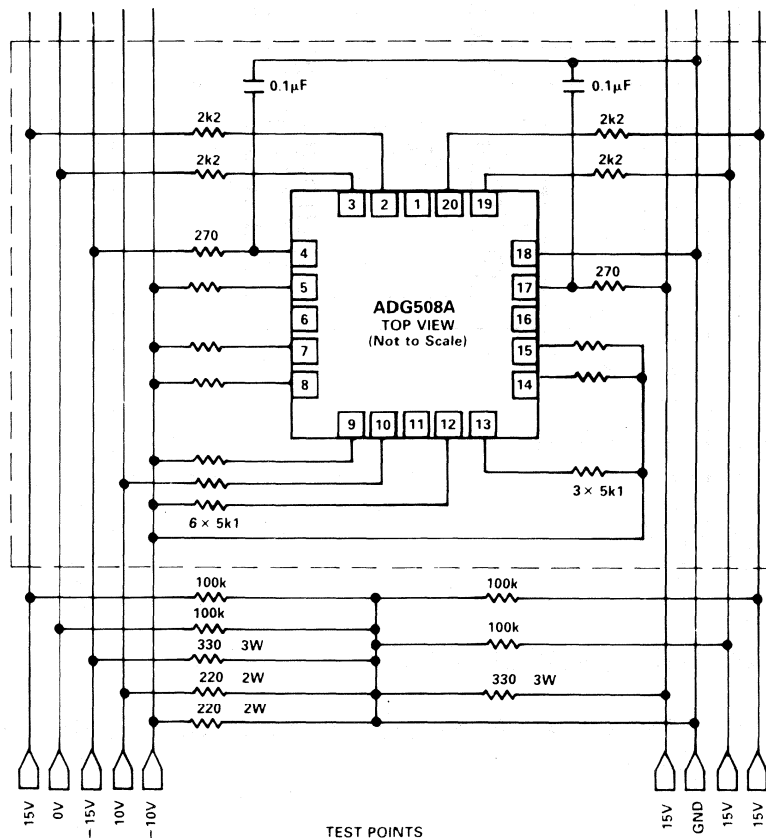


ADG508A (E) Package Static Burn-In (for Boards Built Before August 1, 1989)



ALL 270 OHM RESISTORS ARE 1.5W.

ADG508A (Q) Package Static Burn-In (for Boards Built After July 31, 1989)



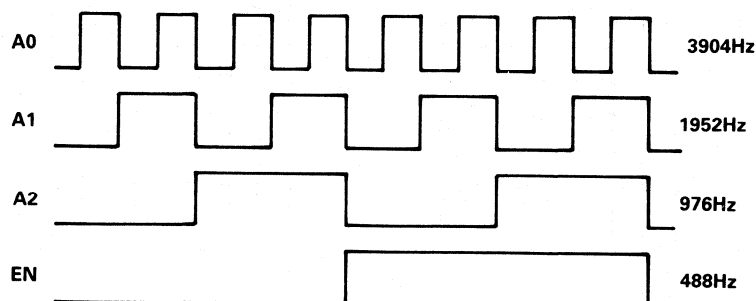
ALL 270 OHM RESISTORS ARE 1.5W.

ADG508A (E) Package Static Burn-In (for Boards Built After July 31, 1989)

ADG508A/ADG509A

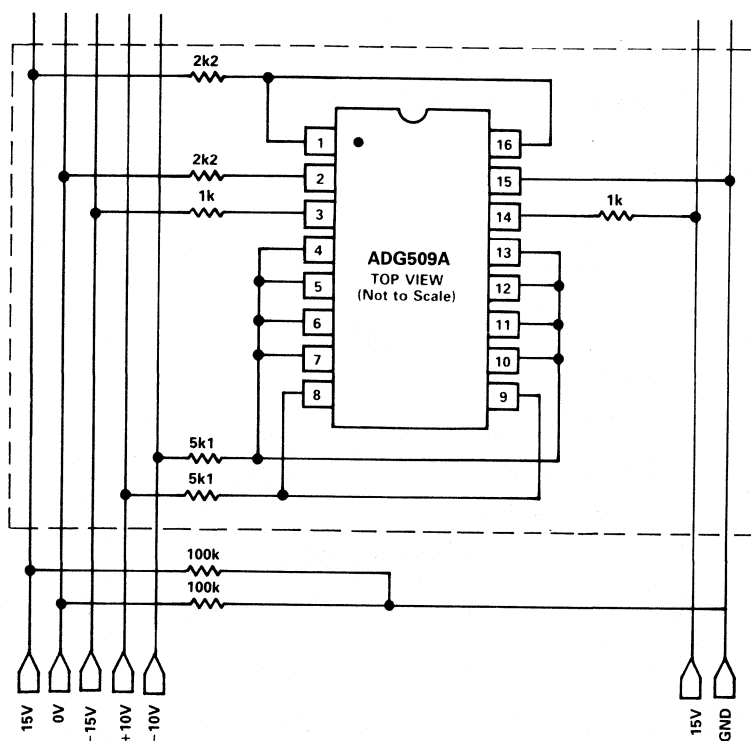
APPLY VOLTAGES IN FOLLOWING SEQUENCE:

- 1 V_{DD} +15V
- 2 V_{SS} -15V
- 3 D 0V
- 4 $S1-S8$ 0V
- 5 V_{DATA} +15V



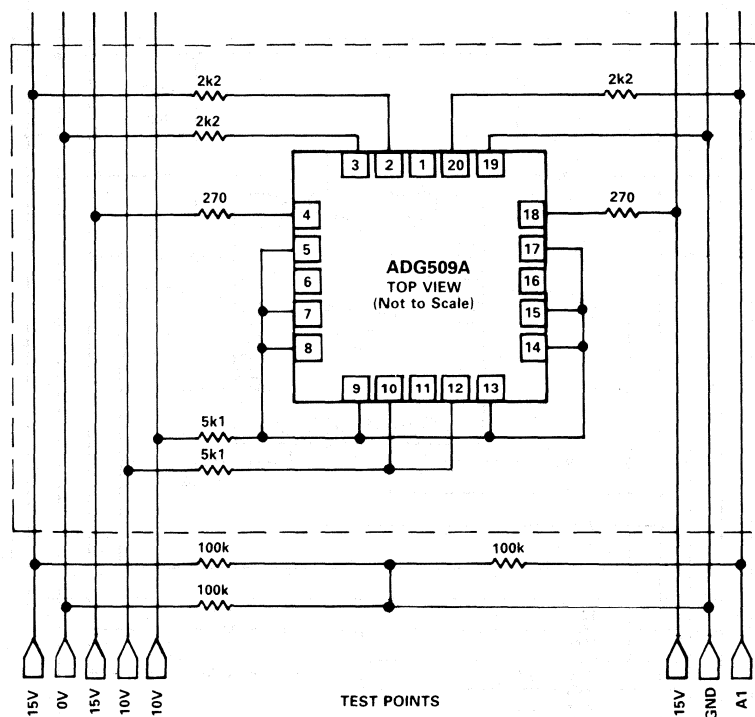
ABOVE VOLTAGES APPLY TO DYNAMIC BURN-IN ONLY.
WAVEFORMS ARE TO BE APPLIED CONTINUOUSLY.

ADG508A (Q & E Packages) Dynamic Burn-In Conditions



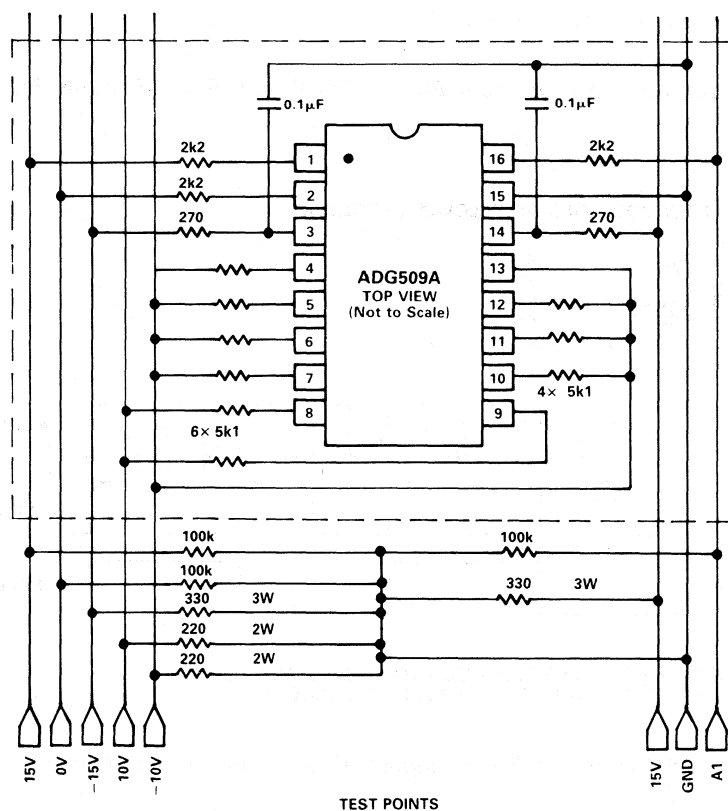
THIS CIRCUIT USES PINS 2 TO 17 OF ADG529A BOARDS
WHICH WERE BUILT BEFORE AUGUST 1989.

ADG509A (Q) Package Static Burn-In (for Boards Built Before August 1, 1989)



270 RESISTORS ARE 2W.

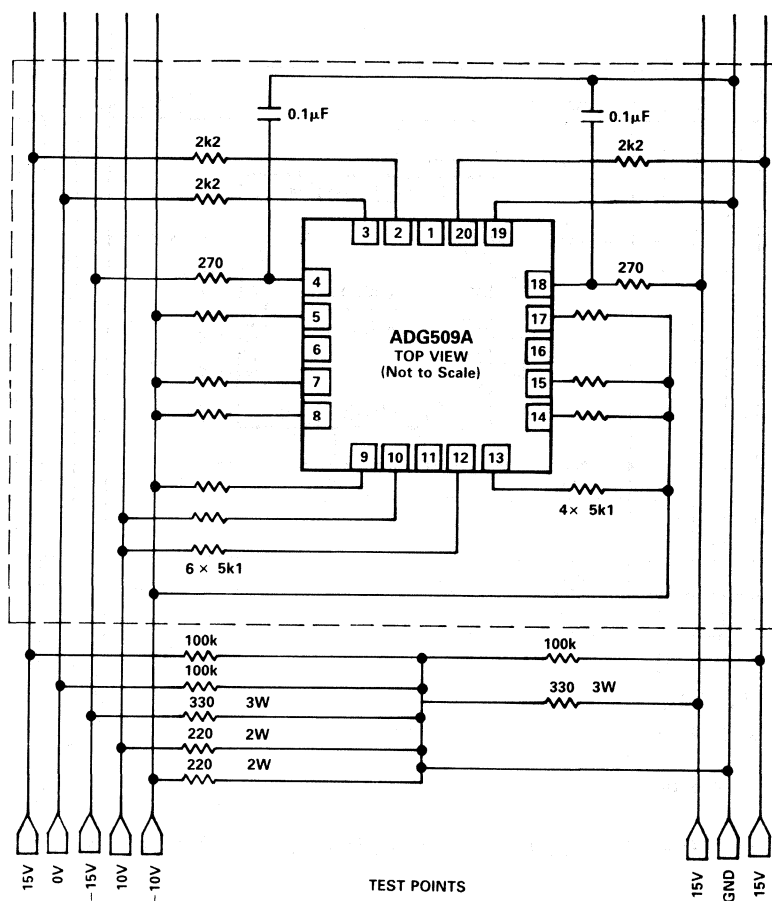
ADG509A (E) Package Static Burn-In (for Boards Built Before August 1, 1989)



ALL 270 OHM RESISTORS ARE 1.5W.

ADG509A (Q) Package Static Burn-In (for Boards Built After July 31, 1989)

ADG508A/ADG509A

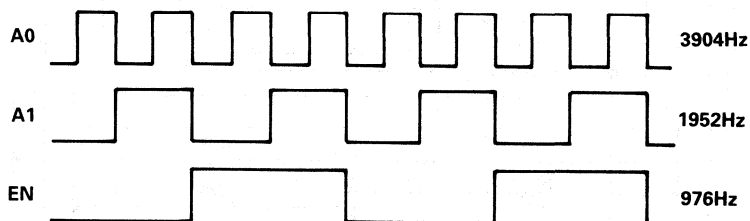


ALL 270 OHM RESISTORS ARE 1.5W.

ADG509A (E) Package Static Burn-In (for Boards Built After July 31, 1989)

APPLY VOLTAGES IN FOLLOWING SEQUENCE:

- 1 V_{DD} +15V
- 2 V_{SS} -15V
- 3 DA-DB 0V
- 4 S1-S4 0V
- 5 CLOCK LINES AS FOLLOWS:



ABOVE VOLTAGES APPLY TO DYNAMIC BURN-IN ONLY.
WAVEFORMS ARE TO BE APPLIED CONTINUOUSLY.

ADG509A (Q & E Packages) Dynamic Burn-In Conditions

1.1 Scope.

This specification covers the detail requirements of CMOS monolithic analog multiplexers ADG526A and ADG527A with 16 channels and dual 8 channels, respectively. These multiplexers also feature high switching speeds, low R_{ON} and on-chip latches to facilitate microprocessor interfacing. Break-Before-Make switching is guaranteed.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADG526AT(X)/883B
-2	ADG527AT(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44 V
V+ to GND	25 V
V- to GND	-25 V
Analog Inputs	
Voltage at S, D	V- to V+
Continuous Current, S or D	30 mA
Pulsed Current S or D	
1 ms Duration, 10% Duty Cycle	70 mA
Digital Inputs	
Voltages at IN	V- -4 V to V+ +4 V or 20 mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	470 mW/°C
Derates above +75°C by	6 mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C
Junction Temperature (T_J)	+175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-28 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-28 and E-28A

ADG526A/ADG527A – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch ON Resistance	R_{DS}	-1, 2	400	300	400	$V_D = +10\text{ V}; V_S = -10\text{ V};$ $I_{DS} = 1\text{ mA};$ Test Circuit 1	Ω max
		-1, 2	600	450	600	$V_+ = +10.8\text{ V}; V_- = -10.8\text{ V};$ Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain OFF Leakage Current	I_D (OFF)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$	$\pm\text{nA}$ max
		-2	100	1	100	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 3	
Channel ON Leakage Current	I_D (ON)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$	$\pm\text{nA}$ max
		-2	100	1	100	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 4	
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_1 = \pm 10\text{ V}; V_2 = \pm 10\text{ V};$ Test Circuit 5	nA max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1	1.5	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
	$-I_{CC}$	-1, 2	0.2	0.1	0.2		
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	400			$V_1 = \pm 10\text{ V}; V_2 = \pm 10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 $t_{ON}(\text{ENABLE}, \overline{\text{WRITE}})$	$t_{ON}(\text{EN}, \overline{\text{WR}})$	-1, 2	400			Test Circuit 7a, 7b, 7c	ns max
$t_{OFF}(\text{ENABLE}, \overline{\text{RESET}})$	$t_{OFF}(\text{EN}, \overline{\text{RS}})$	-1, 2	400				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50			$R_L = 1\text{ k}\Omega; C_L = 12\text{ pF};$ $V_{IN} = 20\text{ V pk-pk}, f = 100\text{ kHz};$ $T_A = +25^\circ\text{C};$ Test Circuit 8	dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60			$V_S = 20\text{ V pk-pk}; R_L = 1\text{ k}\Omega;$ $C_L = 12\text{ pF}; T_A = +25^\circ\text{C};$ Test Circuit 9	dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				

NOTE: DUAL SUPPLY OPERATION – $\pm 15\text{ V}$

¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = -15\text{ V}.$

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch ON Resistance	R_{DS}	-1, 2	1000	700	1000	$V_D = +10\text{ V}; V_S = 0\text{ V}; I_{DS} = 0.5\text{ mA}$ $V_+ = +10.8\text{ V}; V_- = 0\text{ V};$ Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain OFF Leakage Current	I_D (OFF)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V};$ Test Circuit 3	$\pm\text{nA}$ max
		-2	100	1	100		
Channel ON Leakage Current	I_D (ON)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V};$ Test Circuit 4	$\pm\text{nA}$ max
		-2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V};$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1.5	1.5	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	600			$V_1 = 10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 $t_{ON}(\text{ENABLE}, \overline{\text{WRITE}})$	$t_{ON}(\text{EN}, \overline{\text{WR}})$	-1, 2	600			Test Circuit 7a, 7b, 7c	ns max
$t_{OFF}(\text{ENABLE}, \text{RESET})$	$t_{OFF}(\text{EN}, \text{RS})$	-1, 2	600				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50				dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60				dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				

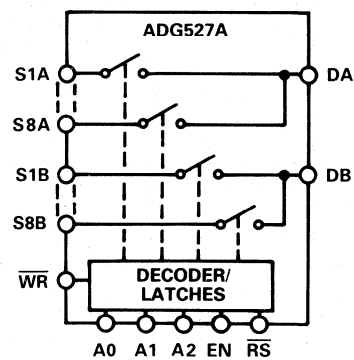
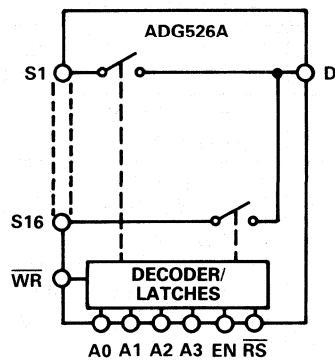
NOTE: SINGLE SUPPLY OPERATION – +15 V

¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = 0\text{ V}$.

Table 2.

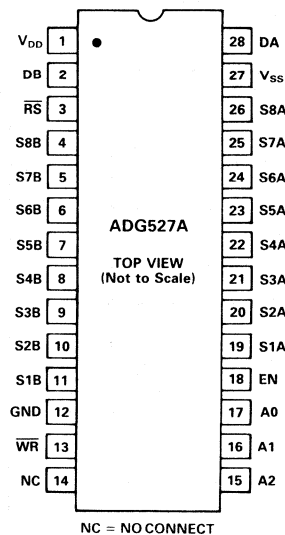
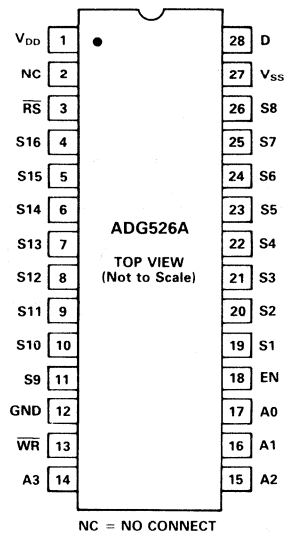
ADG526A/ADG527A

3.2.1 Functional Block Diagram and Terminal Assignments.

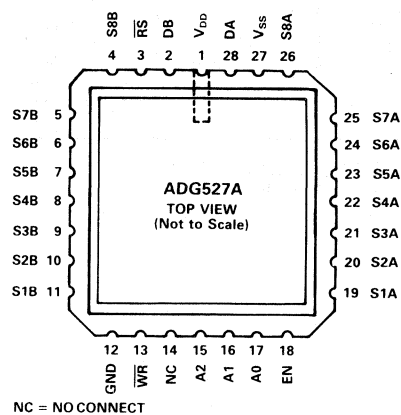
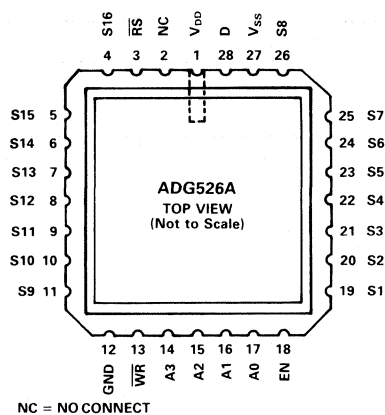


Pin Assignments

DIP



LCC



MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10**, 11**
Group C End Point Electrical Parameters, Method 5005	1

NOTES

*Indicates PDA applies to Subgroup 1.

**Subgroups 10 & 11, if not tested, shall be guaranteed to the limits in the data sheet.

Table 2.

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X		1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

X = Don't Care

Table 3. ADG526A Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X		1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

Table 4. ADG527A Truth Table

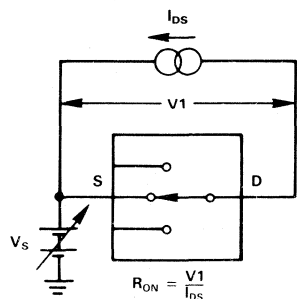
ADG526A/ADG527A

3.2.4 Microcircuit Technology Group.

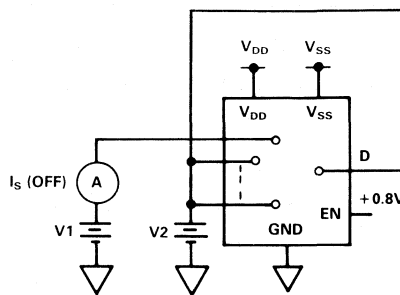
This microcircuit is covered by technology group (82).

4.2.1 Life Test/Burn-In Circuit.

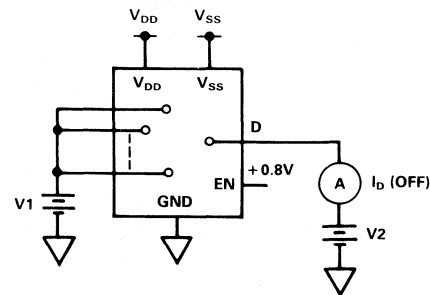
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B). Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.



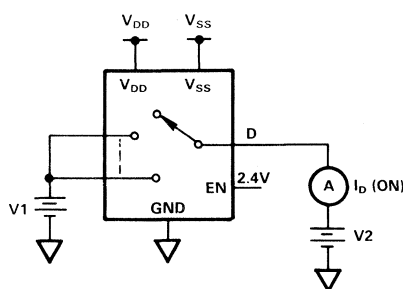
Test Circuit 1
 R_{ON}



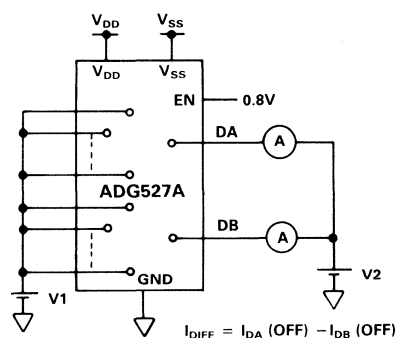
Test Circuit 2
 I_S (OFF)



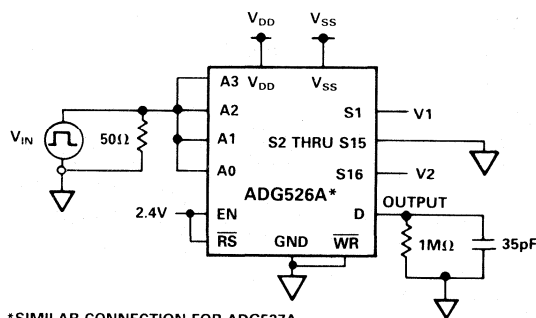
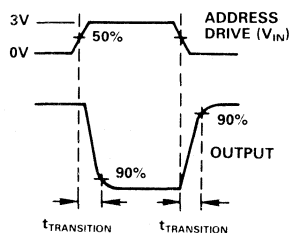
Test Circuit 3
 I_D (OFF)



Test Circuit 4
 I_D (ON)

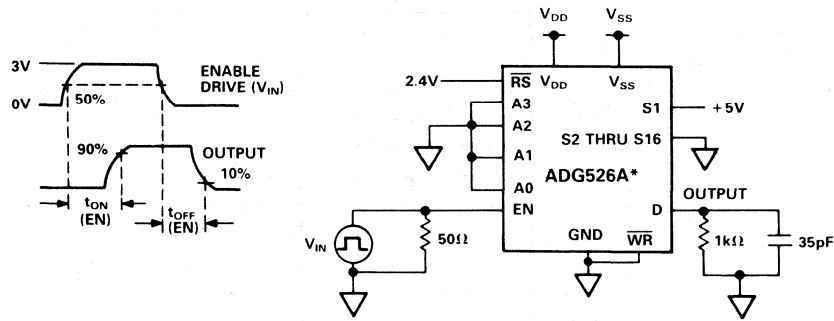


Test Circuit 5
 I_{DIFF}

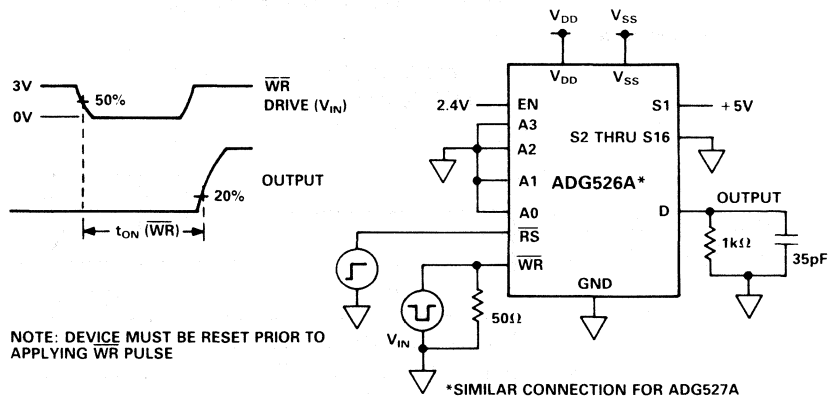


*SIMILAR CONNECTION FOR ADG527A

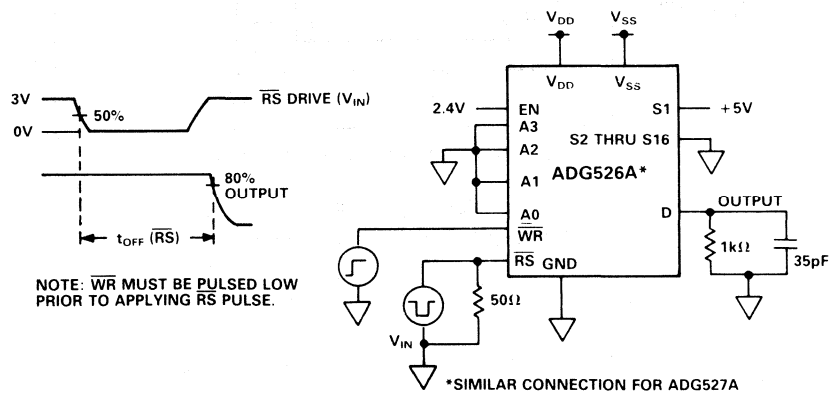
Test Circuit 6
Switching Time of Multiplexer, $t_{TRANSITION}$



Test Circuit 7a
Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

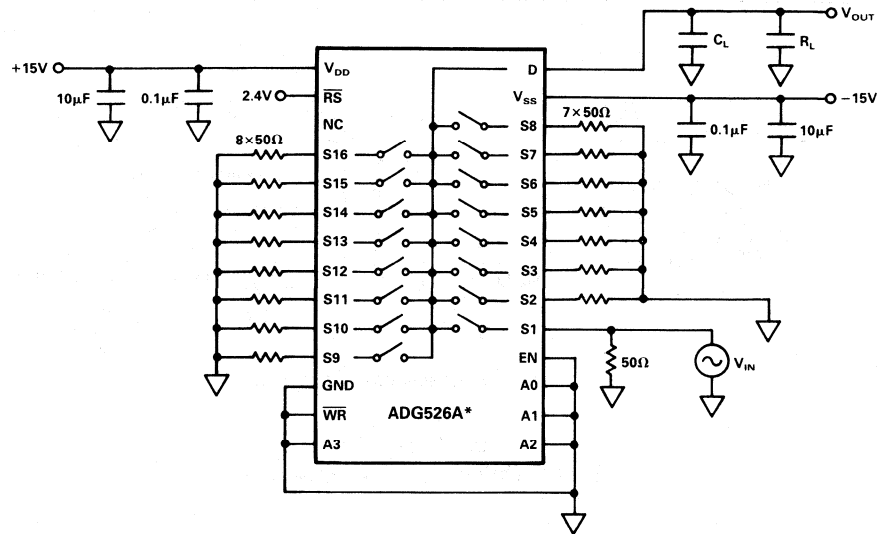


Test Circuit 7b
Write Turn-On TIME, $t_{ON}(\overline{WR})$



Test Circuit 7c
Reset Turn-Off Time, $t_{OFF}(\overline{RS})$

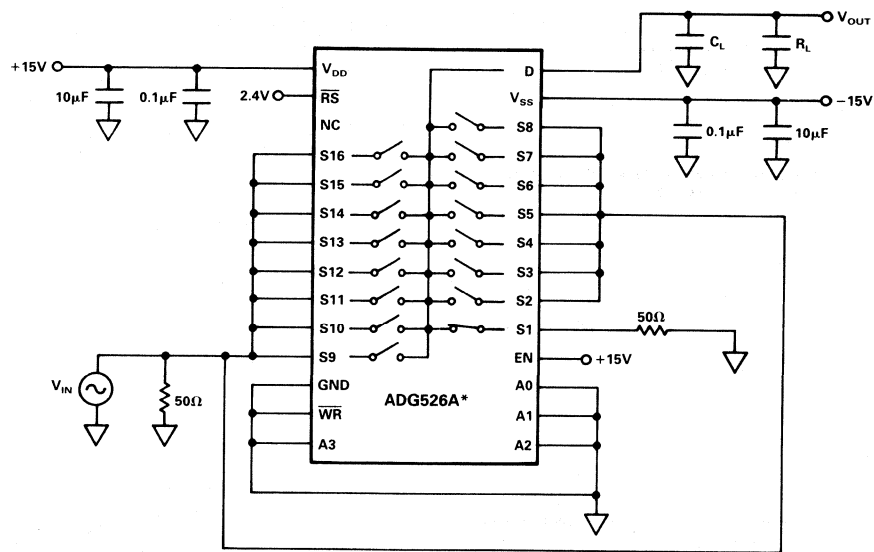
ADG526A/ADG527A



*SIMILAR TYPE OF CIRCUIT APPLIES FOR ADG527A.

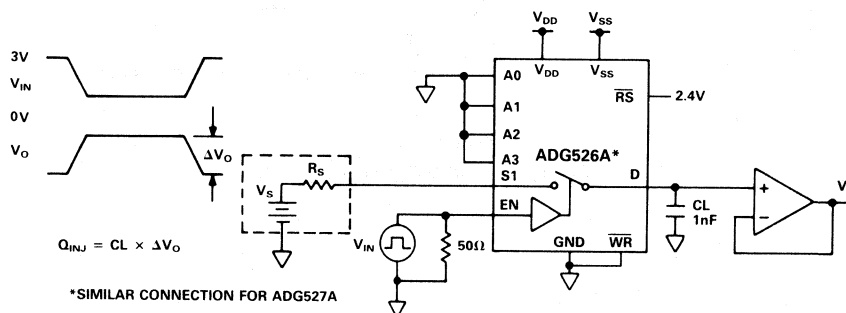
NC = NO CONNECT

*Test Circuit 8
OFF Isolation*



*SIMILAR CIRCUIT APPLIES FOR ADG527A

*Test Circuit 9
Crosstalk Between Channels*

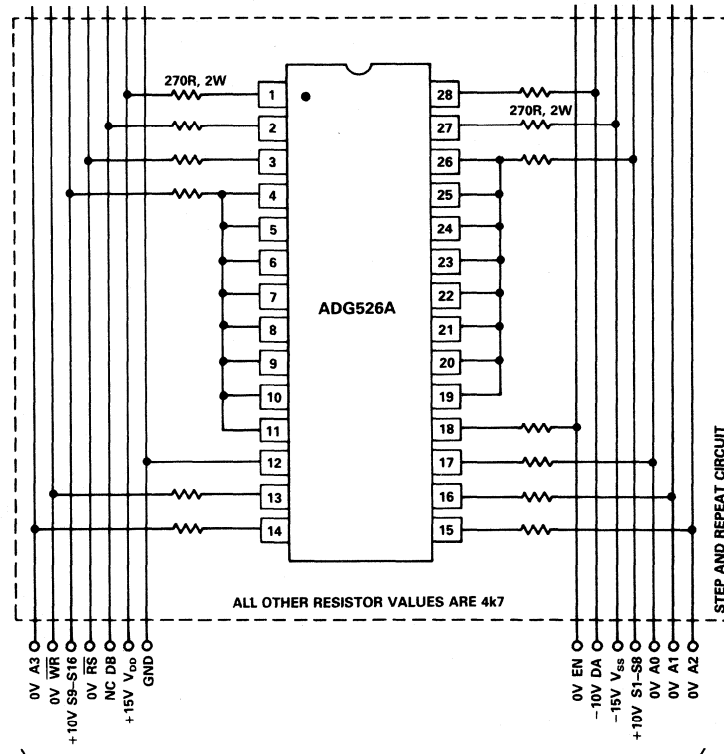


*SIMILAR CONNECTION FOR ADG527A

*Test Circuit 10
Charge Injection*

REV. A

ADG526A/ADG527A



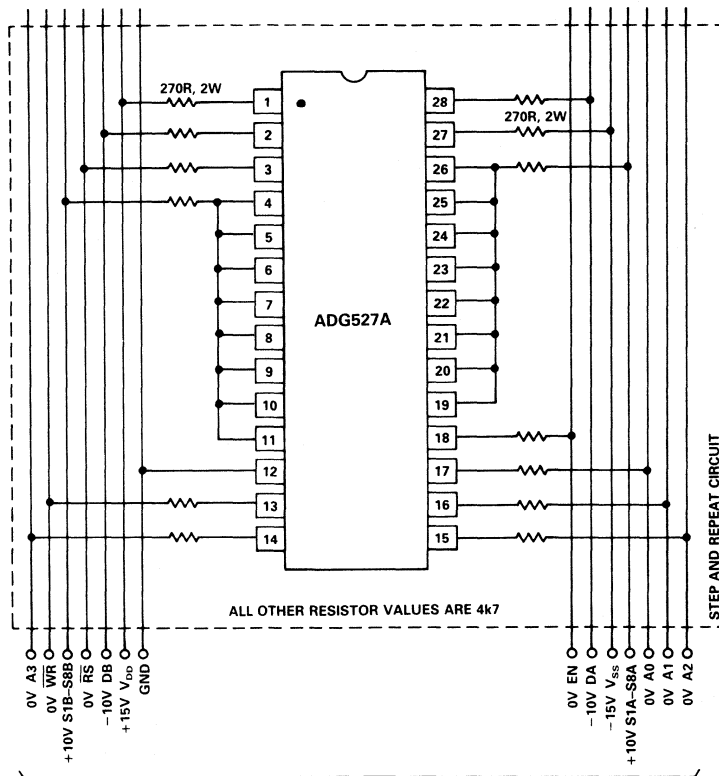
NOTES

A0, A1, A2, A3, WR, RS, and EN EACH HAVE ONE OFF 100k RESISTOR TO GND AT BOARD EDGE.

THE POWER UP SEQUENCE IS AS FOLLOWS: APPLY GND; A0, A1, A2, A3, WR, RS EN; VDD, VSS; DA; S1-S16.

NC = NO CONNECT

ADG526A Edge Connections



NOTES

A0, A1, A2, A3, WR, RS, and EN EACH HAVE ONE OFF 100k RESISTOR TO GND AT BOARD EDGE.

THE POWER UP SEQUENCE IS AS FOLLOWS: APPLY GND; A0, A1, A2, EN, WR, RS; VDD, VSS; S1A-S8A, S1B-S8B.

ADG527A Edge Connections

REV. A

Abstract

1.1 Scope.

This specification covers the detail requirements of CMOS monolithic analog multiplexers ADG528A and ADG529A with 8 channels and dual 4 channels, respectively. These multiplexers also feature high switching speeds, low R_{ON} and on-chip latches to facilitate microprocessor interfacing. Break-Before-Make switching is guaranteed.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADG528AT(X)/883B
-2	ADG529AT(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44 V
V+ to GND	25 V
V- to GND	-25 V

Analog Inputs

Voltage at S, D	V- to V+
Continuous Current, S or D	30 mA
Pulsed Current S or D	
1 ms Duration, 10% Duty Cycle	70 mA

Digital Inputs

Voltages at IN	V- -4 V to V+ +4 V or 20 mA, Whichever Occurs First
----------------	--

Power Dissipation (Package)

Up to $+75^\circ\text{C}$	470 mW/ $^\circ\text{C}$
Derates above $+75^\circ\text{C}$ by	6 mW/ $^\circ\text{C}$
Operating Temperature	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+300^\circ\text{C}$
Junction Temperature (T_J)	$+175^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-18 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-18 and E-20A

ADG528A/ADG529A – SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Conditions ¹ /Comments	Units
Switch ON Resistance	R_{DS}	-1, 2	400	300	400	$V_S = +10\text{ V}; V_S = -10\text{ V};$ $I_{DS} = 1\text{ mA};$ Test Circuit 1	Ω max
		-1, 2	600	450	600	$V_+ = +10.8\text{ V}; V_- = -10.8\text{ V};$ Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain OFF Leakage Current	I_D (OFF)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$ $V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 3	$\pm\text{nA}$ max
		-2	100	1	100		
Channel ON Leakage Current	I_D (ON)	-1	200	1	200	$V_D = V_S = \pm 10\text{ V};$ $V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ Test Circuit 4	$\pm\text{nA}$ max
		-2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_1 = \pm 10\text{ V}; V_2 = \pm 10\text{ V};$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1.5	1.5	$V_+ = +16.5\text{ V}; V_- = -16.5\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
	$-I_{CC}$	-1, 2	0.2	0.2	0.2		
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	400			$V_1 = \pm 10\text{ V}, V_2 = \pm 10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 $t_{ON}(\text{ENABLE}, \overline{\text{WRITE}})$	$t_{ON}(\text{EN}, \overline{\text{WR}})$	-1, 2	400			Test Circuit 7a, 7b, 7c	ns max
$t_{OFF}(\text{ENABLE}, \text{RESET})$	$t_{OFF}(\text{EN}, \overline{\text{RS}})$	-1, 2	400				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50			$R_L = 1\text{ k}\Omega; C_L = 12\text{ pF};$ Test Circuit 8 $V_{IN} = 10\text{ V pk-pk}, f = 100\text{ kHz};$ $T_A = +25^\circ\text{C}$	dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60			$V_S = 20\text{ V pk-pk}; R_L = 1\text{ k}\Omega;$ $C_L = 12\text{ pF}; T_A = +25^\circ\text{C};$ Test Circuit 9	dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				pF max

NOTE: DUAL SUPPLY OPERATION – $\pm 15\text{ V}$
¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = -15\text{ V}.$

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Conditions ¹ /Comments	Units
Switch ON Resistance	R_{DS}	-1, 2	1000	700	1000	$V_D = +10\text{ V}; V_S = 0\text{ V}; I_{DS} = 0.5\text{ mA}$ $V_+ = +10.8\text{ V}; V_- = 0\text{ V};$ Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	-1, 2	50	1	50	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ Test Circuit 2	$\pm\text{nA}$ max
Drain OFF Leakage Current	I_D (OFF)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V}$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V};$ Test Circuit 3	$\pm\text{nA}$ max
		-2	100	1	100		
Channel ON Leakage Current	I_D (ON)	-1	200	1	200	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V}$ Test Circuit 4	$\pm\text{nA}$ max
		-2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	-2	25		25	$V_+ = +16.5\text{ V}; V_- = 0\text{ V}$ $V_1 = +10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/+10\text{ V}$ Test Circuit 5	$\pm\text{nA}$ max
Digital Input High Voltage	V_{INH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	-1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = +16.5\text{ V}$	$\pm\mu\text{A}$ max
Low Level Input Current	I_{INL}	-1, 2	1	1	1	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{IN} = 0\text{ V}$	$\pm\mu\text{A}$ max
Supply Current	$+I_{CC}$	-1, 2	1.5	1.5	1.5	$V_+ = +16.5\text{ V}; V_- = 0\text{ V};$ $V_{INH} = 2.4\text{ V}; V_{INL} = 0.8\text{ V}$	mA max
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	-1, 2	600			$V_1 = 10\text{ V}/0\text{ V}; V_2 = 0\text{ V}/10\text{ V};$ Test Circuit 6	ns max
Subgroup 9, 10, 11 t_{ON} (ENABLE, $\overline{\text{WRITE}}$)	t_{ON} (EN, $\overline{\text{WR}}$)	-1, 2	600			Test Circuit 7a, 7b, 7c	ns max
t_{OFF} (ENABLE, $\overline{\text{RESET}}$)	t_{OFF} (EN, $\overline{\text{RS}}$)	-1, 2	600				
Subgroup 12 Off Isolation	V_{ISO}	-1, 2	50				dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	-1, 2	60				dB min
Subgroup 14 Charge Injection	Q_{INJ}	-1, 2	50				pC max
Digital Input Capacitance	C_{IN}	-1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	-1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	-1	100				pF max
		-2	50				pF max

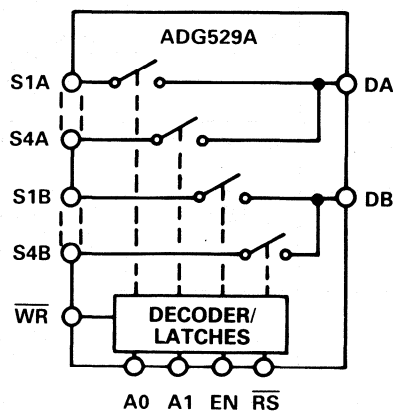
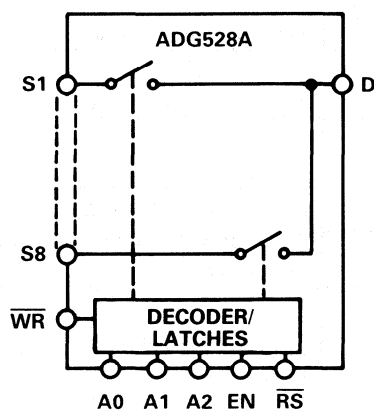
NOTE: SINGLE SUPPLY OPERATION - +15 V

¹Unless otherwise noted $V_+ = +15\text{ V}; V_- = 0\text{ V}$.

Table 2.

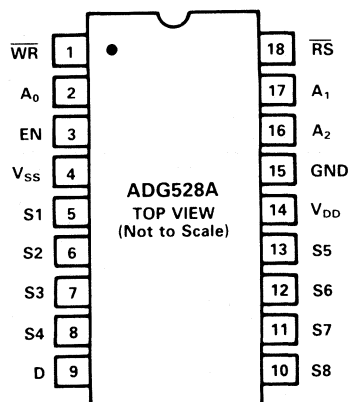
ADG528A/ADG529A

3.2.1 Functional Block Diagram and Terminal Assignments.

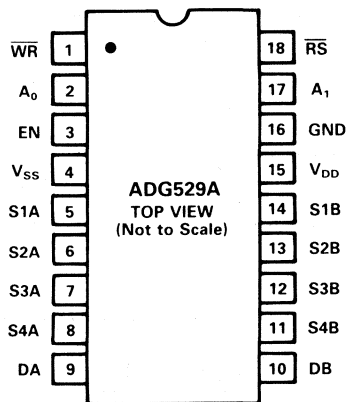


Pin Assignments

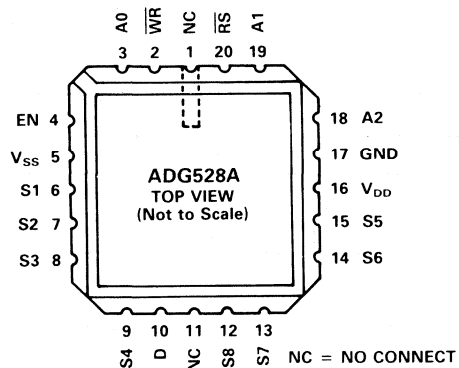
DIP Package



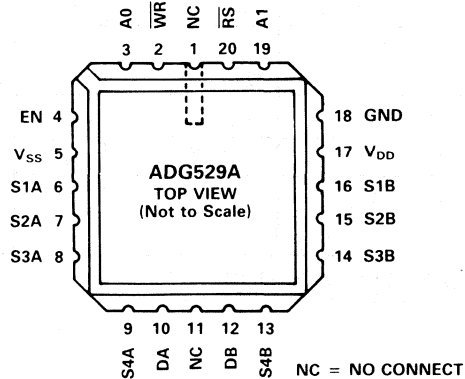
DIP Package



LCCC



LCCC



MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10**, 11**
Group C End Point Electrical Parameters, Method 5005	1

NOTES

*Indicates PDA applies to Subgroup 1.

**Subgroups 10 & 11, if not tested, shall be guaranteed to the limits in the data sheet.

TRUTH TABLES

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	$\overline{1}$	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

Table 3. ADG528 Truth Table

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	$\overline{1}$	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care

Table 4. ADG529A Truth Table

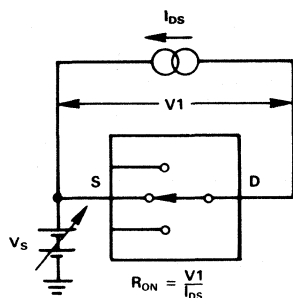
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

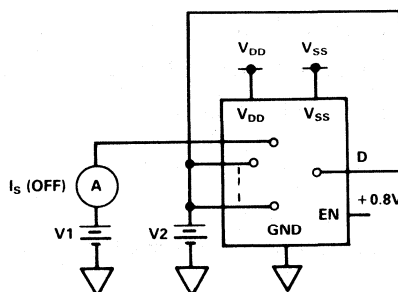
ADG528A/ADG529A

4.2.1 Life Test/Burn-In Circuit.

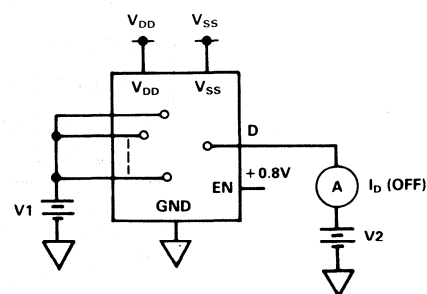
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



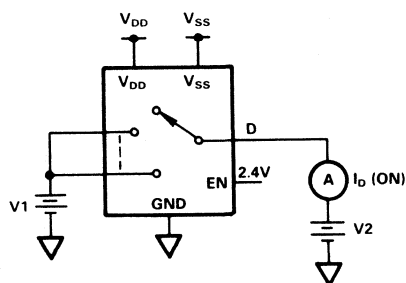
Test Circuit 1
 R_{ON}



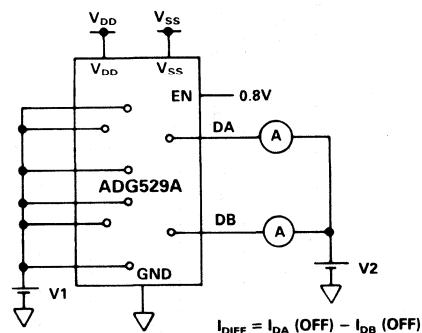
Test Circuit 2
 I_S (OFF)



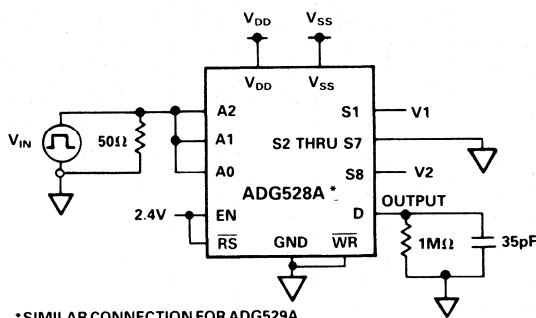
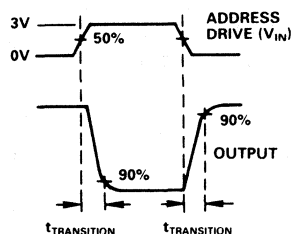
Test Circuit 3
 I_D (OFF)



Test Circuit 4
 I_D (ON)

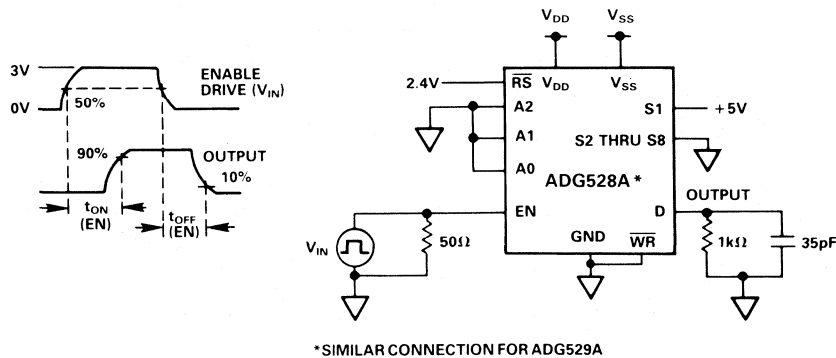


Test Circuit 5
 I_{DIFF}

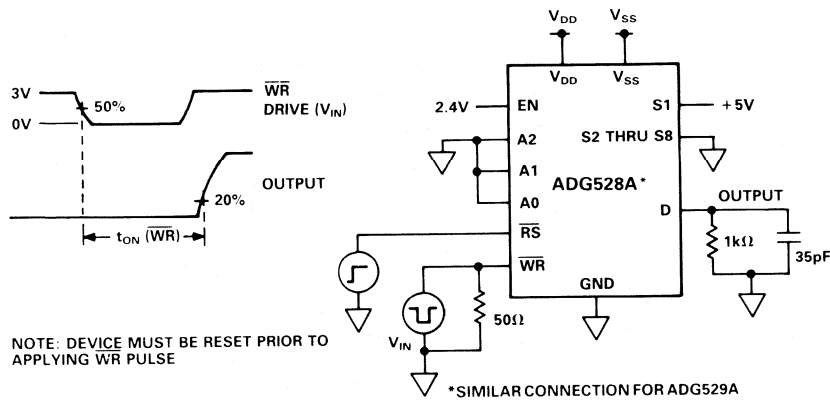


*SIMILAR CONNECTION FOR ADG529A

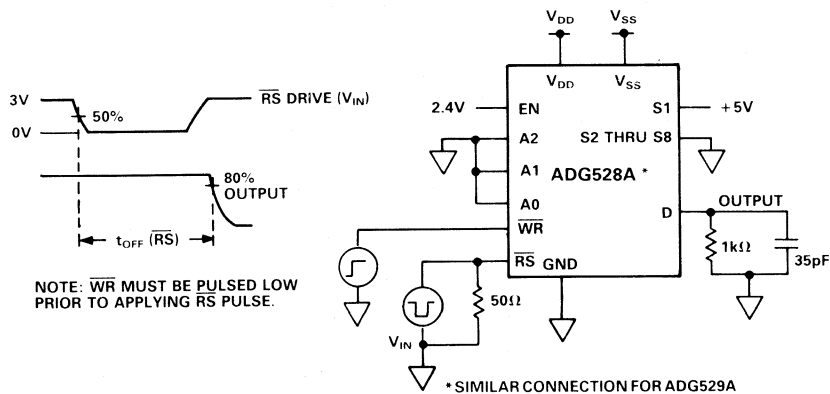
Test Circuit 6
Switching Time of Multiplexer, $t_{TRANSITION}$



Test Circuit 7a
Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

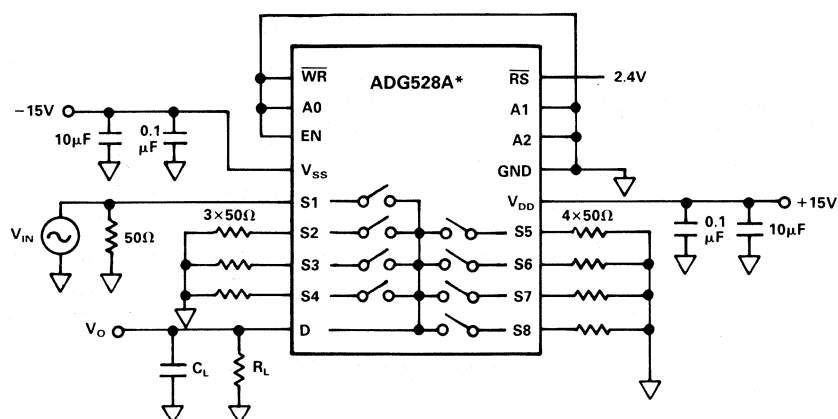


Test Circuit 7b
Write Turn-On Time, $t_{ON}(\overline{WR})$



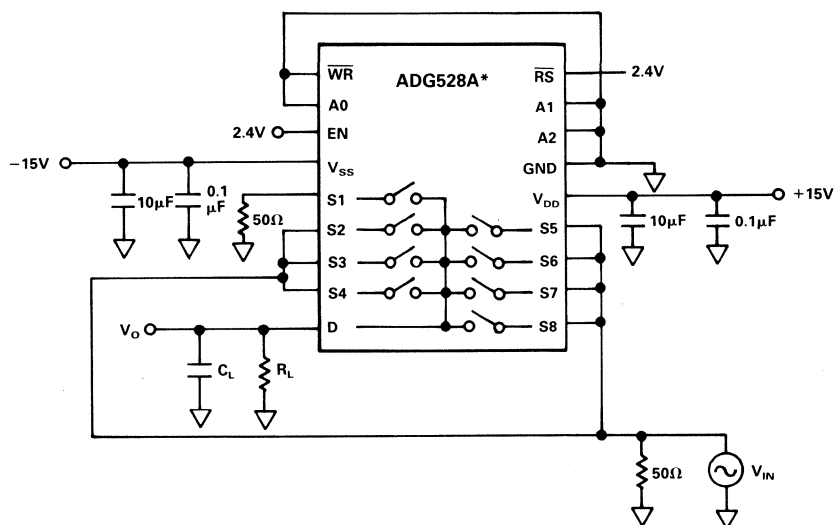
Test Circuit 7c
Reset Turn-Off Time, $t_{OFF}(\overline{RS})$

ADG528A/ADG529A



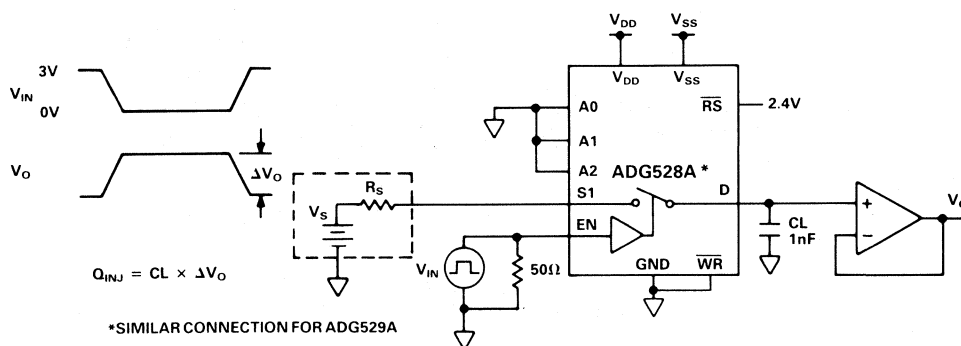
*SIMILAR TYPE OF CIRCUIT APPLIES FOR ADG529A.

Test Circuit 8
OFF Isolation



*SIMILAR TYPE OF CIRCUIT APPLIES FOR ADG529A.

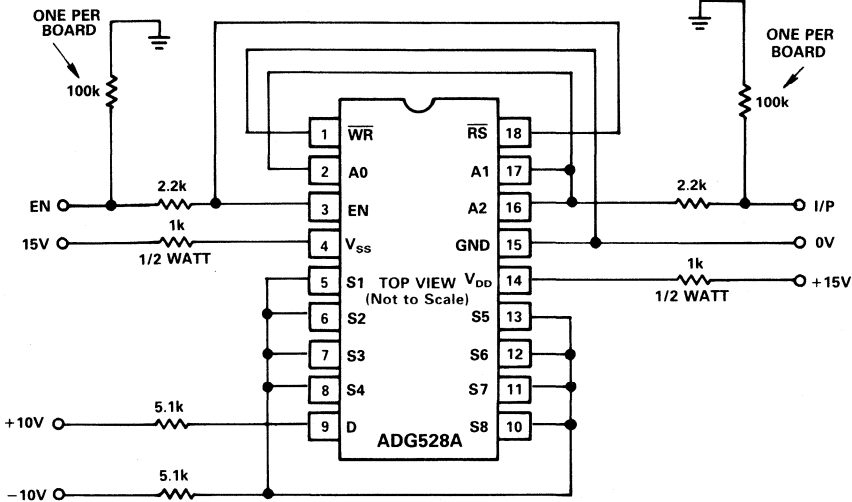
Test Circuit 9
Crosstalk Between Channels



*SIMILAR CONNECTION FOR ADG529A

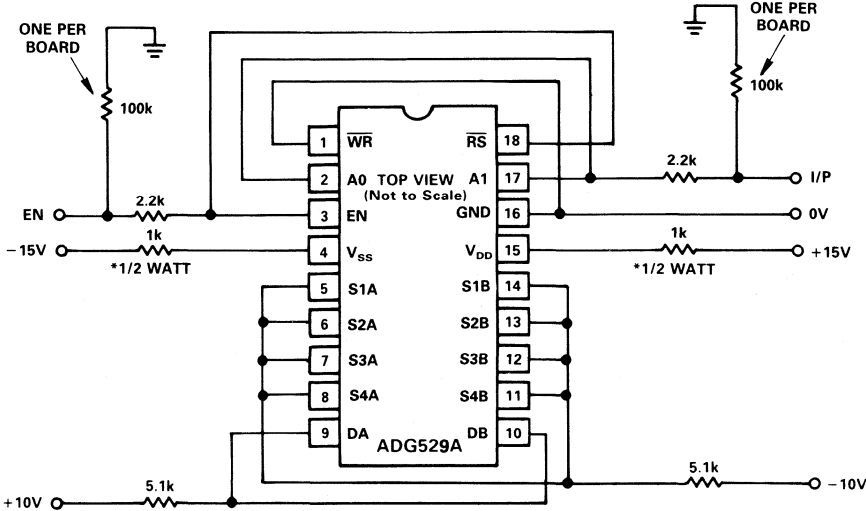
Test Circuit 10
Charge Injection

ADG528A/ADG529A



NOTES
I/P = +15V; WR = GND; EN = 0V; RS = 0V
MAX CURRENT RATINGS
MAX $I_{DD} = 2mA$ NOT THE ABSOLUTE MAX RATINGS
MAX $I_{SS} = 2mA$
MAX CONTINUOUS CURRENT S OR D = 20mA
N.B. NOTE POWER RATINGS OF 1k RESISTORS

AD528A Static Burn-In Board



NOTES
I/P = +15V; WR = GND; EN = 0V; RS = 0V
MAX CURRENT RATINGS
MAX I_{DD} = 2mA
MAX I_{SS} = 2mA **NOT THE ABSOLUTE MAX RATINGS**
***N.B. NOTE POWER RATING OF 1k RESISTORS**
MAX CONTINUOUS CURRENT S OR D = 20mA

ADG529A Static Burn-In Board

1.1 Scope.

This specification covers the detail requirements for a linear bipolar monolithic low drift amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD OP-07(X)/883B
– 2	AD OP-07A(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip
H	H-08A	8-Pin TO-99 Metal Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm V_S$
Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	
AD OP-07A, AD OP-07	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	300°C

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99 (H)	80°C	$7.1\text{mW}/^\circ\text{C}$
Cerdip (Q)	75°C	$6.7\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08A
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08A
θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8A

AD OP-07 – SPECIFICATIONS

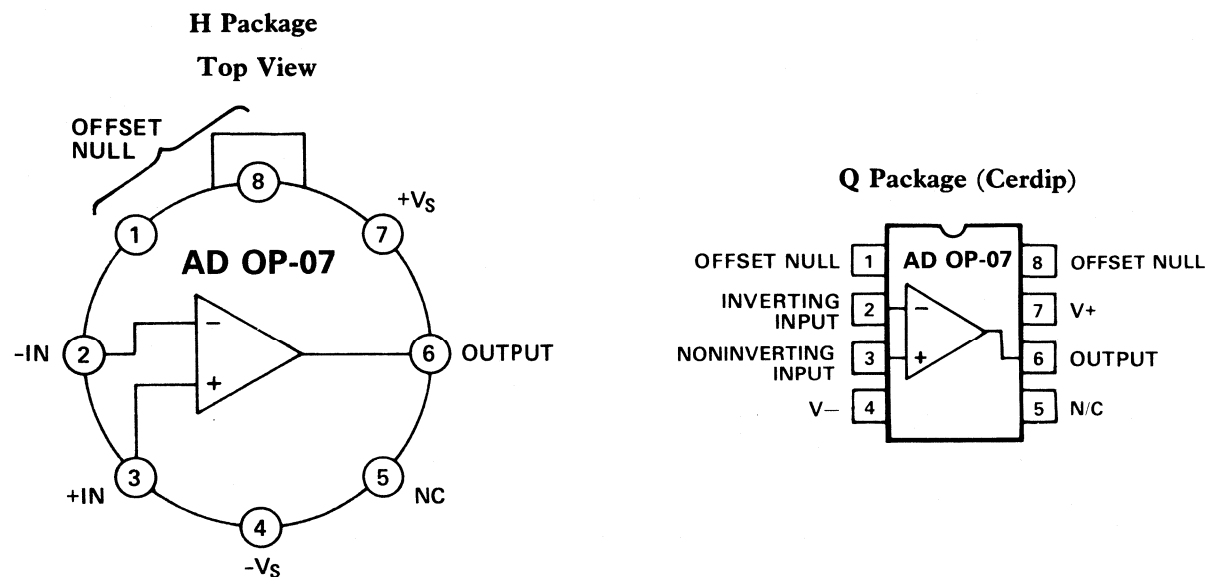
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{VS}	-1	2000	2000	1500		R _L ≥ 2kΩ, V _{OUT} = ±10V	V/mV min
			300				R _L ≥ 500Ω, V _{OUT} = ±0.5V V _S = ±3V	
		-2	3000	3000	2000		R _L ≥ 2kΩ, V _{OUT} = ±10V	
			300				R _L ≥ 500Ω, V _{OUT} = ±0.5V V _S = ±3V	
Output Voltage Swing	V _{OP}	-1, 2	12.5	12.5			R _L ≥ 10kΩ	± V min
			12.0	12.0	12		R _L = 2kΩ	
			10.5	10.5			R _L = 1kΩ	
Output Short Circuit Current	I _{SC}	-1, 2	25	58				± mA max
Input Offset Voltage	V _{IO}	-1	75	75	200			± μV max
		-2	25		60	25		
Input Offset Drift	ΔV _{IO} /ΔT	-1	1.3		1.3			± μV/°C max
		-2	0.6		0.6			
Input Offset Current	I _{IO}	-1	2.8	2.8	5.6			± nA max
		-2	2.0	2.0	4.0			
Input Bias Current	I _{IB}	-1	3	3	6			± nA max
		-2	2	2	4			
Input Offset Current Drift	dI _{IB} /dT	-1	50					± pA/°C max
		-2	25					
Input Bias Current Drift	dI _{IB} /dT	-1	50					± pA/°C max
		-2	25					
Input Resistance Differential	R _{DIFF}	-1	20					MΩ min
		-2	30					
Common-Mode Rejection Ratio	CMRR	-1, 2	110	110	106		V _{CM} = ± CMVR	dB min
Common-Mode Voltage Range	CMVR	-1, 2	13	13	13			± V min
Input Noise Voltage	e _n	-1, 2	0.6				0.1Hz to 10Hz	μV pk-pk max
Input Noise Voltage Density	e _n	-1, 2	18				f _o = 10Hz	nV/√Hz max
			13				f _o = 100Hz	
			11				f _o = 1kHz	
Input Current Noise	I _{NPP}	-1, 2	30				0.1Hz to 10Hz	pA pk-pk max
Power Supply Current	I _Q	-1, 2	4	4				mA max
Power Consumption	P _D	-1, 2	120	120				mW max
Power Supply Rejection Ratio	PSRR	-1, 2	100	100	94		± 3 ≤ V _S ≤ ± 18	dB min

NOTE

¹T_A = +25°C, V_S = ±15, unless otherwise noted.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

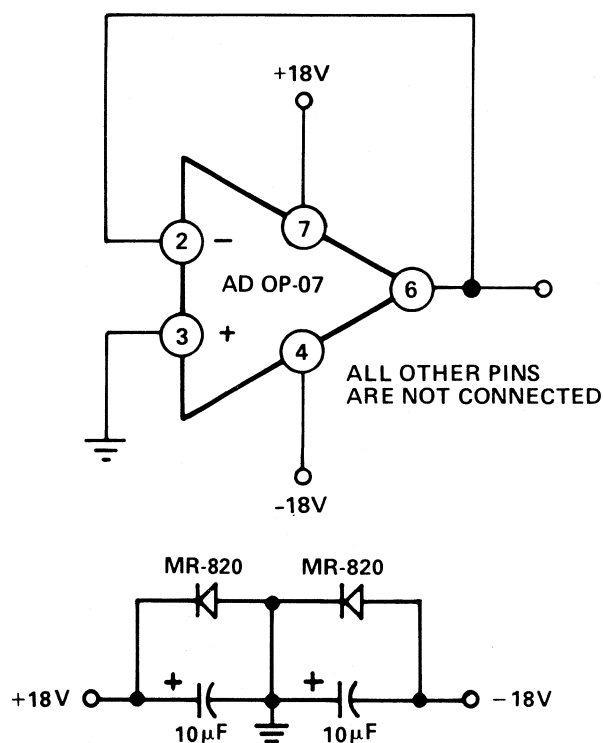


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for an ultralow noise and low offset voltage bipolar amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD OP-27C(X)/883B
-2	AD OP-27B(X)/883B
-3	AD OP-27A(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip
H	H-08A	8-Pin TO-99 Metal Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 0.7\text{V}$
Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	
AD OP-27A, AD OP-27B, AD OP-27C	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$
Differential Input Current	$\pm 25\text{mA}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Package Type		
TO-99 (H)	80°C	$7.1\text{mW}/^\circ\text{C}$
Cerdip (Q)	75°C	$6.7\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08A
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08A
θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8A

AD OP-27 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	- 1	700	700	300		R _L ≥ 2kΩ, V _{OUT} = ± 10V	V/mV min
			200				R _L = 600Ω V _{OUT} = ± 1V, V _S = ± 4V	
		- 2	1000	1000	500		R _L ≥ 2kΩ, V _{OUT} = ± 10V	
			800	800			R _L ≥ 1kΩ, V _{OUT} = ± 10V	
			250				R _L = 600Ω V _{OUT} = ± 1V, V _S = ± 4V	
		- 3	1000	1000	600		R _L ≥ 2kΩ, V _{OUT} = ± 10V	
			800	800			R _L ≥ 1kΩ, V _{OUT} = ± 10V	
			250				R _L = 600Ω V _{OUT} = ± 1V, V _S = ± 4V	
Gain Bandwidth Product	GBW	- 1, 2, 3	5					MHz min
Slew Rate	t _{SR}	- 1, 2, 3	1.7					V/μs min
Input Current Noise Density	I _N	- 1	0.6				f _o = 1kHz	pA/√Hz max
		- 2, 3	4.0				f _o = 10Hz	
			2.3				f _o = 30Hz	
			0.6				f _o = 1kHz	
Output Voltage Swing	V _{OUT}	- 1	11.5	11.5	10.5		R _L ≥ 2kΩ	± V min
			10.0	10.0			R _L = 600Ω	
		- 2	12.0	12.0	11.0		R _L ≥ 2kΩ	
			10.0	10.0			R _L = 600Ω	
		- 3	12.0	12.0	11.5		R _L ≥ 2kΩ	
			10.0	10.0			R _L = 600Ω	
Output Short Circuit Current	I _{SC}	- 1, 2, 3	25	55				± mA max
Input Offset Voltage	V _{OS}	- 1	100	100	300			± μV max
		- 2	60	60	200			
		- 3	25		60	25		
Input Offset Drift ²	TC V _{OS}	- 1	1.8		1.8			± μV/°C max
		- 2	1.3		1.3			
		- 3	0.6		0.6			
Input Offset Current	I _{OS}	- 1	75	75	135			± nA max
		- 2	50	50	85			
		- 3	35	35	50			
Input Bias Current	I _B	- 1	80	80	150			± nA max
		- 2	55	55	95			
		- 3	40	40	60			
Common-Mode Rejection Ratio	CMRR	- 1	100	100	94		V _{CM} = ± 11V	dB min
		- 2	106	106	100		V _{CM} = ± 10V for	
		- 3	114	114	108		Subgroup 2, 3	
Input Resistance Differential	R _{DIFF}	- 1	0.8					MΩ min
		- 2	1.2					
		- 3	1.5					
Differential Input Voltage ³	V _{DIFF}	- 1, 2, 3	0.7					± V max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Common-Mode Voltage Range	CMVR	-1	11.0	11.0	10.2			± V min
		-2, 3	11.0	11.0	10.3			
Input Noise Voltage	E _{NPP}	-1	0.25				0.1Hz to 10Hz	μV pk-pk max
		-2, 3	0.18					
Input Noise Voltage Density	E _N	-1	8.0				f _o = 10Hz	nV/√Hz max
			5.6				f _o = 30Hz	
			4.5				f _o = 1kHz	
		-2	5.5				f _o = 10Hz	
			4.5				f _o = 30Hz	
			3.8				f _o = 1kHz	
		-3	5.5				f _o = 10Hz	
			4.5				f _o = 30Hz	
			3.8				f _o = 1kHz	
Power Supply Current	I _Q	-1	5.6	5.6			V _S = ±15V	mA max
		-2, 3	4.6	4.6				
Power Consumption	P _D	-1	170	170			V _{OUT} = 0V	mW max
		-2, 3	140	140				
Power Supply Rejection Ratio	PSRR	-1	20	20	51		V _S = ±4V to ±18V	μV/V max
		-2	10	10	20			
		-3	10	10	16			

NOTES

¹T_A = +25°C, V_S = ±15 unless otherwise noted.

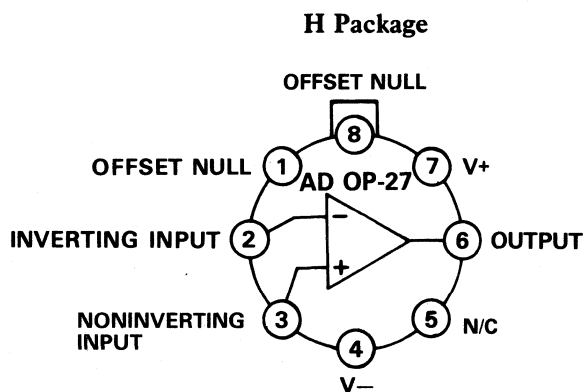
²TCV_{OS} is within specification unnullled, or when nullled with R_P = 8 to 20kΩ.

³If the differential input voltage exceeds ±0.7V, then the output current should be limited to 25mA.

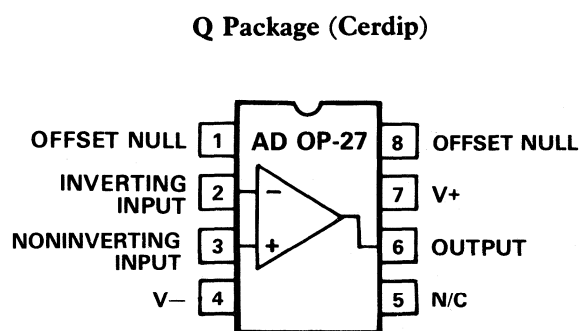
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



NOTE: PIN 4 CONNECTED TO CASE



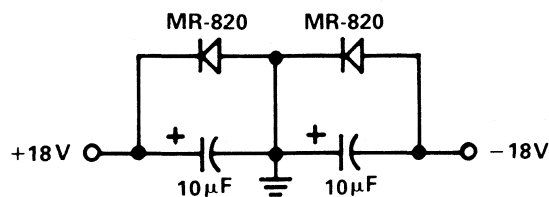
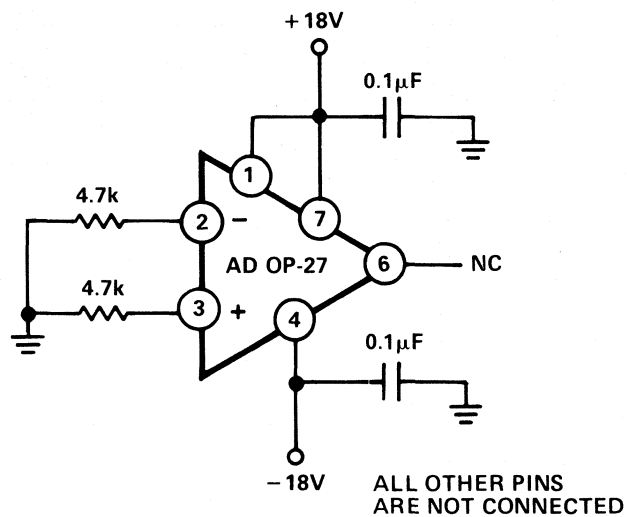
AD OP-27

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for an ultralow noise, high speed precision bipolar amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD OP-37C(X)/883B
– 2	AD OP-37B(X)/883B
– 3	AD OP-37A(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip
H	H-08A	8-Pin TO-99 Metal Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm 0.7\text{V}$
Input Voltage	$\pm V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	300°C
Differential Input Current	$\pm 25\text{mA}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
TO-99 (H)	80°C	$7.1\text{mW}/^\circ\text{C}$
Cerdip (Q)	75°C	$6.7\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08A
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08A
θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8A

AD OP-37 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A _{OL}	- 1	700	700	300		R _L ≥ 2kΩ, V _{OUT} = ± 10V	V/mV min
			200				R _L = 600Ω V _{OUT} = ± 1V, V _S = ± 4V	
		- 2	1000	1000	500		R _L ≥ 2kΩ, V _{OUT} = ± 10V	
			800	800			R _L ≥ 1kΩ, V _{OUT} = ± 10V	
			250				R _L = 600Ω V _{OUT} = ± 1V, V _S = ± 4V	
		- 3	1000	1000	600		R _L ≥ 2kΩ, V _{OUT} = ± 10V	
			800	800			R _L ≥ 1kΩ, V _{OUT} = ± 10V	
			250				R _L = 600Ω V _{OUT} = ± 1V, V _S = ± 4V	
Gain Bandwidth Product	GBW	- 1, 2, 3	45				f _o = 10kHz	MHz min
Slew Rate	t _{SR}	- 1, 2, 3	11.0					V/μs min
Input Current Noise Density	I _N	- 1	0.6				f _o = 1kHz	pA/√Hz max
		- 2, 3	4.0				f _o = 10Hz	
			2.3				f _o = 30Hz	
			0.6				f _o = 1kHz	
Output Voltage Swing	V _{OUT}	- 1	11.5	11.5	10.5		R _L ≥ 2kΩ	± V min
			10.0	10.0			R _L = 600Ω	
		- 2	12.0	12.0	11.0		R _L ≥ 2kΩ	
			10.0	10.0			R _L = 600Ω	
		- 3	12.0	12.0	11.5		R _L ≥ 2kΩ	
			10.0	10.0			R _L = 600Ω	
Output Short Circuit Current	I _{SC}	- 1, 2, 3	25	55				± mA max
Input Offset Voltage	V _{OS}	- 1	100	100	300			± μV max
		- 2	60	60	200			
		- 3	25		60	25		
Input Offset Drift ²	TC V _{OS}	- 1	1.8		1.8			± μV/°C max
		- 2	1.3		1.3			
		- 3	0.6		0.6			
Input Offset Current	I _{OS}	- 1	75	75	135			± nA max
		- 2	50	50	85			
		- 3	35	35	50			
Input Bias Current	I _B	- 1	80	80	150			± nA max
		- 2	55	55	95			
		- 3	40	40	60			
Common-Mode Rejection Ratio	CMRR	- 1	100	100	94		V _{CM} = ± 11V	dB min
		- 2	106		100	106	V _{CM} = ± 10V for	
		- 3	114		108	114	Subgroup 2, 3	
Input Resistance Differential	R _{DIFF}	- 1	0.8					MΩ min
		- 2	1.2					
		- 3	1.5					
Differential Input Voltage ³	V _{DIFF}	- 1, 2, 3	0.7					± V max

Table 1. (Continued on next page)

REV. B

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Common-Mode Voltage Range	CMVR	-1	11.0	11.0	10.2			$\pm V$ min
		-2, 3	11.0	11.0	10.3			
Input Noise Voltage	E_{NPP}	-1	0.25				0.1Hz to 10Hz	μV pk-pk max
		-2, 3	0.18					
Input Noise Voltage Density	E_N	-1	8.0				$f_o = 10\text{Hz}$	$nV/\sqrt{Hz}$ max
			5.6				$f_o = 30\text{Hz}$	
			4.5				$f_o = 1\text{kHz}$	
		-2, 3	5.5				$f_o = 10\text{Hz}$	
			4.5				$f_o = 30\text{Hz}$	
			3.8				$f_o = 1\text{kHz}$	
Power Supply Current	I_Q	-1	5.6	5.6			$V_S = \pm 15V$	mA max
		-2, 3	4.6	4.6				
Power Consumption	P_D	-1	170	170			$V_{OUT} = 0V$	mW max
		-2, 3	140	140				
Power Supply Rejection Ratio	PSRR	-1	20	20	51		$V_S = \pm 4V$ to $\pm 18V$	$\mu V/V$ max
		-2	10	10	20			
		-3	10	10	16			

NOTES

¹ $T_A = +25^\circ\text{C}$, $V_S = \pm 15V$, unless otherwise specified.

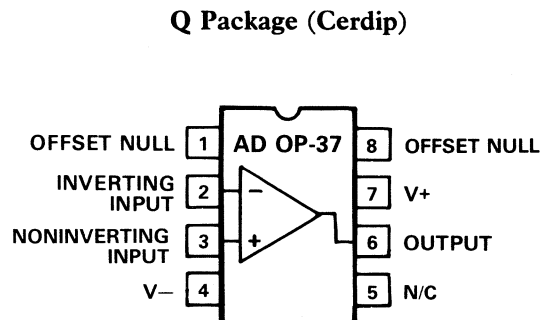
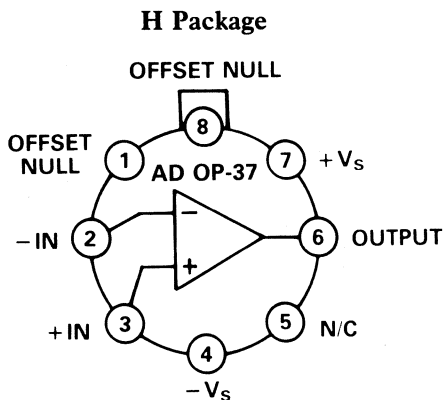
² TCV_{OS} is within specification unnull, or when nulled with $R_P = 8$ to $20k\Omega$.

³If the differential input voltage exceeds $\pm 0.7V$, then the output current should be limited to 25mA.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



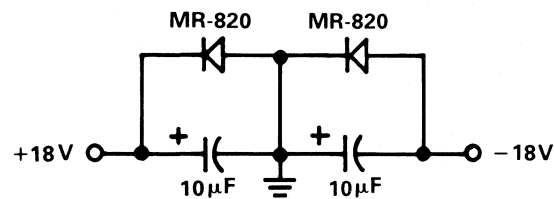
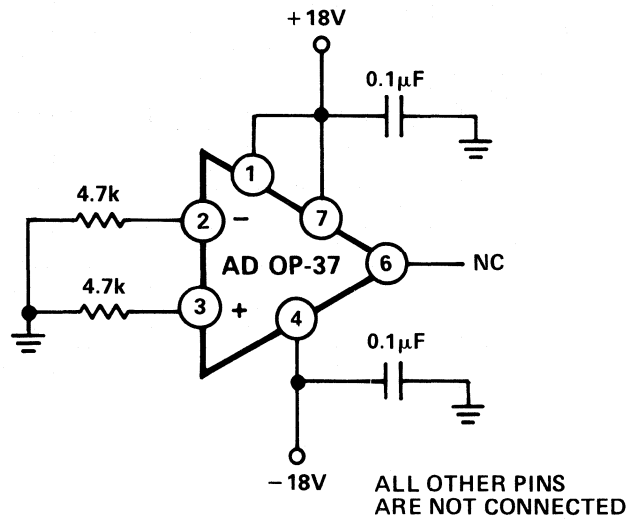
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

AD OP-37

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a 10 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADREF01Q/883B
-2	ADREF01AQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{IN} to Ground	+ 36V
Power Dissipation	500mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

ADREF01 – SPECIFICATIONS

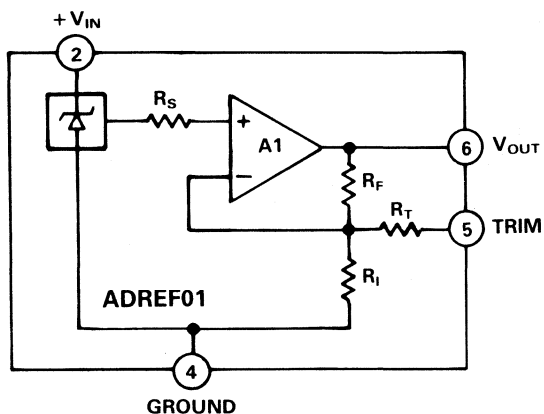
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	– 1, 2	4	4				+ mA max
Output Voltage Error	V _{OUT}	– 1 – 2	50 30	50 50		30		± mV max
Output Voltage Temperature Coefficient	V _{OUT} /dT	– 1 – 2	25 8.5		25 8.5		T _A = – 55°C to + 125°C	± ppm/°C
Gain Adjustment	V _{ADJ}	– 1, 2	+ 300 – 100	+ 300 – 100				mV min
Line Regulation	VR _{LINE}	– 1, 2	100	100	100		13.5V ≤ V _{IN} ≤ 36V	± μV/V max
Load Regulation, Sourcing	VR _{LOAD}	– 1, 2	100	100	100		I _L = 0 to 10mA	± μV/mA max
Load Regulation, Sinking	I _{OUT}	– 1, 2	100	100	100		I _L = – 10 to 0mA	± μV/mA max
Output Short-Circuit Current	I _{OS}	– 1, 2	50	50			To Ground	+ mA max
Output Short-Circuit Current	I _{OS}	– 1, 2	50	50			To V _{IN}	– mA max

NOTE

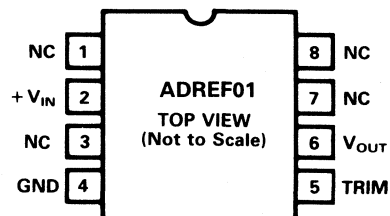
¹T_A = + 25°C; V_{CC} = + 15V unless otherwise stated.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



NOTE: MAKE NO CONNECTIONS TO PINS 1, 3, 7 AND 8.

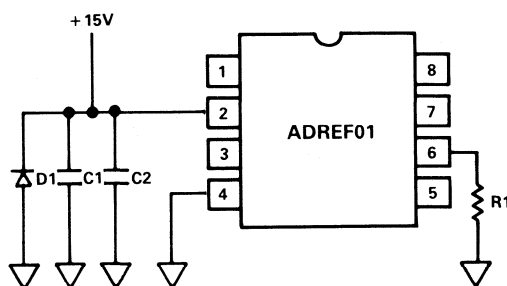


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE: D1 = MR-820
C1 = 0.1 μ F
C2 = 47 μ F
R1 = 1k Ω 1/2 WATT AT 25°C

1.1 Scope.

This specification covers the detail requirements for a 5 volt IC reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADREF02Q/883B
-2	ADREF02AQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Input Voltage V_{IN} to Ground	+36V
Power Dissipation	500mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

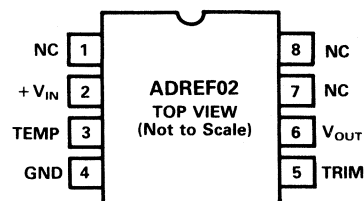
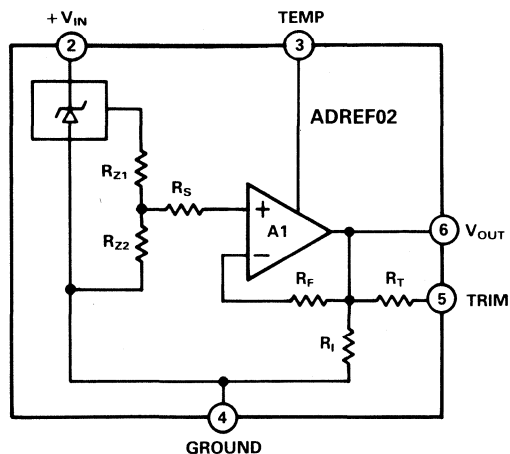
Thermal Resistance $\theta_{JC} = 22^\circ\text{C/W}$
 $\theta_{JA} = 110^\circ\text{C/W}$

ADREF02 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Quiescent Current	I _{CC}	– 1, 2	3	3				+ mA max
Output Voltage Error	V _{OUT}	– 1 – 2	25 15	25 25		15		± mV max
Gain Adjustment	V _{ADJ}	– 1, 2	+ 300 – 100	+ 300 – 100				mV min
Line Regulation	VR _{LINE}	– 1, 2	150	150	150		11.4V ≤ V _{IN} ≤ 36V	± μV/V max
Load Regulation, Sourcing	VR _{LOAD}	– 1, 2	150	150	150		I _L = 0 to 10mA	± μV/mA max
Load Regulation, Sinking	I _{OUT}	– 1, 2	400	400			I _L = – 10 to 0mA	± μV/mA max
Output Voltage Temperature Coefficient	DV _{OUT} /dT	– 1 – 2	25 8.5		25 8.5		T _A = – 55°C to + 125°C	± ppm/°C max
Output Short-Circuit Current	I _{OS}	– 1	50	50			To Ground	+ mA max

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



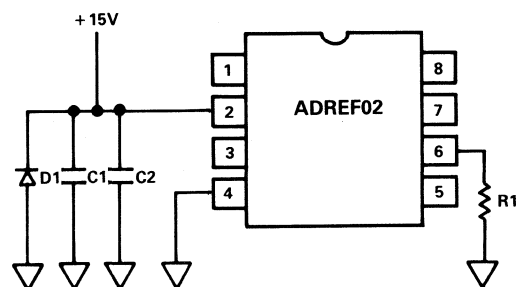
NOTE: PINS 1, 7 & 8 ARE INTERNAL TEST POINTS.
MAKE NO CONNECTIONS TO THESE POINTS.

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (59).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE: D1 = MR-820
C1 = 0.1 μ F
C2 = 47 μ F
R1 = 500 Ω 1/2 WATT AT 25°C

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8×8-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	ADSP-1008ASD/883B
–2	ADSP-1008ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1008A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –1 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.6	0.6			V _{DD} = min I _{OH} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = 0 V (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	40	55	55			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	25	30	30			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay*	t _D	–1, 2	25			35	35	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t _{ENA}	–1, 2	25			35	35	Notes 2 and 3	ns max
Three-State Disable* (High or Low to High Z)	t _{DIS}	–1, 2	25			35	35	Notes 2 and 3	ns max
Clock Pulse Width*	t _{PW}	–1, 2	15			25	25	Note 2	ns min
Input Setup Time*	t _S	–1, 2	15			20	20	Note 2	ns min
Input Hold Time*	t _H	–1, 2	3			3	3	Note 2	ns min
Multiply/Accumulate Time*	t _{MAC}	–1	60			80	80	Note 2	ns max
		–2	50			65	65		

NOTES

*Indicates that a limit for this parameter has changed from REV. D.

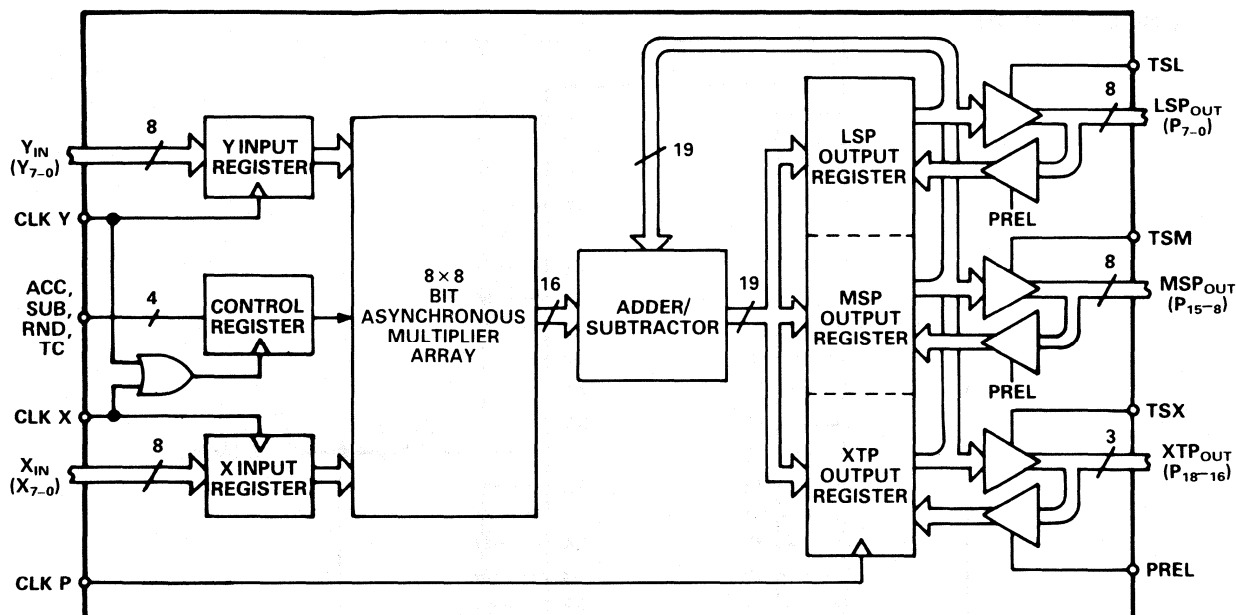
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	P12	25	X3
2	P11	26	X4
3	P10	27	X5
4	P9	28	X6
5	P8	29	X7
6	TSM	30	CLK X
7	CLK P	31	CLK Y
8	PREL	32	Y0
9	P7	33	Y1
10	P6	34	Y2
11	P5	35	Y3
12	GND	36	Y4
13	P4	37	V _{CC}
14	P3	38	Y5
15	P2	39	Y6
16	P1	40	Y7
17	P0	41	TC
18	TSL	42	TSX
19	SUB	43	P18
20	ACC	44	P17
21	RND	45	P16
22	X0	46	P15
23	X1	47	P14
24	X2	48	P13

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

ADSP-1008A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

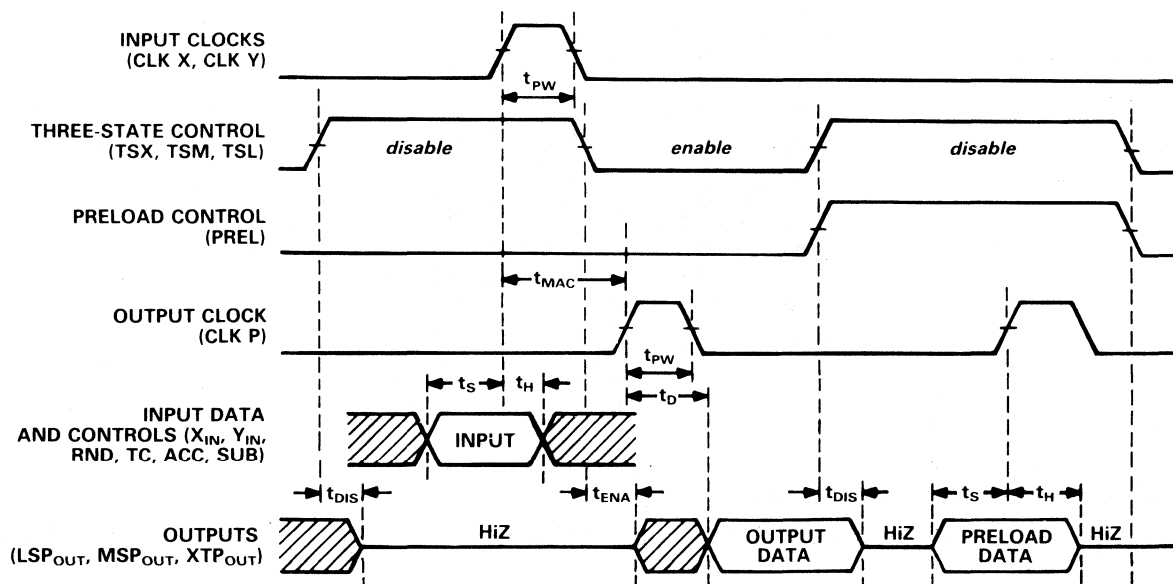
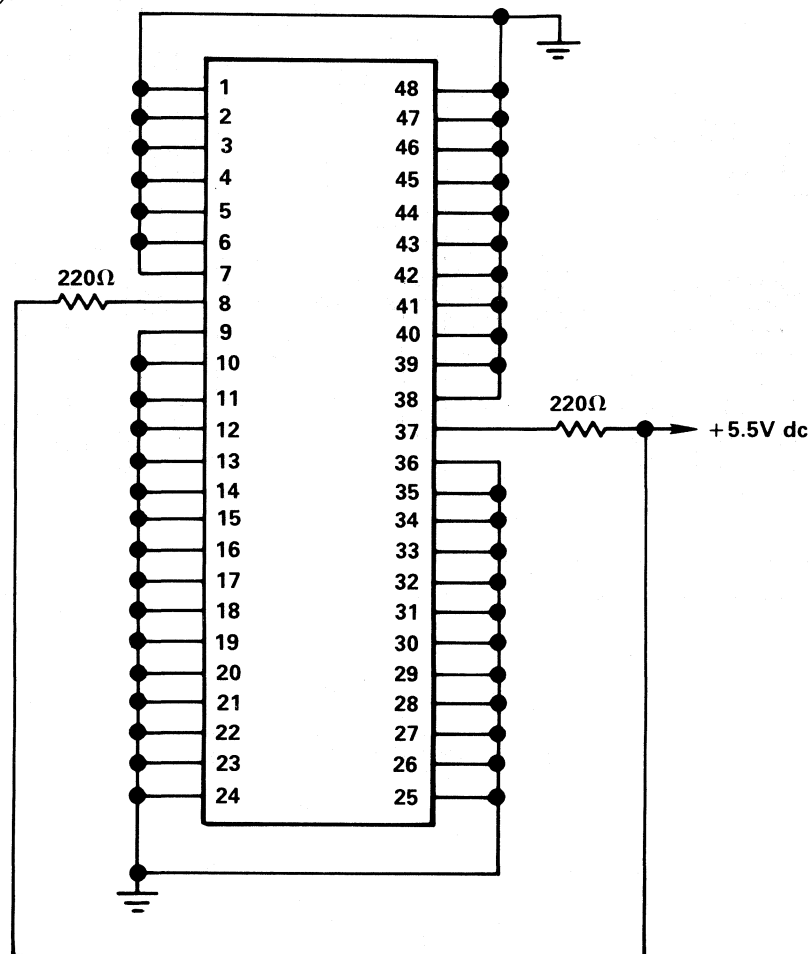


Figure 1. ADSP-1008A Timing Diagram

REV. E

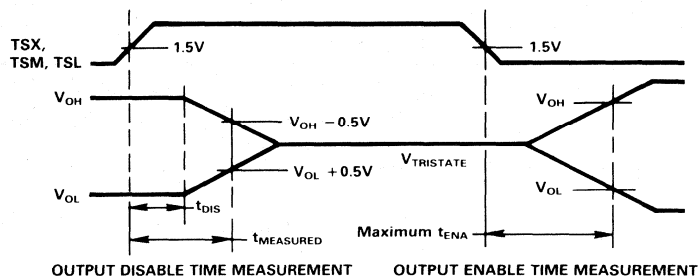


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

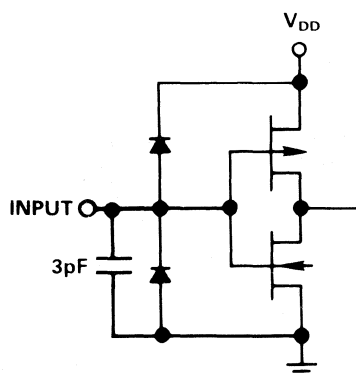


Figure 3. Equivalent Input Circuit

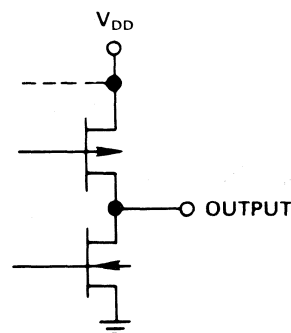


Figure 4. Equivalent Output Circuit

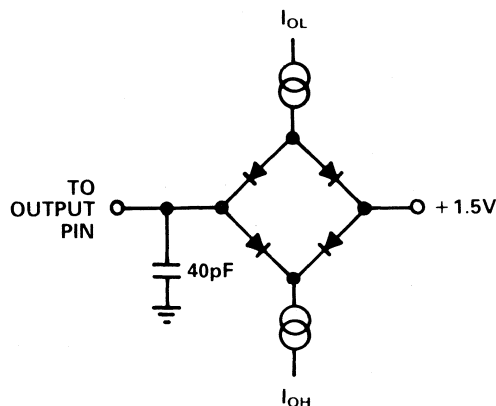


Figure 5. Normal Load Circuit for AC Measurements

ACC	SUB	Function
1	1	$\text{Accumulator}_t = X_t \cdot Y_t - \text{Accumulator}_{t-1}$
1	0	$\text{Accumulator}_t = X_t \cdot Y_t + \text{Accumulator}_{t-1}$
0	X	$\text{Accumulator}_t = X_t \cdot Y_t$

Table 2. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:

Z = Output buffers at high impedance (output disabled)

Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.

Preload = Output buffers at high impedance.

Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table 3. Preload Truth Table

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12×12-bit digital multiplier/accumulator integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	ADSP-1009AS(X)/883B
–2	ADSP-1009AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
E	E-68A	68-Contact LCC
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1009A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –0.4 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage* Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = 0 V (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	70	75	75			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	35	40	40			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay*	t _D	–1, 2	35			40	40	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t _{ENA}	–1, 2	30			35	35	Notes 2 and 3	ns max
Three-State Disable* (High or Low to High Z)	t _{DIS}	–1, 2	20			30	30	Notes 2 and 3	ns max
Input Setup Time*	t _S	–1, 2	20			20	20	Note 2	ns min
Clock Pulse Width*	t _{PW}	–1, 2	15			25	25	Note 2	ns min
Input Hold Time*	t _H	–1, 2	2			3	3	Note 2	ns min
Multiply/Accumulate Time*	t _{MAC}	–1	85			105	105	Note 2	ns max
		–2	70			90	90		

NOTES

*Indicates that a limit for this parameter has changed from REV. D.

¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0.3 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

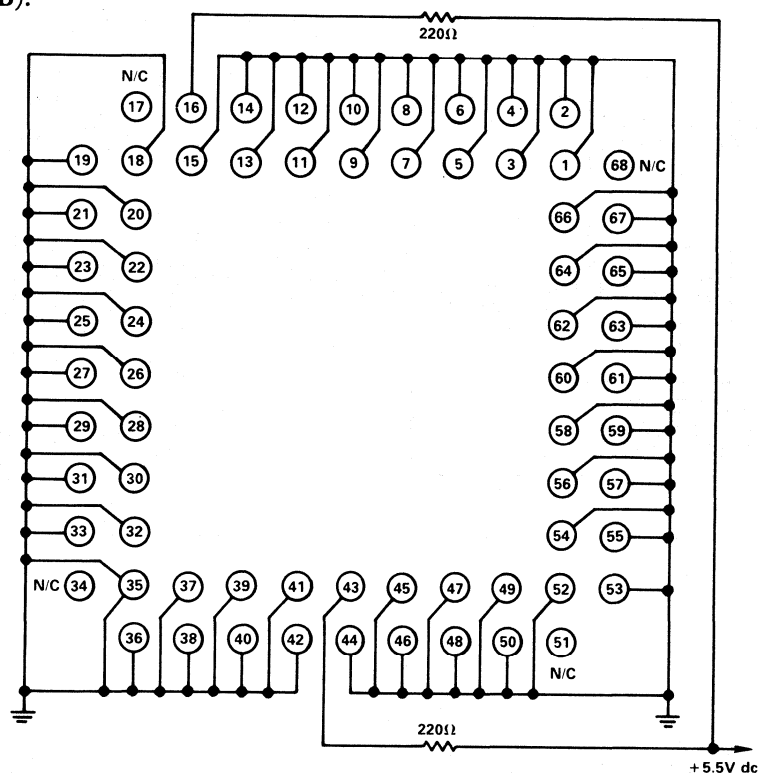
³Transitions measured per Figure 2.

Table 1.

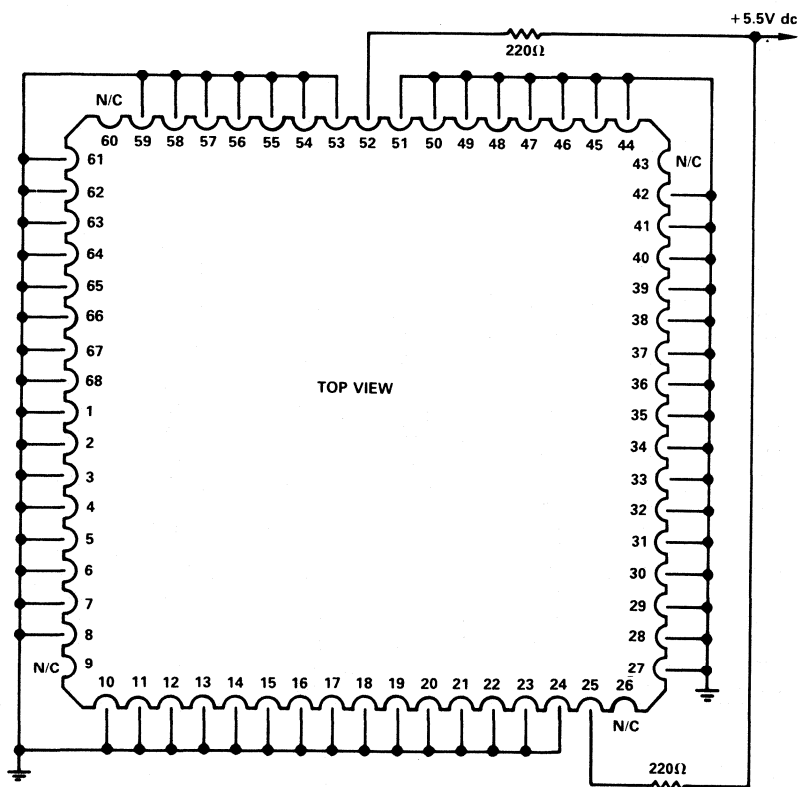
ADSP-1009A

4.2.1 Life Test/Burn-In Circuit.

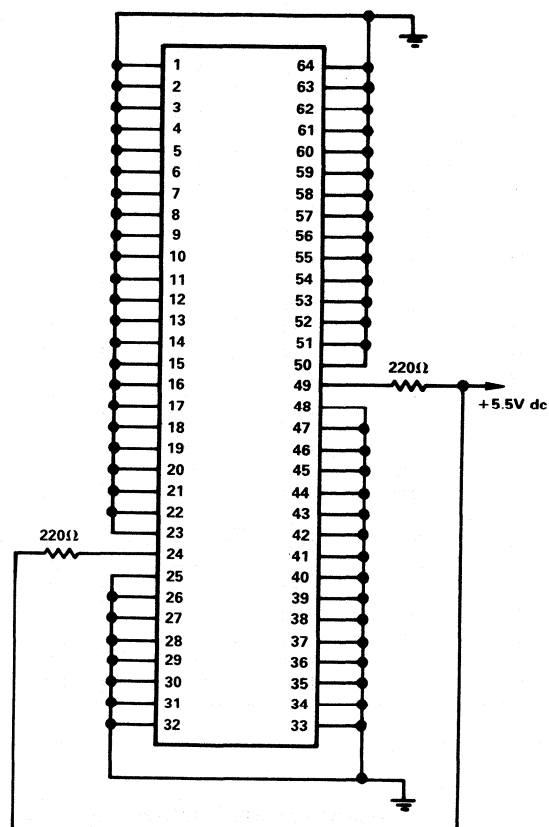
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1009AG Life Test and Burn-In Circuit



ADSP-1009AE Life Test and Burn-In Circuit



ADSP-1009AD Life Test and Burn-In Circuit

REV. E

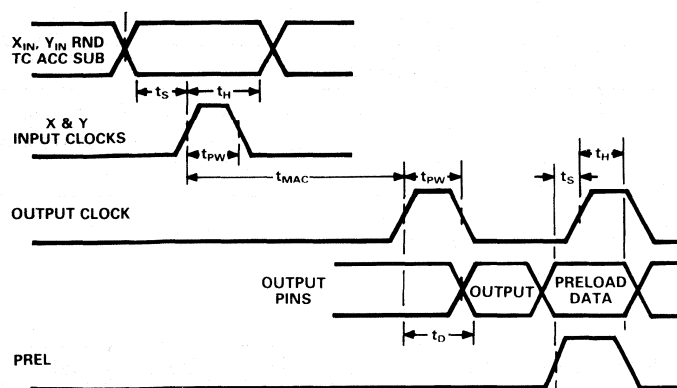


Figure 1. ADSP-1009A Timing Diagram

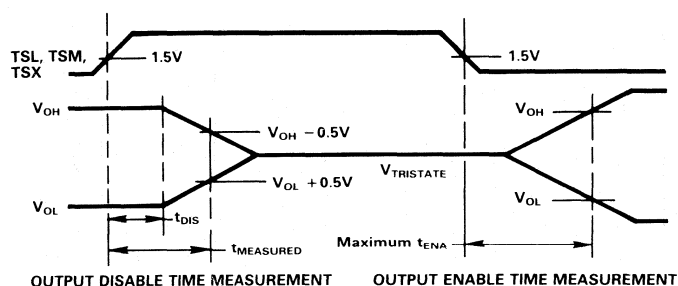


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

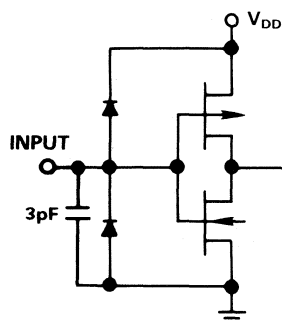


Figure 3. Equivalent Input Circuit

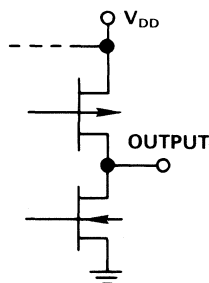


Figure 4. Equivalent Output Circuit

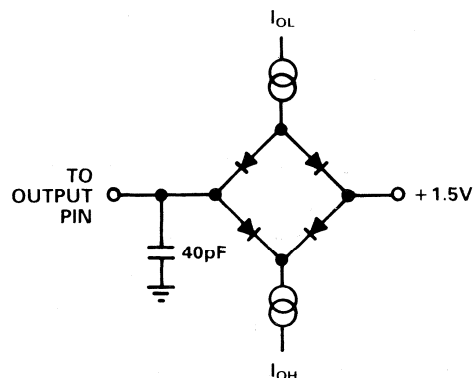


Figure 5. Normal Load Circuit for AC Measurements

ACC	SUB	Function
1	1	$\text{Accumulator}_t = X_t \cdot Y_t - \text{Accumulator}_{t-1}$
1	0	$\text{Accumulator}_t = X_t \cdot Y_t + \text{Accumulator}_{t-1}$
0	X	$\text{Accumulator}_t = X_t \cdot Y_t$

Table 2. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:

Z = Output buffers at high impedance (output disabled)

Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.

Preload = Output buffers at high impedance, or output disabled.

Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table 3. Preload Truth Table

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit digital multiplier/accumulator integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	ADSP-1010AS(X)/883B
–2	ADSP-1010AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
E	E-68A	68-Contact LCC
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1010A – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –1 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	80	100	100			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	35	40	40			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay*	t _D	–1, 2	30			40	40	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t _{ENA}	–1, 2	25			35	35	Notes 2 and 3	ns max
Three-State Disable* (High Z to High or Low)	t _{DIS}	–1, 2	25			35	35	Notes 2 and 3	ns max
Input Setup Time*	t _S	–1, 2	15			20	20	Note 2	ns min
Clock Pulse Width	t _{PW}	–1, 2	15			15	15	Note 2	ns min
Input Hold Time	t _H	–1, 2	3			3	3	Note 2	ns min
Multiply/Accumulate Time*	t _{MAC}	–1	85			100	100	Note 2	ns max
		–2	75			90	90		

NOTES

*Indicates that a limit for this parameter has changed from REV. D.

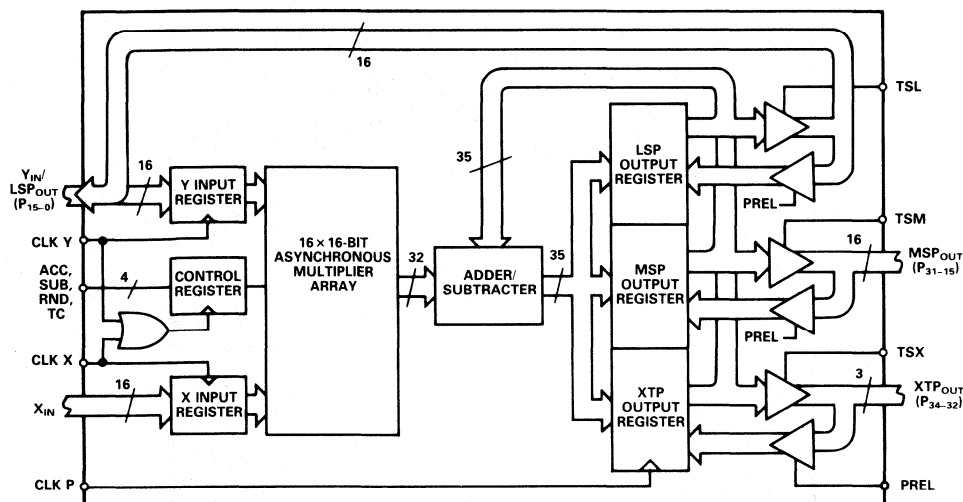
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +0.3 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



PIN ASSIGNMENTS

D-64A Package

PIN	FUNCTION	PIN	FUNCTION
1	X6	33	P24
2	X5	34	P25
3	X4	35	P26
4	X3	36	P27
5	X2	37	P28
6	X1	38	P29
7	X0	39	P30
8	Y0, P0	40	P31
9	Y1, P1	41	P32
10	Y2, P2	42	P33
11	Y3, P3	43	P34
12	Y4, P4	44	CLK P
13	Y5, P5	45	TSM
14	Y6, P6	46	PREL
15	Y7, P7	47	TSX
16	GND	48	TC
17	Y8, P8	49	V _{DD}
18	Y9, P9	50	CLK Y
19	Y10, P10	51	CLK X
20	Y11, P11	52	ACC
21	Y12, P12	53	SUB
22	Y13, P13	54	RND
23	Y14, P14	55	TSL
24	Y15, P15	56	X15
25	P16	57	X14
26	P17	58	X13
27	P18	59	X12
28	P19	60	X11
29	P20	61	X10
30	P21	62	X9
31	P22	63	X8
32	P23	64	X7

G-68A Package

PIN	FUNCTION	PIN	FUNCTION
1	Y1, P1	35	P32
2	Y2, P2	36	P33
3	Y3, P3	37	P34
4	Y4, P4	38	CLK P
5	Y5, P5	39	TSM
6	Y6, P6	40	PREL
7	Y7, P7	41	TSX
8	GND	42	TC
9	Y8, P8	43	V _{DD}
10	Y9, P9	44	CLK Y
11	Y10, P10	45	CLK X
12	Y11, P11	46	ACC
13	Y12, P12	47	SUB
14	Y13, P13	48	RND
15	Y14, P14	49	TSL
16	Y15, P15	50	X15
17	N/C	51	N/C
18	P16	52	X14
19	P17	53	X13
20	P18	54	X12
21	P19	55	X11
22	P20	56	X10
23	P21	57	X9
24	P22	58	X8
25	P23	59	X7
26	P24	60	X6
27	P25	61	X5
28	P26	62	X4
29	P27	63	X3
30	P28	64	X2
31	P29	65	X1
32	P30	66	X0
33	P31	67	Y0, P0
34	N/C	68	N/C

E-68A Package

PIN	FUNCTION	PIN	FUNCTION
1	X6	35	P24
2	X5	36	P25
3	X4	37	P26
4	X3	38	P27
5	X2	39	P28
6	X1	40	P29
7	X0	41	P30
8	Y0, P0	42	P31
9	N/C	43	N/C
10	Y1, P1	44	P32
11	Y2, P2	45	P33
12	Y3, P3	46	P34
13	Y4, P4	47	CLK P
14	Y5, P5	48	TSM
15	Y6, P6	49	PREL
16	Y7, P7	50	TSX
17	GND	51	TC
18	Y8, P8	52	V _{DD}
19	Y9, P9	53	CLK Y
20	Y10, P10	54	CLK X
21	Y11, P11	55	ACC
22	Y12, P12	56	SUB
23	Y13, P13	57	RND
24	Y14, P14	58	TSL
25	Y15, P15	59	X15
26	N/C	60	N/C
27	P16	61	X14
28	P17	62	X13
29	P18	63	X12
30	P19	64	X11
31	P20	65	X10
32	P21	66	X9
33	P22	67	X8
34	P23	68	X7

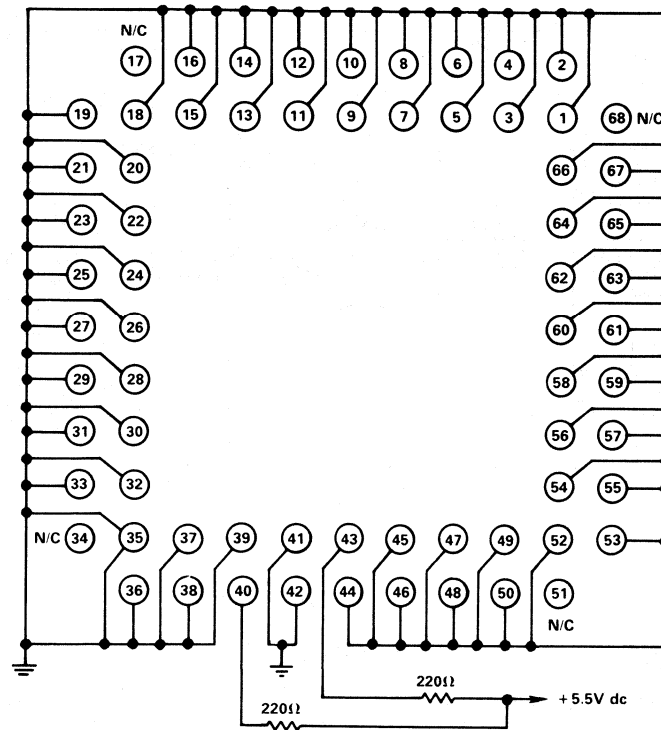
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

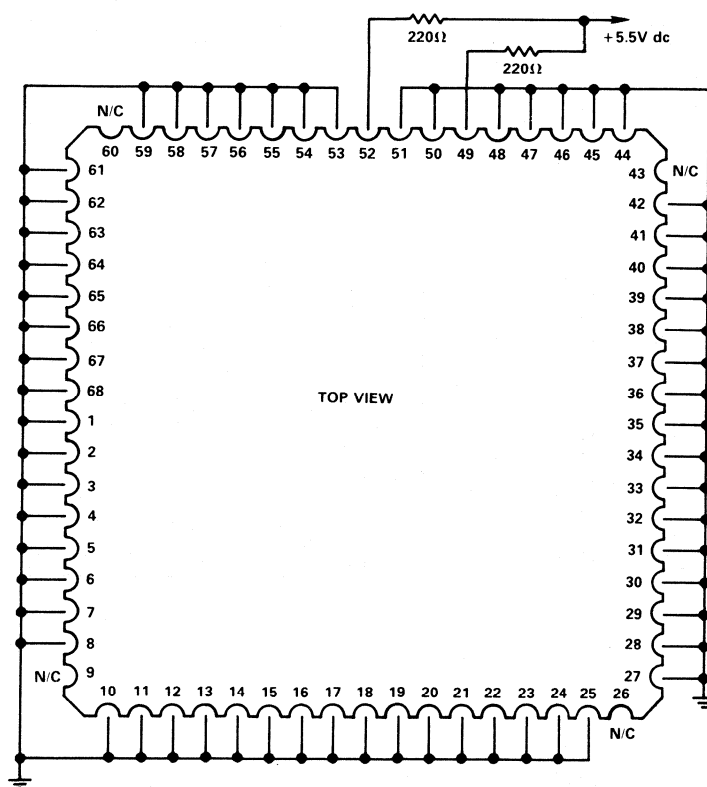
ADSP-1010A

4.2.1 Life Test/Burn-In Circuit.

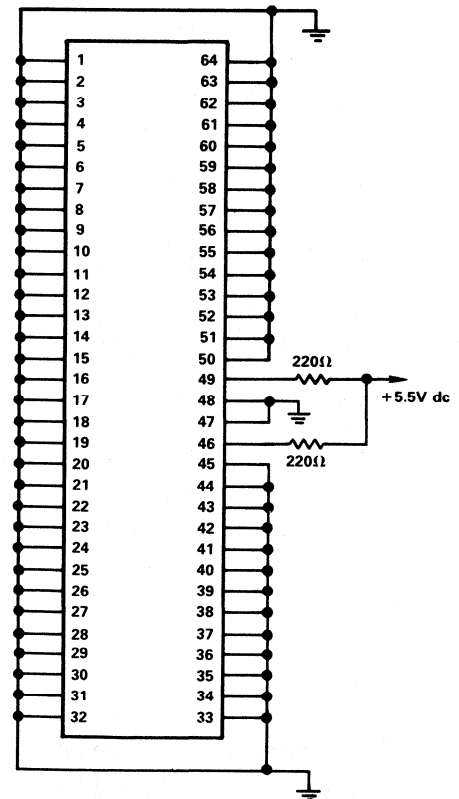
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1010AG Life Test and Burn-In Circuit



ADSP-1010AE Life Test and Burn-In Circuit



ADSP-1010AD Life Test and Burn-In Circuit

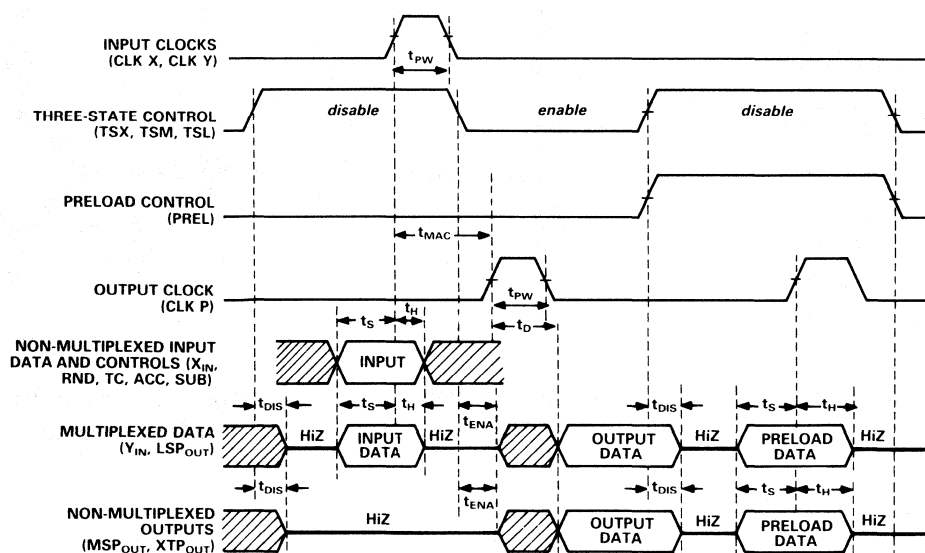


Figure 1. ADSP-1010A Timing Diagram

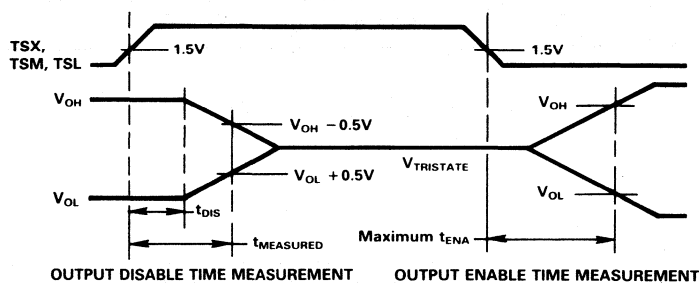


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

ADSP-1010A

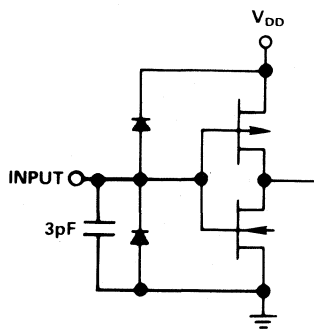


Figure 3. Equivalent Input Circuit

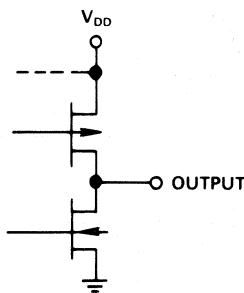


Figure 4. Equivalent Output Circuit

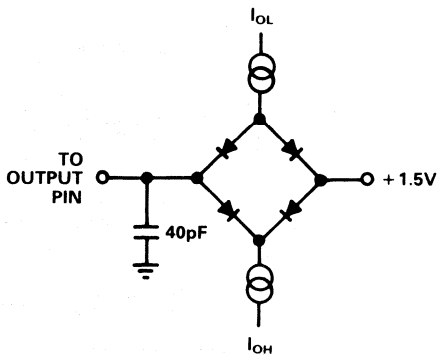


Figure 5. Normal Load Circuit for AC Measurements

ACC	SUB	Function
1	1	$\text{Accumulator}_t = X_t \cdot Y_t - \text{Accumulator}_{t-1}$
1	0	$\text{Accumulator}_t = X_t \cdot Y_t + \text{Accumulator}_{t-1}$
0	X	$\text{Accumulator}_t = X_t \cdot Y_t$

Table 2. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:
Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance, or output disabled.
Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table 3. Preload Truth Table

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit digital multiplier/accumulator integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	ADSP-1010BS(X)/883B
–2	ADSP-1010BT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1010B – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –1 mA	V min
Digital Output Low Voltage	V _{OL}	–1, 2	0.4	0.4	0.4			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IN} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IN} = max (High Z)	μA max
Supply Current	I _{DD1}	–1, 2	110	125	125			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	35	40	40			V _{DD} = max All V _{IN} = 2.4 V	
Output Delay	t _D	–1, 2	25			30	30	Note 2	ns max
Three-State Enable (High Z to High or Low)	t _{ENA}	–1, 2	25			30	30	Notes 2 and 3	ns max
Three-State Disable (High Z to High or Low)	t _{DIS}	–1, 2	25			30	30	Notes 2 and 3	ns max
Input Setup Time	t _S	–1, 2	15			20	20	Note 2	ns min
Clock Pulse Width	t _{PW}	–1, 2	15			15	15	Note 2	ns min
Input Hold Time	t _H	–1, 2	3			3	3	Note 2	ns min
Multiply/Accumulate Time	t _{MAC}	–1	55			65	65	Note 2	ns max
		–2	45			55	55		

NOTES

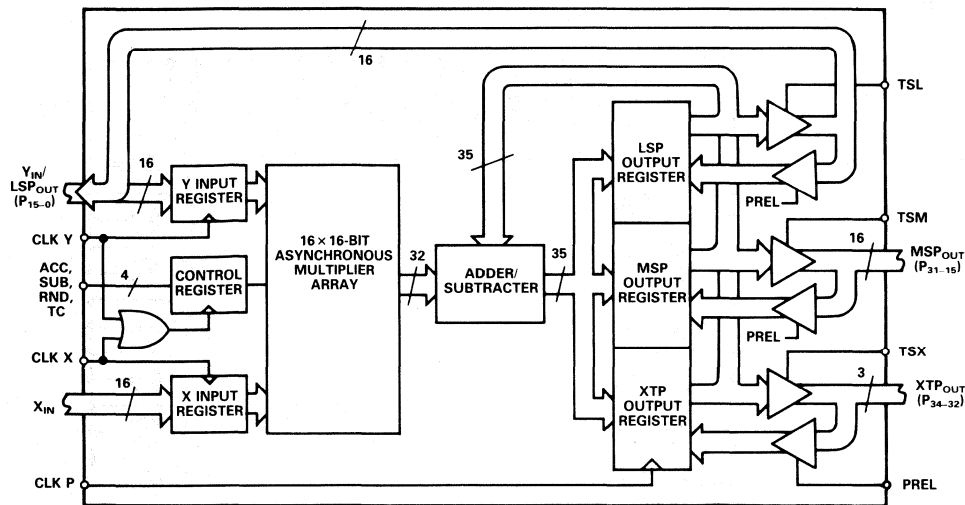
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

D-64A Package

PIN	FUNCTION	PIN	FUNCTION
1	X6	33	P24
2	X5	34	P25
3	X4	35	P26
4	X3	36	P27
5	X2	37	P28
6	X1	38	P29
7	X0	39	P30
8	Y0, P0	40	P31
9	Y1, P1	41	P32
10	Y2, P2	42	P33
11	Y3, P3	43	P34
12	Y4, P4	44	CLK P
13	Y5, P5	45	TSM
14	Y6, P6	46	PREL
15	Y7, P7	47	TSX
16	GND	48	TC
17	Y8, P8	49	V _{DD}
18	Y9, P9	50	CLK Y
19	Y10, P10	51	CLK X
20	Y11, P11	52	ACC
21	Y12, P12	53	SUB
22	Y13, P13	54	RND
23	Y14, P14	55	TSL
24	Y15, P15	56	X15
25	P16	57	X14
26	P17	58	X13
27	P18	59	X12
28	P19	60	X11
29	P20	61	X10
30	P21	62	X9
31	P22	63	X8
32	P23	64	X7

G-68A Package

PIN	FUNCTION	PIN	FUNCTION
1	Y1, P1	35	P32
2	Y2, P2	36	P33
3	Y3, P3	37	P34
4	Y4, P4	38	CLK P
5	Y5, P5	39	TSM
6	Y6, P6	40	PREL
7	Y7, P7	41	TSX
8	GND	42	TC
9	Y8, P8	43	V _{DD}
10	Y9, P9	44	CLK Y
11	Y10, P10	45	CLK X
12	Y11, P11	46	ACC
13	Y12, P12	47	SUB
14	Y13, P13	48	RND
15	Y14, P14	49	TSL
16	Y15, P15	50	X15
17	N/C	51	N/C
18	P16	52	X14
19	P17	53	X13
20	P18	54	X12
21	P19	55	X11
22	P20	56	X10
23	P21	57	X9
24	P22	58	X8
25	P23	59	X7
26	P24	60	X6
27	P25	61	X5
28	P26	62	X4
29	P27	63	X3
30	P28	64	X2
31	P29	65	X1
32	P30	66	X0
33	P31	67	Y0, P0
34	N/C	68	N/C

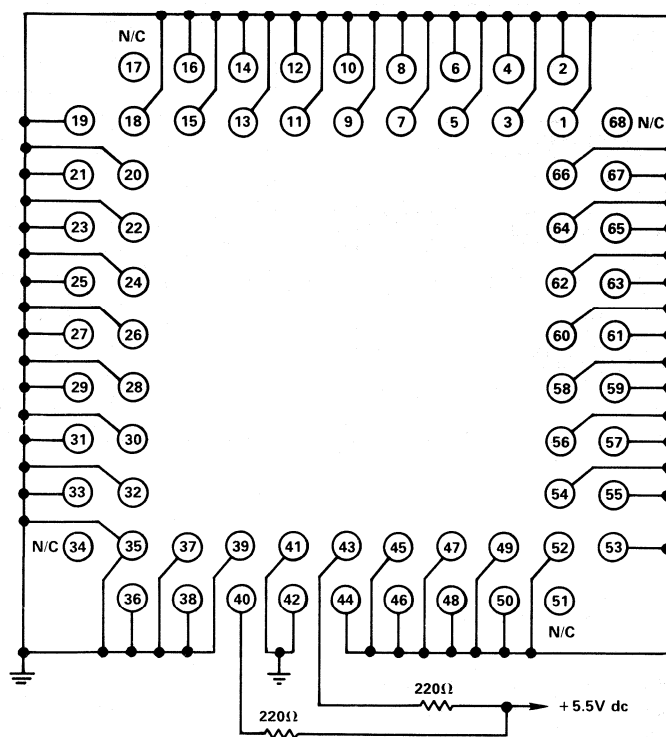
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

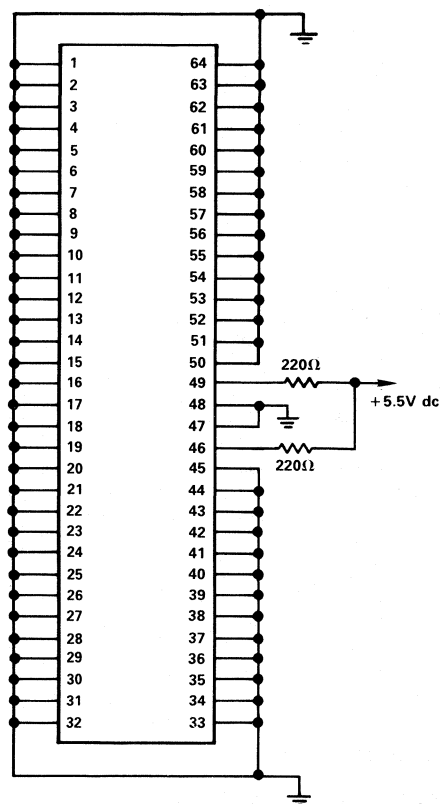
ADSP-1010B

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1010BG Life Test and Burn-In Circuit



ADSP-1010BD Life Test and Burn-In Circuit

REV. A

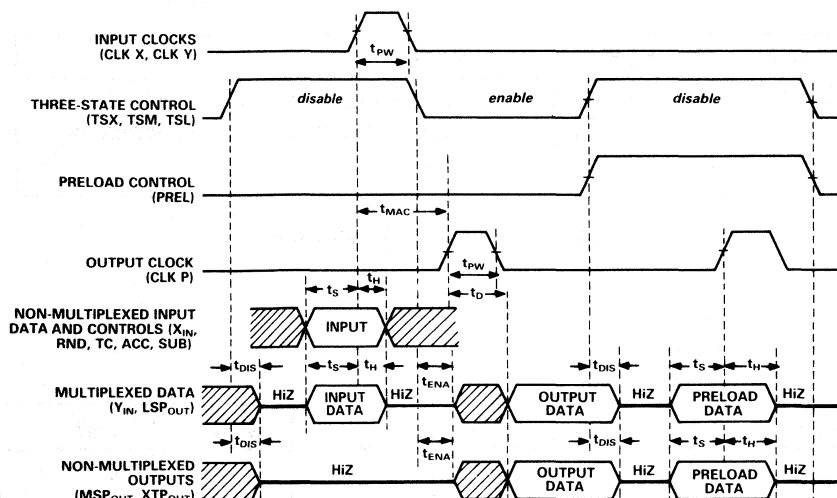


Figure 1. ADSP-1010B Timing Diagram

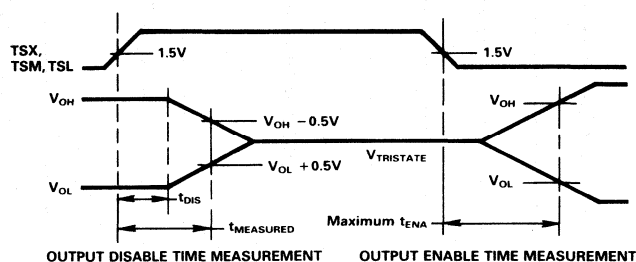


Figure 2. Three-State Disable and Enable

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

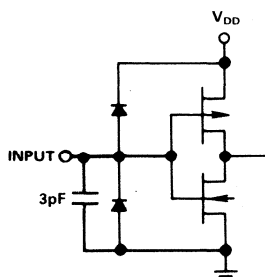


Figure 3. Equivalent Input Circuit

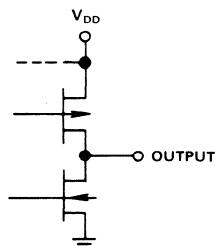


Figure 4. Equivalent Output Circuit

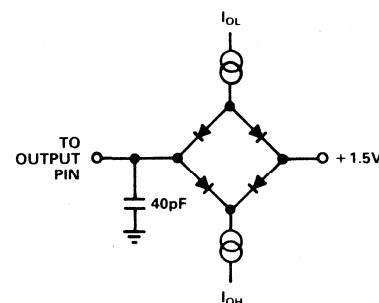


Figure 5. Normal Load Circuit for AC Measurements

ACC	SUB	Function
1	1	$\text{Accumulator}_t = X_t \cdot Y_t - \text{Accumulator}_{t-1}$
1	0	$\text{Accumulator}_t = X_t \cdot Y_t + \text{Accumulator}_{t-1}$
0	X	$\text{Accumulator}_t = X_t \cdot Y_t$

Table 2. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE

- Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance, or output disabled. Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

Table 3. Preload Truth Table

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12×12-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	ADSP-1012AS(X)/883B
–2	ADSP-1012AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
E	E-68A	68-Contact LCC
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for D-64A
 25°C/W for E-68A
 25°C/W for G-68A

ADSP-1012A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.2	2.2			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –1.0 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.5	0.5			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	60	70	70			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	30	35	35			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay*	t _D	–1, 2	30			40	40	Note 2	ns max
Three-State Enable* (High Z to Low)	t _{ENA}	–1, 2	30			35	35	Notes 2 and 3	ns max
Three-State Disable* (Low to High Z)	t _{DIS}	–1, 2	30			35	35	Notes 2 and 3	ns max
Clock Pulse Width	t _{PW}	–1, 2	20			25	25	Note 2	ns min
Input Setup Time*	t _S	–1, 2	15			20	20	Note 2	ns min
Input Hold Time	t _H	–1, 2	3			3	3	Note 2	ns min
Unclocked Multiply Time*	t _{MUC}	–1	105			125	125	Note 2	ns max
		–2	80			95	95		
Clocked Multiply Time*	t _{MC}	–1	75			90	90	Note 2	ns max
		–2	50			60	60		

NOTES

*Indicates that a limit for this parameter has changed from REV. D.

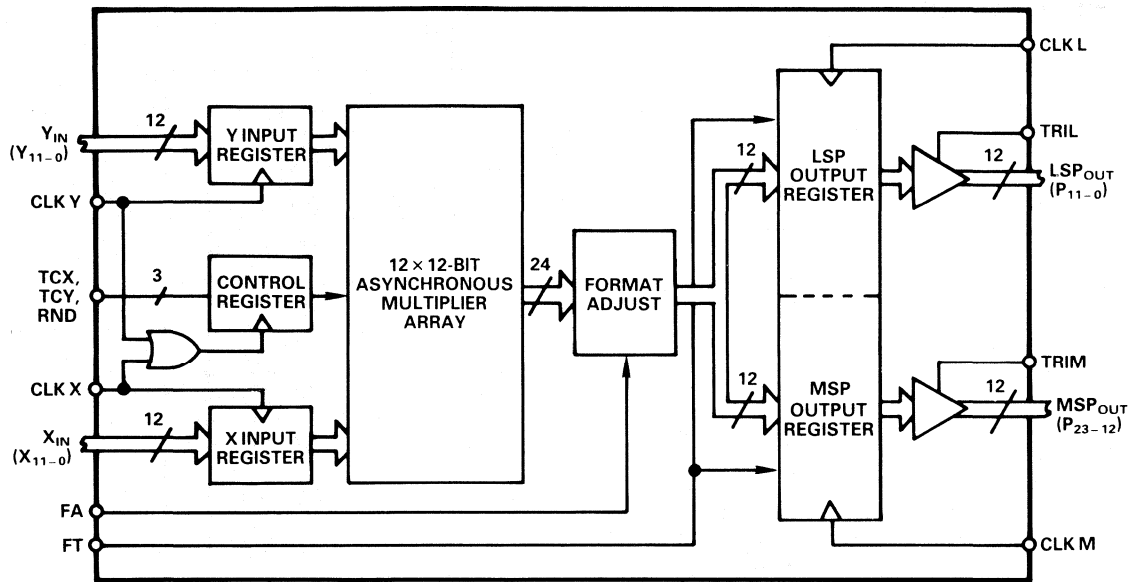
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

DIP

PIN	FUNCTION	PIN	FUNCTION
1	X7	33	P16
2	X6	34	P17
3	X5	35	P18
4	X4	36	P19
5	X3	37	P20
6	X2	38	P21
7	X1	39	P22
8	X0	40	P23
9	P0	41	TCY
10	P1	42	Y11
11	P2	43	Y10
12	P3	44	Y9
13	P4	45	Y8
14	P5	46	Y7
15	P6	47	Y6
16	P7	48	+V _{DD}
17	P8	49	+V _{DD}
18	P9	50	+V _{DD}
19	P10	51	Y5
20	P11	52	Y4
21	TRIL	53	Y3
22	TRIM	54	Y2
23	GND	55	Y1
24	GND	56	Y0
25	FT	57	TCX
26	FA	58	RND
27	CLK L	59	CLK Y
28	CLK M	60	CLK X
29	P12	61	X11
30	P13	62	X10
31	P14	63	X9
32	P15	64	X8

Pin Grid Array

PIN	FUNCTION	PIN	FUNCTION
1	P0	35	TCY
2	P1	36	Y11
3	P2	37	Y10
4	P3	38	Y9
5	P4	39	Y8
6	P5	40	Y7
7	P6	41	Y6
8	P7	42	V _{DD}
9	P8	43	V _{DD}
10	P9	44	V _{DD}
11	P10	45	Y5
12	P11	46	Y4
13	TRIL	47	Y3
14	TRIM	48	Y2
15	GND	49	Y1
16	GND	50	Y0
17	N/C	51	N/C
18	FT	52	TCX
19	FA	53	RND
20	CLK L	54	CLK Y
21	CLK M	55	CLK X
22	P12	56	X11
23	P13	57	X10
24	P14	58	X9
25	P15	59	X8
26	P16	60	X7
27	P17	61	X6
28	P18	62	X5
29	P19	63	X4
30	P20	64	X3
31	P21	65	X2
32	P22	66	X1
33	P23	67	X0
34	N/C	68	N/C

LCC

PIN	FUNCTION	PIN	FUNCTION
1	X7	35	P16
2	X6	36	P17
3	X5	37	P18
4	X4	38	P19
5	X3	39	P20
6	X2	40	P21
7	X1	41	P22
8	X0	42	P23
9	N/C	43	N/C
10	P0	44	TCY
11	P1	45	Y11
12	P2	46	Y10
13	P3	47	Y9
14	P4	48	Y8
15	P5	49	Y7
16	P6	50	Y6
17	P7	51	+V _{DD}
18	P8	52	+V _{DD}
19	P9	53	+V _{DD}
20	P10	54	Y5
21	P11	55	Y4
22	TRIL	56	Y3
23	TRIM	57	Y2
24	GND	58	Y1
25	GND	59	Y0
26	N/C	60	N/C
27	FT	61	TCX
28	FA	62	RND
29	CLK L	63	CLK Y
30	CLK M	64	CLK X
31	P12	65	X11
32	P13	66	X10
33	P14	67	X9
34	P15	68	X8

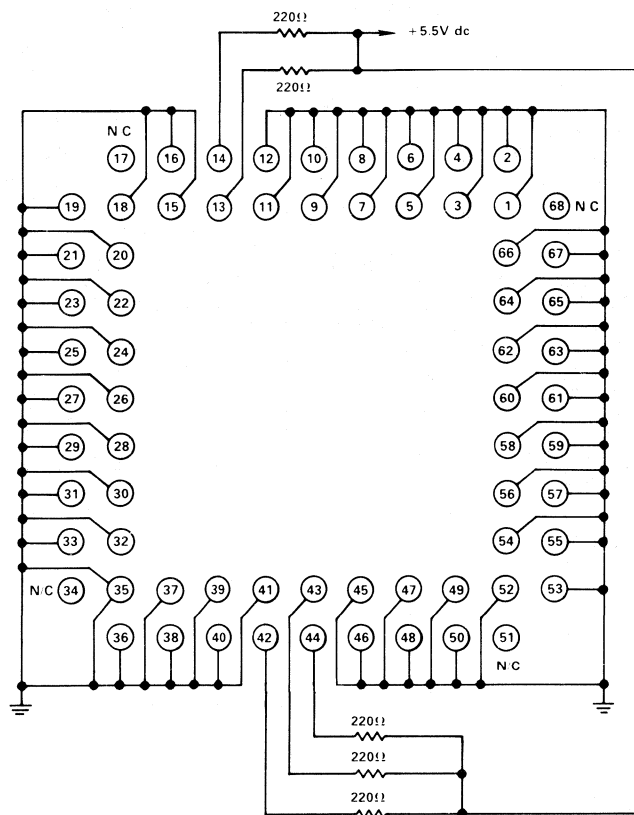
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

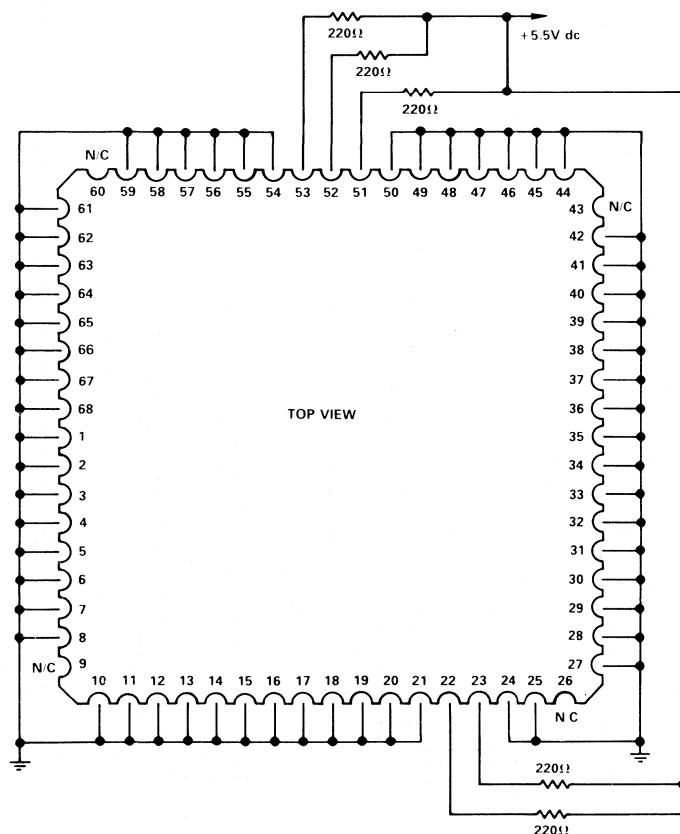
ADSP-1012A

4.2.1 Life Test/Burn-In Circuit.

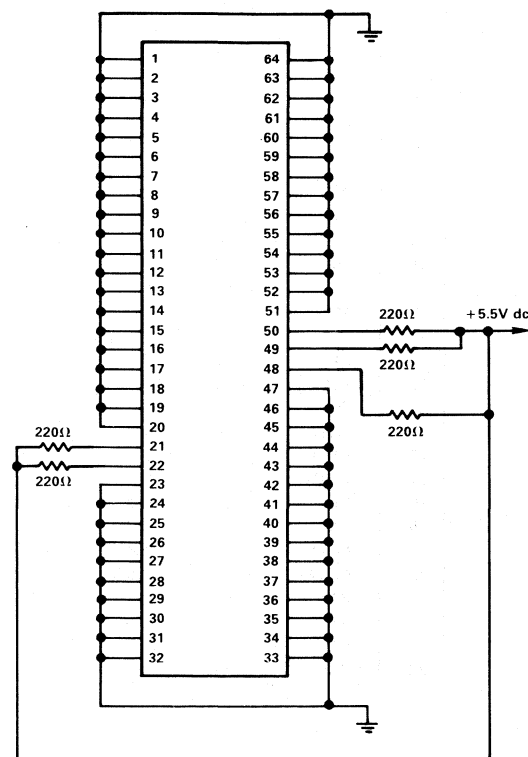
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1012AG Life Test and Burn-In Circuit



ADSP-1012AE Life Test and Burn-In Circuit



ADSP-1012AD Life Test and Burn-In Circuit

REV. E

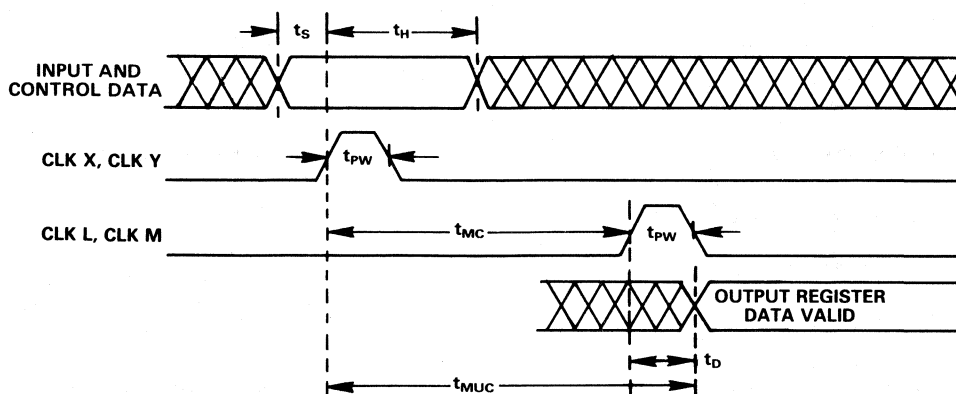


Figure 1. ADSP-1012A Timing Diagram

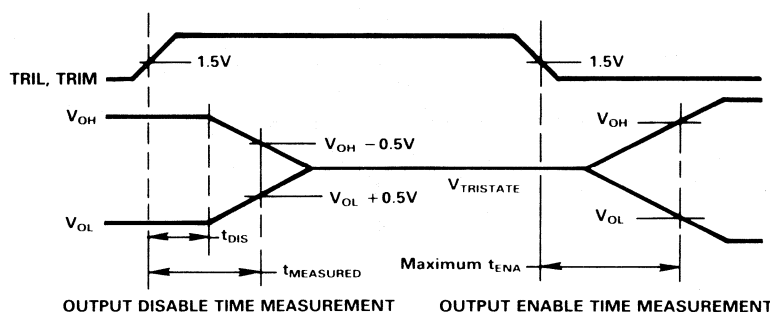


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

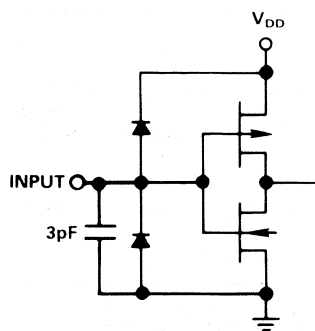


Figure 3. Equivalent Input Circuit

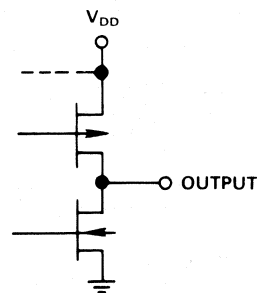


Figure 4. Equivalent Output Circuit

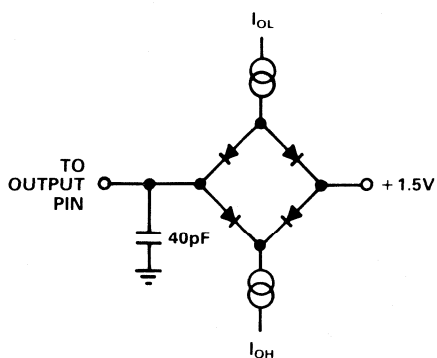


Figure 5. Normal Load Circuit for AC Measurements

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
–1	ADSP-1016AS(X)/883B
–2	ADSP-1016AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
E	E-68A	68-Contact LCC
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1016A – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –0.4 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	45	55	55			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	35	40	40			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay*	t _D	–1, 2	20			35	35	Note 2	ns max
Three-State Enable* (High Z to Low)	t _{ENA}	–1, 2	20			35	35	Notes 2 and 3	ns max
Three-State Disable* (Low to High Z)	t _{DIS}	–1, 2	20			35	35	Notes 2 and 3	ns max
Clock Pulse Width	t _{PW}	–1, 2	15			15	15	Note 2	ns min
Input Data Setup Time*	t _{DS}	–1, 2	25			25	25	Note 2	ns min
Input Control Setup Time*	t _{CS}	–1, 2	30			30	30	Notes 2 and 3	ns min
Input Hold Time	t _H	–1, 2	2			2	2	Note 2	ns min
Unclocked Multiply Time*	t _{MUC}	–1	105			120	120	Note 2	ns max
		–2	90			105	105		
Clocked Multiply Time*	t _{MC}	–1	85			95	95	Note 2	ns max
		–2	70			80	80		

NOTES

*Indicates that a limit for this parameter has changed from REV. D.

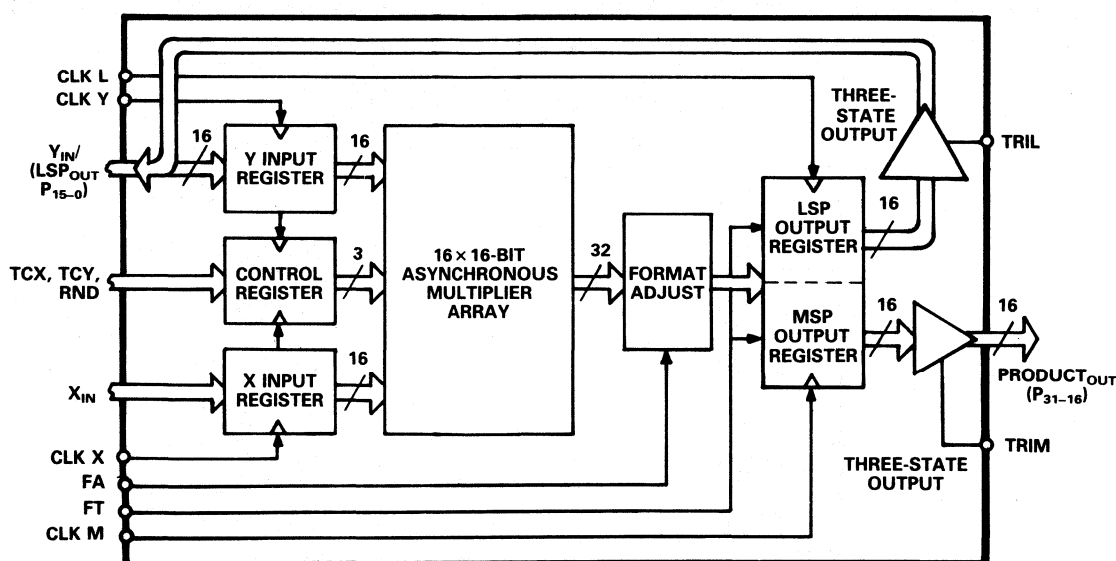
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Functional Block Diagram

Pin Assignments

PIN NO.	FUNCTION			PIN NO.	FUNCTION		
	DIP	LCC	PIN-GRID		DIP	LCC	PIN-GRID
1	X4	X4	P0, Y0	35	P26	P24	CLK M
2	X3	X3	P1, Y1	36	P27	P25	TRIM
3	X2	X2	P2, Y2	37	P28	P26	FA
4	X1	X1	P3, Y3	38	P29	P27	FT
5	X0	X0	P4, Y4	39	P30	P28	GND
6	TRIL	TRIL	P5, Y5	40	P31	P29	GND
7	CLK L	CLK L	P6, Y6	41	CLK M	P30	GND
8	CLK Y	CLK Y	P7, Y7	42	TRIM	P31	V _{DD}
9	P0, Y0	N/C	P8, Y8	43	FA	N/C	V _{DD}
10	P1, Y1	P0, Y0	P9, Y9	44	FT	CLK M	TCY
11	P2, Y2	P1, Y1	P10, Y10	45	GND	TRIM	TCX
12	P3, Y3	P2, Y2	P11, Y11	46	GND	FA	RND
13	P4, Y4	P3, Y3	P12, Y12	47	GND	FT	CLK X
14	P5, Y5	P4, Y4	P13, Y13	48	V _{DD}	GND	X15
15	P6, Y6	P5, Y5	P14, Y14	49	V _{DD}	GND	X14
16	P7, Y7	P6, Y6	P15, Y15	50	TCY	GND	X13
17	P8, Y8	P7, Y7	N/C	51	TCX	V _{DD}	N/C
18	P9, Y9	P8, Y8	P16	52	RND	V _{DD}	X12
19	P10, Y10	P9, Y9	P17	53	CLK X	TCY	X11
20	P11, Y11	P10, Y10	P18	54	X15	TCX	X10
21	P12, Y12	P11, Y11	P19	55	X14	RND	X9
22	P13, Y13	P12, Y12	P20	56	X13	CLK X	X8
23	P14, Y14	P13, Y13	P21	57	X12	X15	X7
24	P15, Y15	P14, Y14	P22	58	X11	X14	X6
25	P16	P15, Y15	P23	59	X10	X13	X5
26	P17	N/C	P24	60	X9	N/C	X4
27	P18	P16	P25	61	X8	X12	X3
28	P19	P17	P26	62	X7	X11	X2
29	P20	P18	P27	63	X6	X10	X1
30	P21	P19	P28	64	X5	X9	X0
31	P22	P20	P29	65	N/A	X8	TRIL
32	P23	P21	P30	66	N/A	X7	CLK L
33	P24	P22	P31	67	N/A	X6	CLK Y
34	P25	P23	N/C	68	N/A	X5	N/C

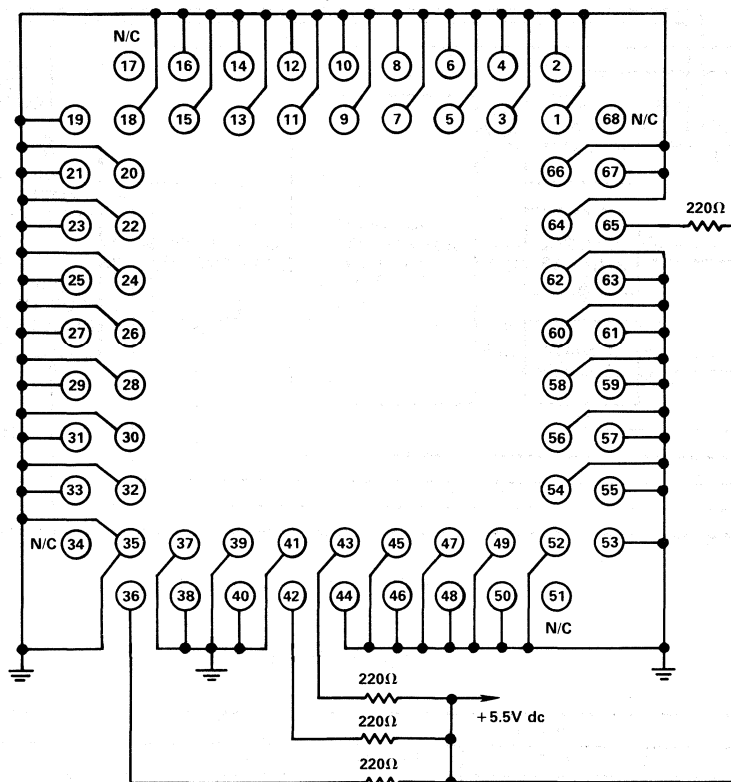
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

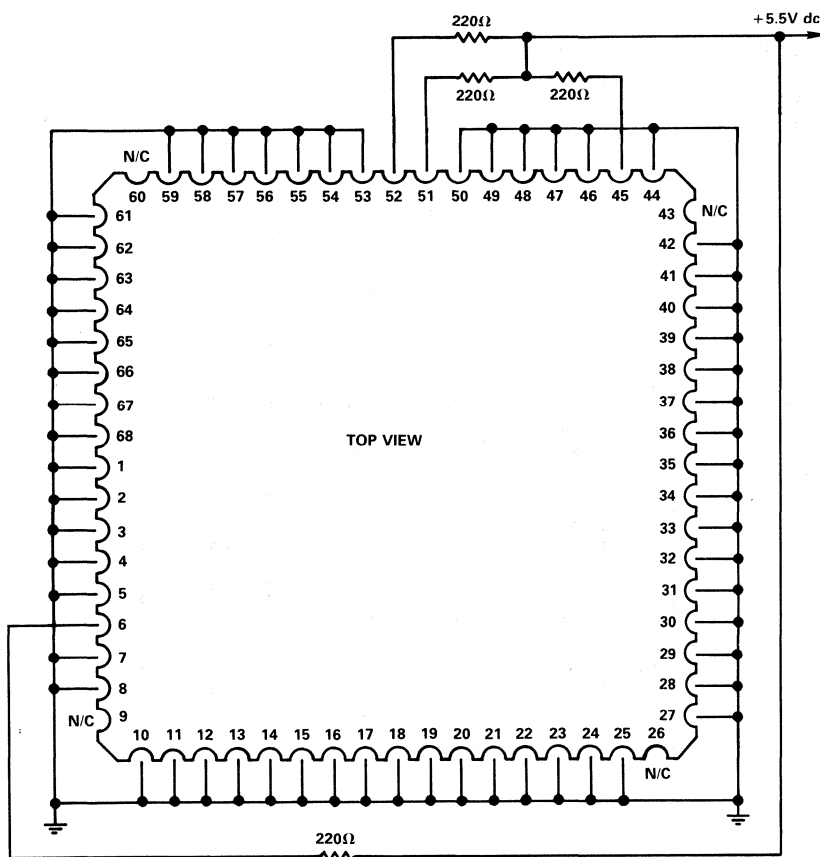
ADSP-1016A

4.2.1 Life Test/Burn-In Circuit.

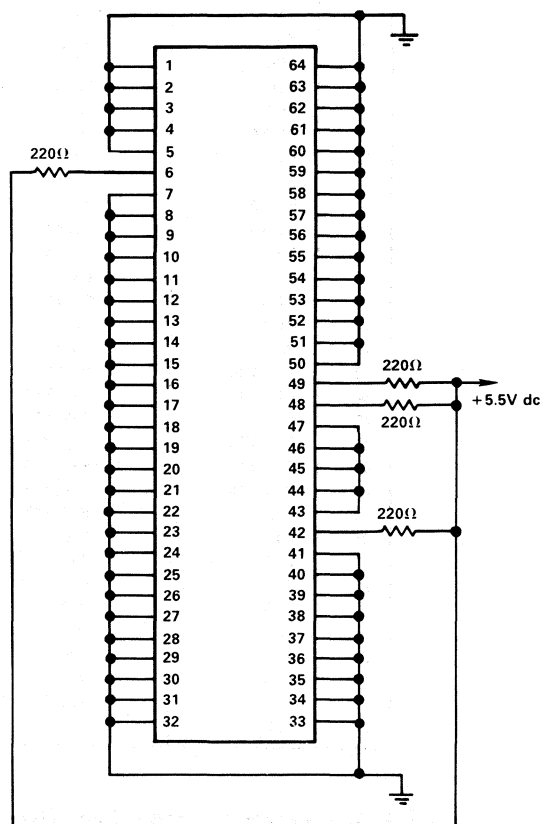
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1016AG Life Test and Burn-In Circuit



ADSP-1016AE Life Test and Burn-In Circuit



ADSP-1016AD Life Test and Burn-In Circuit

REV. E

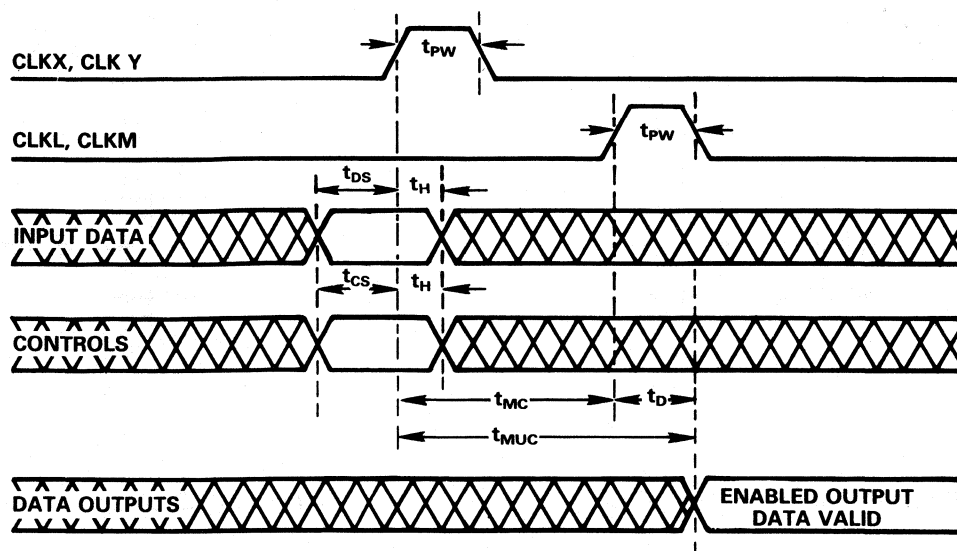


Figure 1. ADSP-1016A Timing Diagram

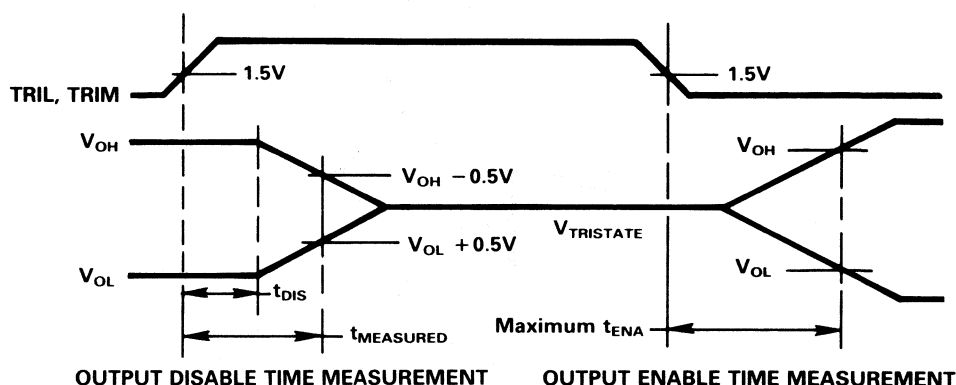


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

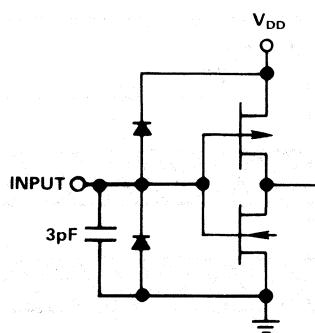


Figure 3. Equivalent Input Circuit

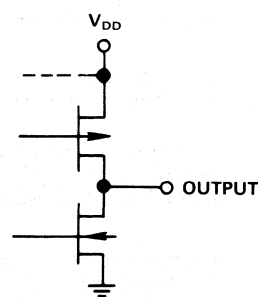


Figure 4. Equivalent Output Circuit

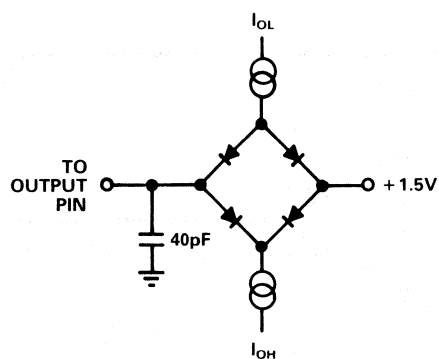


Figure 5. Normal Load Circuit for AC Measurements

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 24×24-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	ADSP-1024ASG/883B
–2	ADSP-1024ATG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-84A.

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1024A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.2	2.2	2.2			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –4.0 mA	V min
Digital Output Low Voltage	V _{OL}	–1, 2	0.6	0.6	0.6			V _{DD} = min I _{OL} = +4.0 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	75	90	90			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	35	40	40			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay*	t _D	–1, 2	30			40	40	Note 2	ns max
Three-State Enable* (High Z to Low)	t _{ENA}	–1	35			40	40	Notes 2 and 3	ns max
		–2	30			35	35		
Three-State Disable* (Low to High Z)	t _{DIS}	–1	35			40	40	Notes 2 and 3	ns max
		–2	30			35	35		
Clock Pulse Width	t _{PW}	–1, 2	15			15	15	Note 2	ns min
Input Setup Time*	t _S	–1	30			35	35	Note 2	ns min
		–2	25			30	30		
Input Hold Time	t _H	–1, 2	3			3	3	Note 2	ns min
Clock to OVF Valid*	t _{DOVF}	–1	30			40	40	Note 2	ns max
		–2	25			35	35		
Clock to NORM Valid*	t _{DNRM}	–1	30			40	40	Note 2	ns max
		–2	25			35	35		
Clocked Multiply Time*	t _{MC}	–1	120			150	150	Note 2	ns max
		–2	95			120	120		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

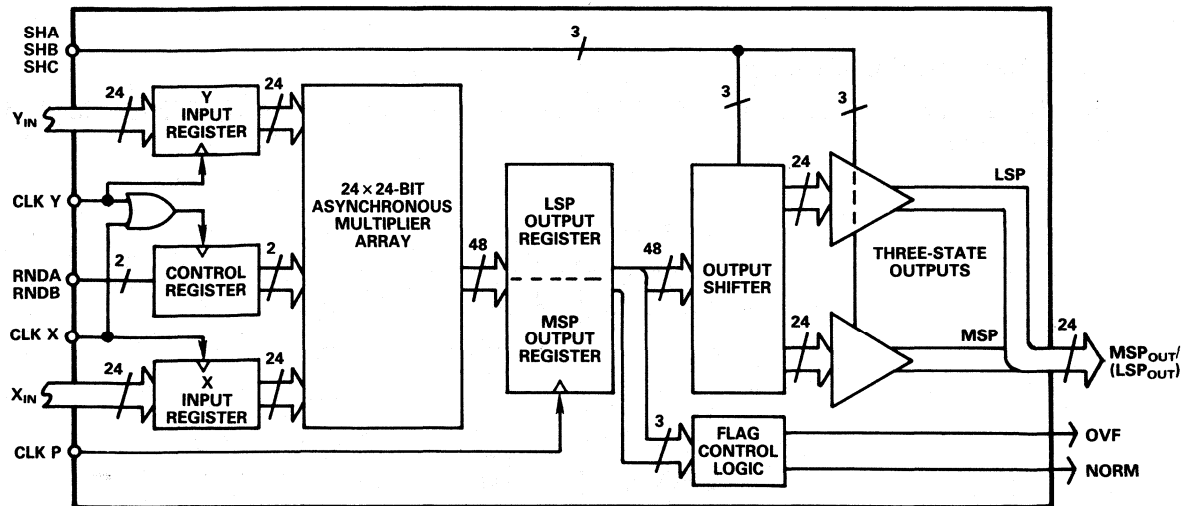
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

FUNCTION	PIN NO.	FUNCTION	PIN NO.
X20	C6	P16, P40	J6
X21	C5	P15, P39	L6
X22	A5	P14, P38	L7
X23	B5	P13, P37	K7
CLKX	A6	P12, P36	J7
CLKY	A4	P11, P35	L8
RNDB	B4	P10, P34	K8
RNDA	A3	P9, P33	L9
Y0	A2	P8, P32	L10
Y1	B3	P7, P31	K9
Y2	A1	P6, P30	L11
Y3	B2	P5, P29	K10
Y4	C2	P4, P28	J10
Y5	B1	P3, P27	K11
Y6	C1	P2, P26	J11
Y7	D2	P1, P25	H10
Y8	D1	P0, P24	H11
Y9	F2	SHA	G9
Y10	E2	SHB	G10
Y11	E1	SHC	G11
V _{DD}	E3	CLKP	F10
Y12	F3	GND	F9
Y13	F1	X0	E9
Y14	G1	X1	E11
Y15	G2	X2	E10
Y16	G3	X3	F11
Y17	H1	X4	D11
Y18	H2	X5	D10
Y19	J1	X6	C11
Y20	K1	X7	B11
Y21	J2	X8	C10
Y22	L1	X9	A11
Y23	K2	X10	B10
OVF	K3	X11	B9
NORM	L2	X12	A10
P23, P47	L3	X13	A9
P22, P46	K4	X14	B8
P21, P45	L4	X15	A8
P20, P44	K6	X16	C7
P19, P43	K5	X17	B7
P18, P42	L5	X18	A7
P17, P41	J5	X19	B6

ADSP-1024A

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

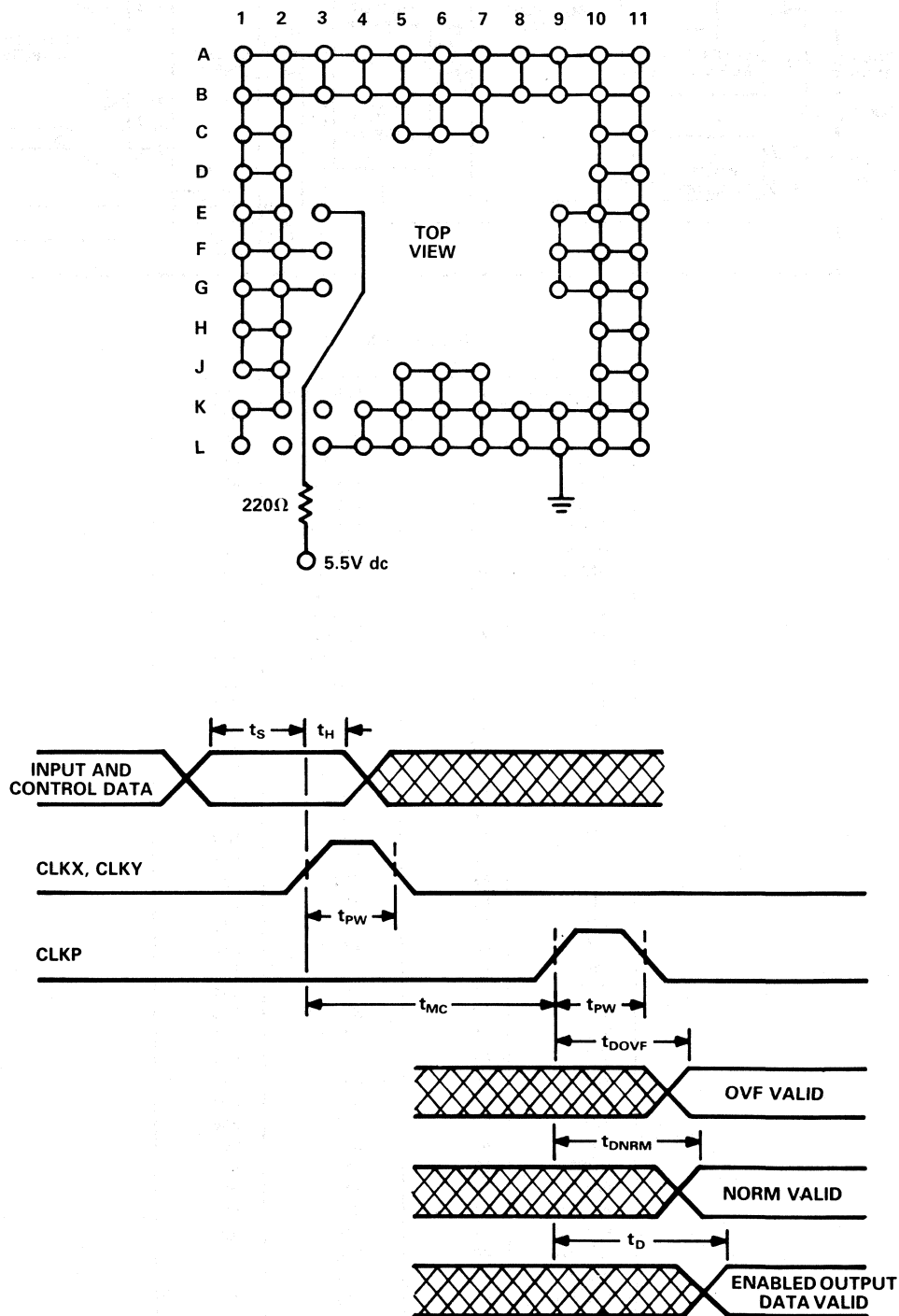


Figure 1. ADSP-1024A Timing Diagram

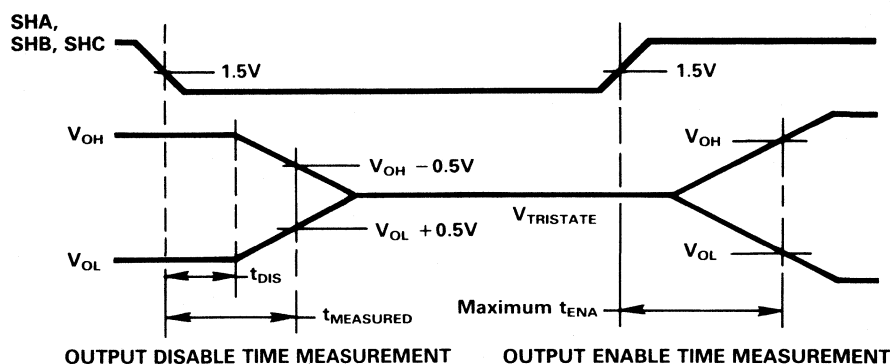


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

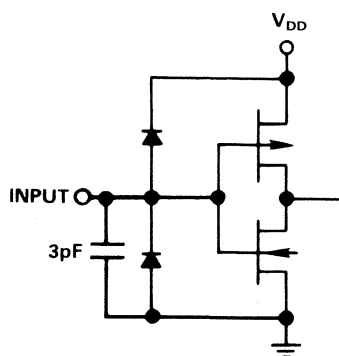


Figure 3. Equivalent Input Circuit

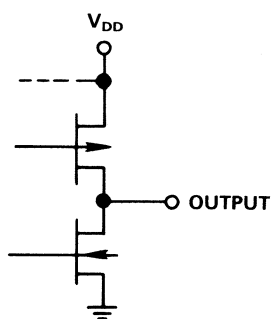


Figure 4. Equivalent Output Circuit

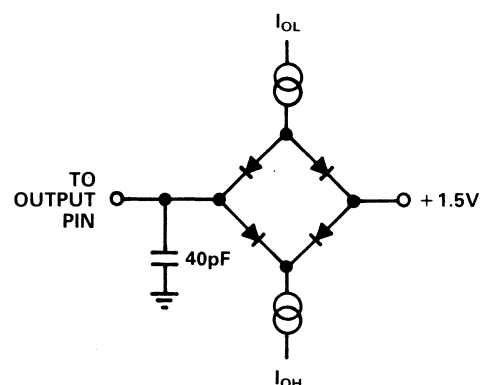


Figure 5. Normal Load Circuit for AC Measurements

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8×8-bit digital multiplier integrated circuit, with twos-complement data format.

1.2 Part Number.

The complete part numbers per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-1080ASD/883B
-2	ADSP-1080ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-40A.

1.3 Absolute Maximum Ratings.

Supply Voltage		-0.3 V to 7 V
Input Voltage		-0.3 V to V_{DD}
Output Voltage		-0.3 V to V_{DD}
Operating Temperature Range (Ambient)		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1080A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –1 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.6	0.6			V _{DD} = min I _{OH} = +4 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = 0 V (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	45	55	55			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	30	35	35			V _{DD} = max All V _{IN} = 2.4 V	mA max
Output Delay	t _D	–1, 2	25			30	30	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t _{ENA}	–1, 2	20			25	25	Notes 2 and 3	ns max
Three-State Disable* (High or Low to High Z)	t _{DIS}	–1, 2	20			25	25	Notes 2 and 3	ns max
Input Setup Time	t _S	–1, 2	20			20	20	Note 2	ns min
Clock Pulse Width	t _{PW}	–1, 2	15			25	25	Note 2	ns min
Input Hold Time	t _H	–1, 2	2			3	3	Note 2	ns min
Multiply Time*	t _{MC}	–1	45			55	55	Note 2	ns max
		–2	33			45	45		

NOTES

*Indicates that a limit for this parameter has changed from REV. D.

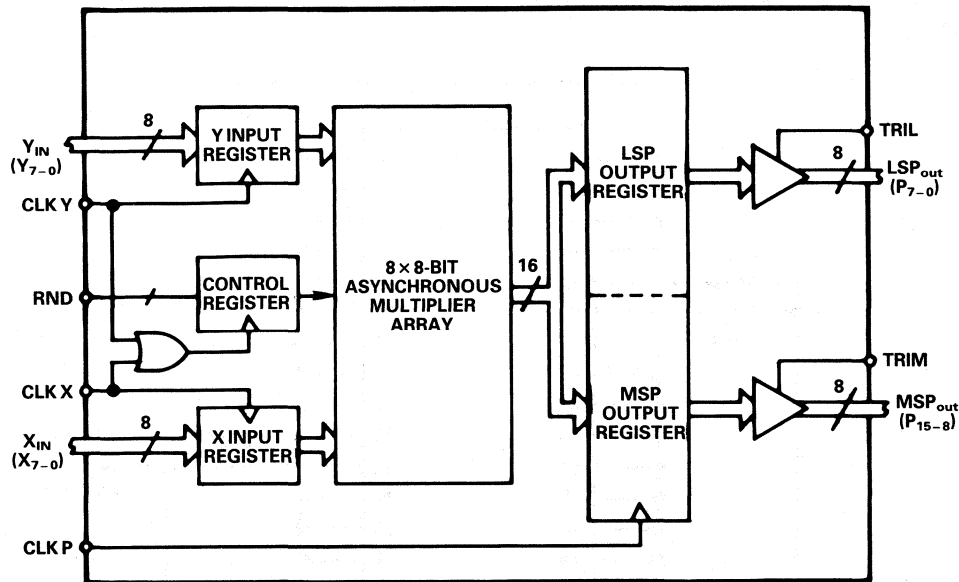
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	P10	21	X6
2	P9	22	X7 (MSB)
3	P8	23	CLK X
4	CLK P	24	CLK Y
5	TRIM	25	RND
6	TRIL	26	Y0
7	P7	27	Y1
8	P6	28	Y2
9	P5	29	Y3
10	P4	30	V _{DD}
11	P3	31	Y4
12	P2	32	GND
13	P1	33	Y5
14	P0	34	Y6
15	X0	35	Y7 (MSB)
16	X1	36	P15 (MSB)
17	X2	37	P14
18	X3	38	P13
19	X4	39	P12
20	X5	40	P11

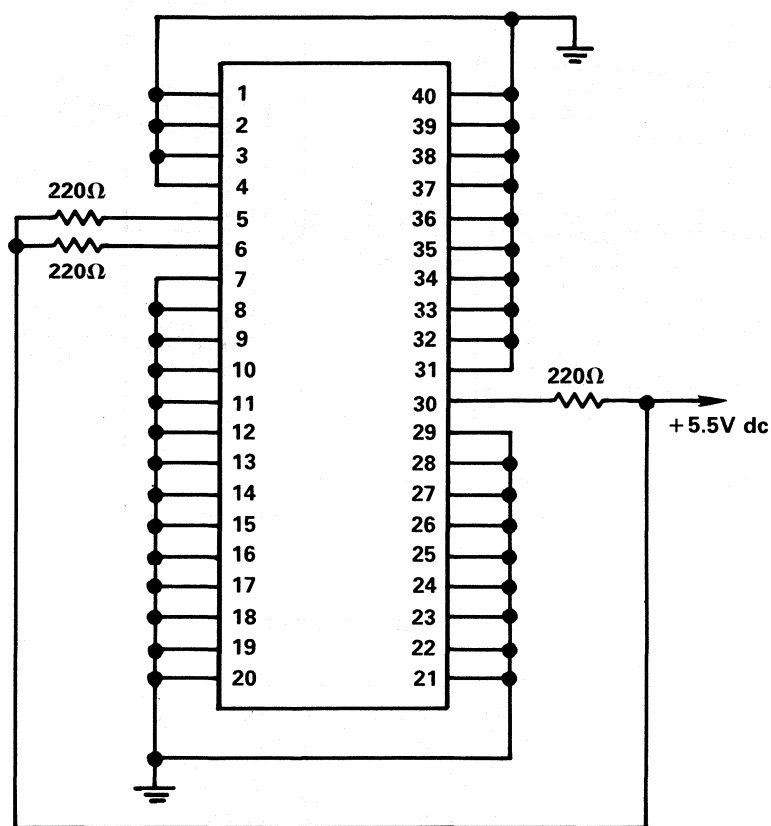
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

ADSP-1080A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1080AD Life Test and Burn-In Circuit

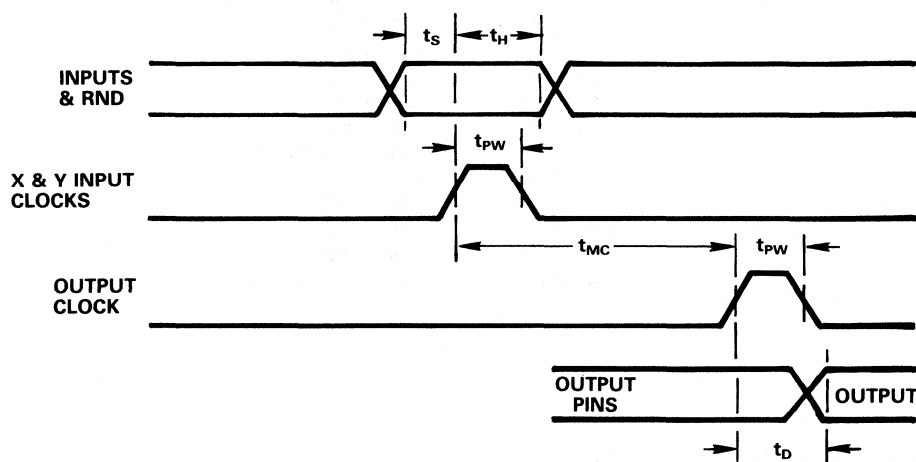


Figure 1. ADSP-1080A Timing Diagram

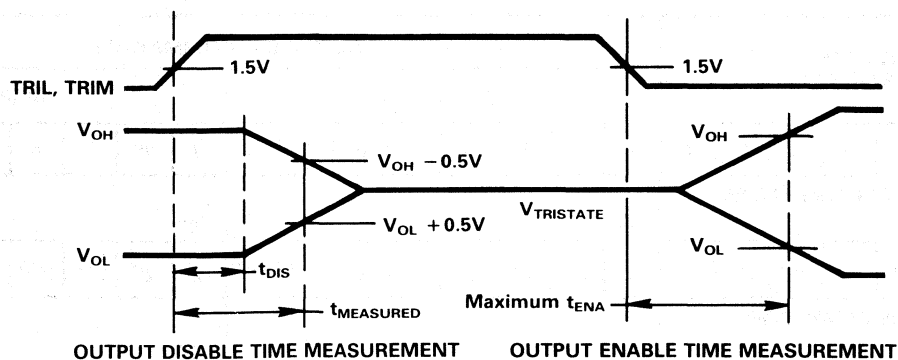


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as “data valid.” Maximum enable times are longest at the highest specified temperature.

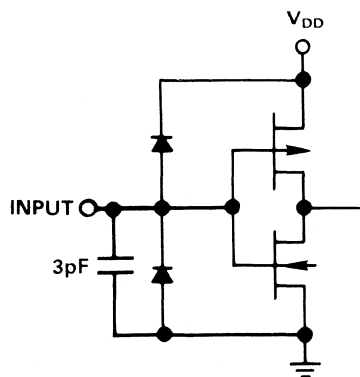


Figure 3. Equivalent Input Circuit

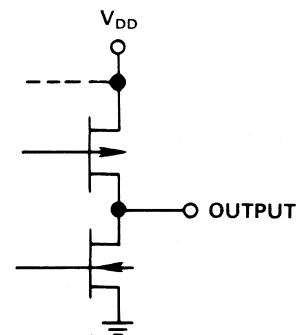


Figure 4. Equivalent Output Circuit

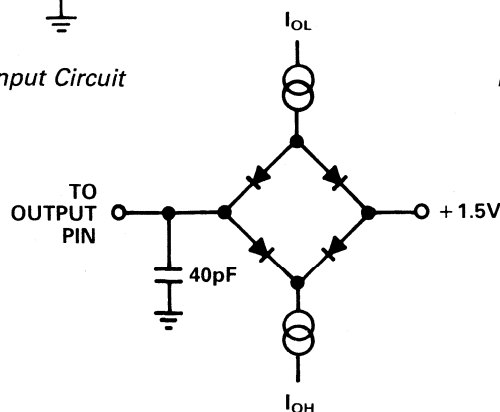


Figure 5. Normal Load Circuit for AC Measurements

ADSP-1080A

INPUT DATA FORMAT (X & Y)								OUTPUT DATA FORMATS (P)															
								MSP (P ₁₅₋₈)								LSP (P ₇₋₀)							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACTIONAL TWOS COMPLEMENT sign								sign								sign							
−2 ⁰	2 ^{−1}	2 ^{−2}	2 ^{−3}	2 ^{−4}	2 ^{−5}	2 ^{−6}	2 ^{−7}	−2 ⁰	2 ^{−1}	2 ^{−2}	2 ^{−3}	2 ^{−4}	2 ^{−5}	2 ^{−6}	2 ^{−7}	−2 ⁰	2 ^{−8}	2 ^{−9}	2 ^{−10}	2 ^{−11}	2 ^{−12}	2 ^{−13}	2 ^{−14}
INTEGER TWOS COMPLEMENT sign								sign								sign							
−2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	−2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	−2 ¹⁴	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰

Table 2. Data Formats

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8×8-bit digital multiplier integrated circuit, unsigned magnitude data format.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-1081ASD/883B
-2	ADSP-1081ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-40A.

1.3 Absolute Maximum Ratings.

Supply Voltage		-0.3 V to 7 V
Input Voltage		-0.3 V to V_{DD}
Output Voltage		-0.3 V to V_{DD}
Operating Temperature Range (Ambient)		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1081A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –1.0 mA	V min
Digital Output Low Voltage*	V _{OL}	–1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4.0 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = 0 V (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	45	55	55			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	–1, 2	30	35	35			V _{DD} = max All V _{IN} = 2.4 V	
Output Delay	t _D	–1, 2	25			30	30	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t _{ENA}	–1, 2	20			25	25	Notes 2 and 3	ns max
Three-State Disable* (High or Low to High Z)	t _{DIS}	–1, 2	20			25	25	Notes 2 and 3	ns max
Input Setup Time	t _S	–1, 2	20			20	20	Note 2	ns min
Clock Pulse Width	t _{PW}	–1, 2	15			15	15	Note 2	ns min
Input Hold Time	t _H	–1, 2	2			3	3	Note 2	ns min
Multiply Time*	t _{MC}	–1	45			55	55	Note 2	ns max
		–2	33			45	45		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

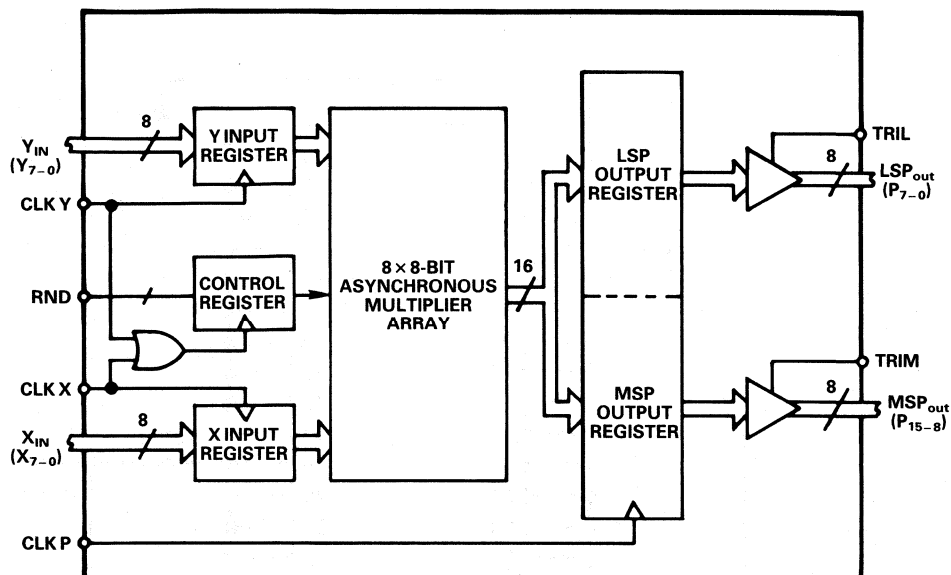
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	P10	21	X6
2	P9	22	X7 (MSB)
3	P8	23	CLK X
4	CLK P	24	CLK Y
5	TRIM	25	RND
6	TRIL	26	Y0
7	P7	27	Y1
8	P6	28	Y2
9	P5	29	Y3
10	P4	30	V _{DD}
11	P3	31	Y4
12	P2	32	GND
13	P1	33	Y5
14	P0	34	Y6
15	X0	35	Y7 (MSB)
16	X1	36	P15 (MSB)
17	X2	37	P14
18	X3	38	P13
19	X4	39	P12
20	X5	40	P11

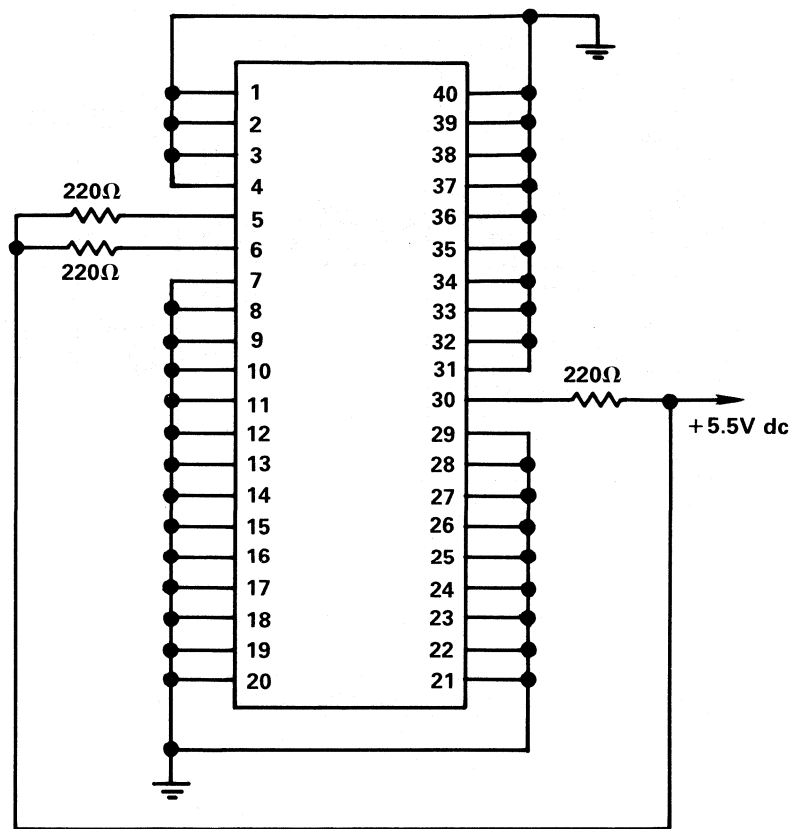
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

ADSP-1081A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1081AD Life Test and Burn-In Circuit

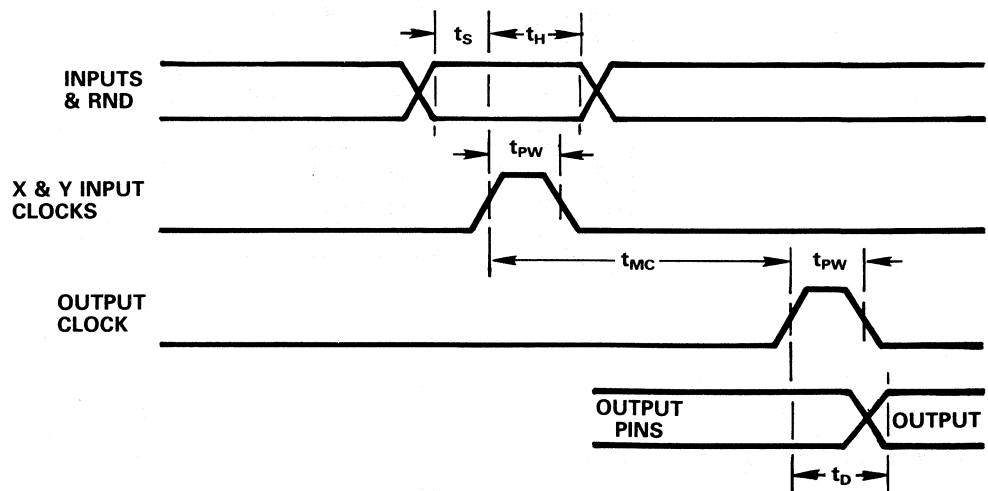


Figure 1. ADSP-1081A Timing Diagram

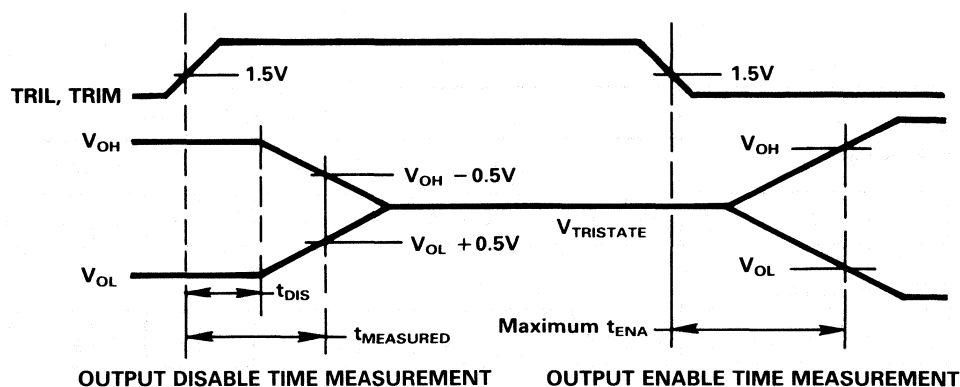


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as “data valid.” Maximum enable times are longest at the highest specified temperature.

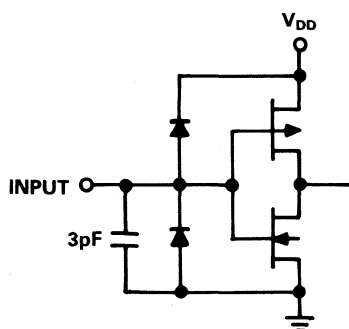


Figure 3. Equivalent Input Circuit

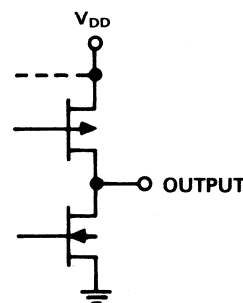


Figure 4. Equivalent Output Circuit

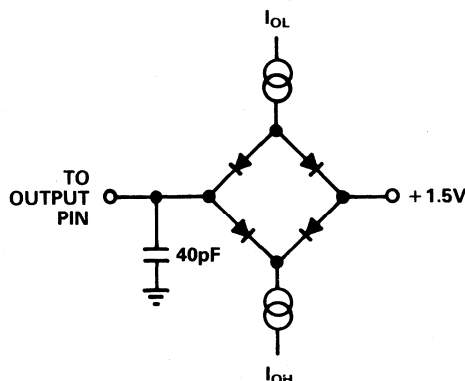


Figure 5. Normal Load Circuit for AC Measurements

X & Y INPUT DATA FORMAT								OUTPUT DATA FORMATS															
								MSP (P_{15-8})								LSP (P_{7-0})							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNSIGNED FRACTIONAL																							
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}
UNSIGNED INTEGER																							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table 2. Data Formats



16×16-Bit CMOS Single Port Multiplier/Accumulator

ADSP-1110A

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit multiplier/accumulator integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-1110AS(X)/883B
-2	ADSP-1110AT(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28	28-Contact LCC

1.3 Absolute Maximum Ratings.

Supply Voltage		-0.3 V to 7 V
Input Voltage		-0.3 V to V_{DD}
Output Voltage		-0.3 V to V_{DD}
Operating Temperature Range (Ambient)		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1110A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9, 10, 11	Test Condition ¹	Units
Digital Input High Voltage*	V _{IH}	-1, 2	2.0	2.2	2.2		V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8		V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	-1, 2	2.4	2.4	2.4		V _{DD} = min I _{OH} = -1 mA	V min
Digital Output Low Voltage*	V _{OL}	-1, 2	0.4	0.6	0.6		V _{DD} = min I _{OH} = +4 mA	V max
Digital Input High Current	I _{IH}	-1, 2	10	10	10		V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	-1, 2	10	10	10		V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage* Current Low	I _{OZL}	-1, 2	50	50	50		V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	-1, 2	50	50	50		V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	-1, 2	70	80	80		V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	-1, 2	35	40	40		V _{DD} = max All V _{IN} = 2.4 V	mA max
Clock Pulse Width	t _{PW}	-1, 2	15			15	Note 2	ns min
Input Control Hold Time	t _{CH}	-1, 2	5			6	Note 2	ns min
Input Data Setup Time	t _{DS}	-1, 2	15			15	Note 2	ns min
Clock Period*	t _{CLK}	-1	50			60	Note 2	ns min
		-2	42.5			50		
Input Control Setup Time	t _{CS}	-1	25			25	Note 2	ns min
		-2	20			20		
Input Data Hold Time*	t _{DH}	-1, 2	3			4	Note 2	ns min
Multiply/Accumulate Time*	t _{MAC}	-1	100			120	Note 2	ns max
		-2	85			100		
Control to Valid Output*	t _D	-1	30			30	Note 2	ns max
		-2	25			30		
Control to Valid Output* with Saturation	t _{DSAT}	-1	35			40	Note 2	ns max
		-2	32			35		
Output Driver Disable Time	t _{DIS}	-1, 2	25			25	Notes 2 and 3	ns max
Control to Overflow Flag*	t _O	-1	30			35	Note 2	ns max
		-2	25			30		
Control to Overflow Flag* W/SL	t _{LO}	-1	40			45	Note 2	ns max
		-2	35			45		

NOTES

*Indicates that a limit for this parameter has changed from REV. C.

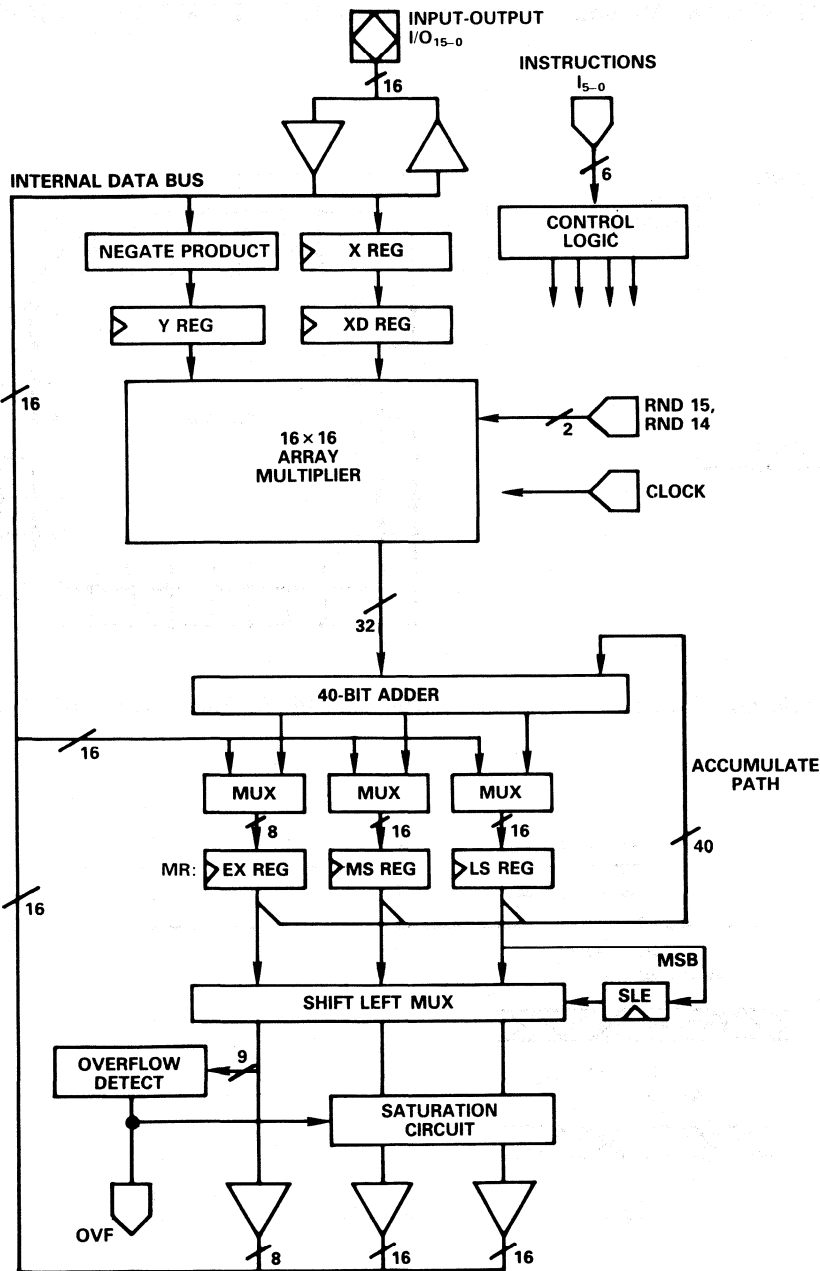
¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

³Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	RND15	15	CLK
2	RND14	16	I ₃
3	I/O ₁₄	17	I ₄
4	I/O ₁₂	18	I ₅
5	I/O ₁₀	19	OVF
6	I/O ₈	20	I/O ₁
7	I/O ₆	21	I/O ₃
8	I/O ₄	22	I/O ₅
9	I/O ₂	23	I/O ₇
10	I/O ₀	24	I/O ₉
11	I ₀	25	I/O ₁₁
12	I ₁	26	I/O ₁₃
13	I ₂	27	I/O ₁₅
14	GND	28	V _{DD}

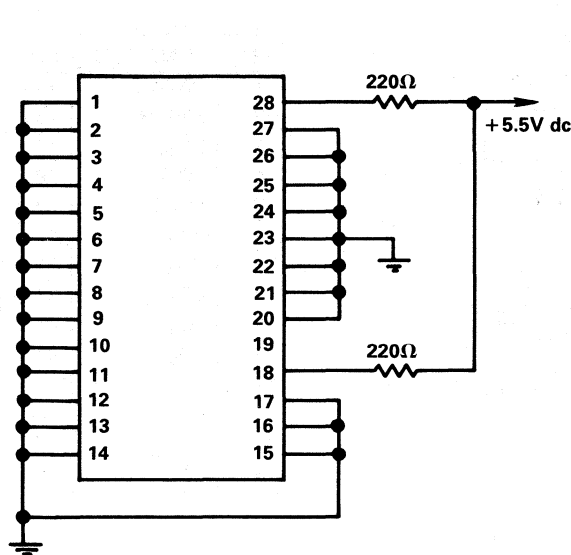
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

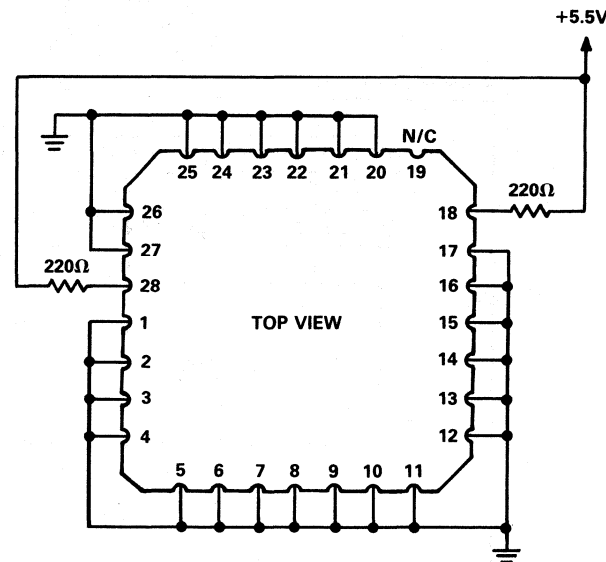
ADSP-1110A

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1110AD Life Test and Burn-In Circuit



ADSP-1110AE Life Test and Burn-In Circuit

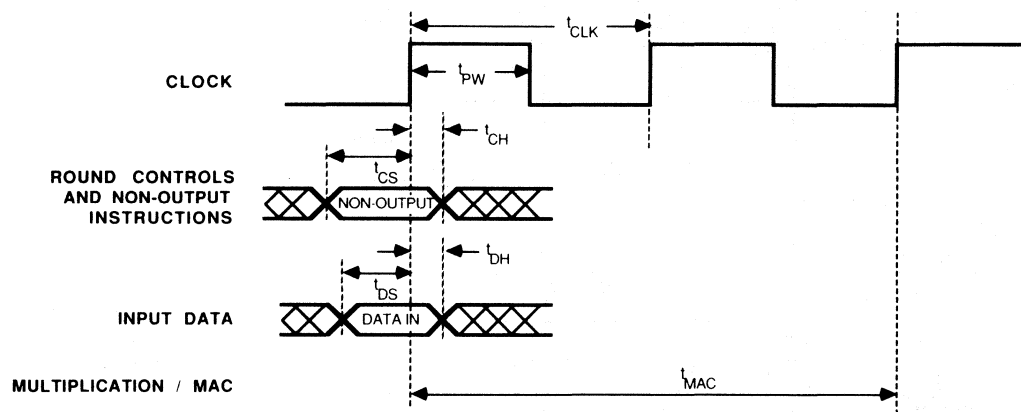


Figure 1. ADSP-1110A Timing: Clocked (Synchronous) Operations All Non-Output Instructions

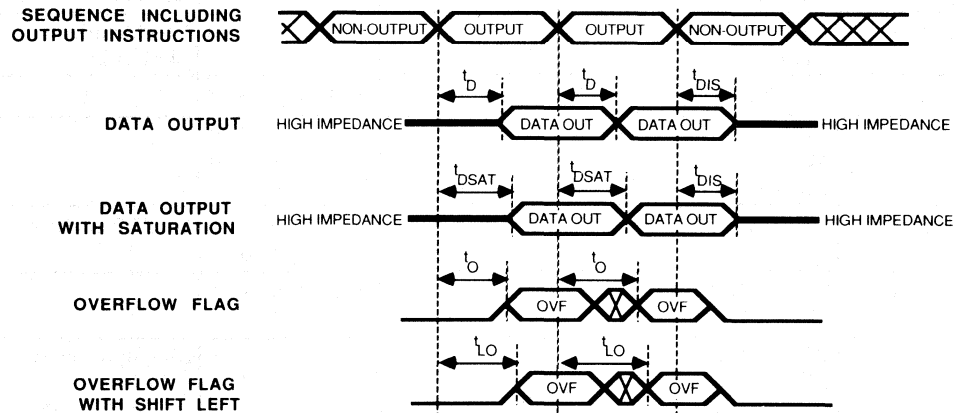


Figure 2. ADSP-1110A Timing: Unlocked (Asynchronous) Operations All Output Instructions

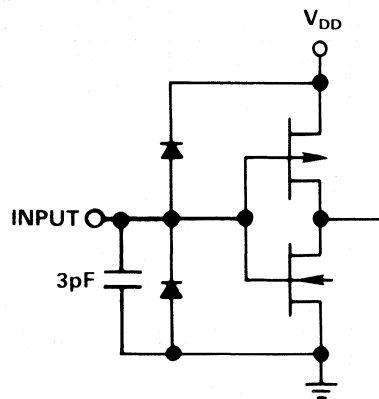


Figure 3. Equivalent Input Circuit

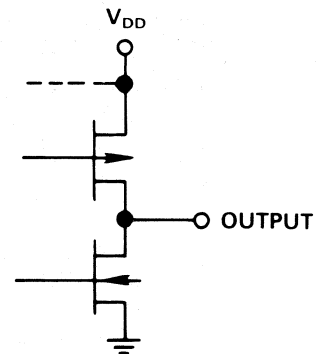


Figure 4. Equivalent Output Circuit

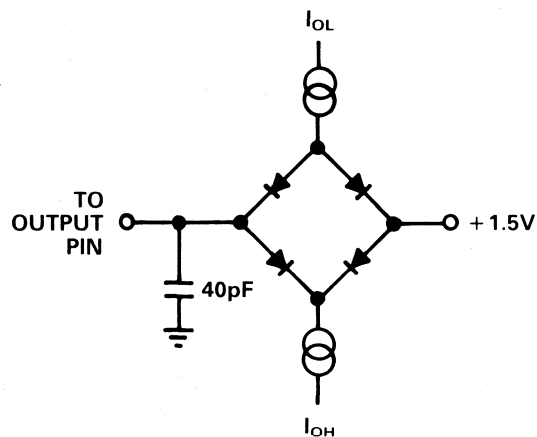


Figure 5. Normal Load Circuit for AC Measurements

Instruction Group	Instruction	Microcode Instruction						Comments
		5	4	3	2	1	0	
Miscellaneous	NOP	0	0	0	0	X	X	No Operation
	CKMR	0	0	0	1	X	X	Clock MR
Input	X = BUS	0	0	1	0	X	X	
Preload	LS = BUS	0	1	0	0	0	0	
	MS = BUS	0	1	0	1	X	0	
	EX = BUS	0	1	0	0	1	0	
Transfer	LS = MS	0	1	0	0	0	1	Set SLE register
	MS = EX	0	1	0	1	0	1	
Sign Extend	EX = SIGN EXT MS	0	1	0	0	1	1	
	MS = SIG EXT LS	0	1	0	1	1	1	
Output	BUS = EX	0	0	1	1	0	1	All output instructions are asynchronous I5-I2: 0011 = EX 0110 = MS 0111 = LS I1-I0: 01 = to bus 00 = to bus shifted 10 = to bus shifted w/saturation 11 = to bus w/saturation
	BUS = EX (sl)	0	0	1	1	0	0	
	BUS = MS	0	1	1	0	0	1	
	BUS = MS (sl)	0	1	1	0	0	0	
	BUS = MS (sat)	0	1	1	0	1	1	
	BUS = MS (sl, sat)	0	1	1	0	1	0	
	BUS = LS	0	1	1	1	0	1	
	BUS = LS (sl)	0	1	1	1	0	0	
	BUS = LS (sat)	0	1	1	1	1	1	
	BUS = LS (sl, sat)	0	1	1	1	1	0	
Multi-Operation	Y = BUS; CKMR; $X_{US} * Y_{US}$	1	0	0	X	0	0	Require two cycles to complete. Other instructions can be executed on the second cycle. I5 = Multiply/MAC operation I4 = Y twos complement I3 = X twos complement I2 = Subtract previous result I1 = Add/subtract previous result from product I0 = Negate product
	Y = BUS; CKMR; $-X_{US} * Y_{US}$	1	0	0	X	0	1	
	Y = BUS; CKMR; $X_{US} * Y_{US} + MR$	1	0	0	0	1	0	
	Y = BUS; CKMR; $-X_{US} * Y_{US} + MR$	1	0	0	0	1	1	
	Y = BUS; CKMR; $X_{US} * Y_{US} - MR$	1	0	0	1	1	0	
	Y = BUS; CKMR; $-X_{US} * Y_{US} - MR$	1	0	0	1	1	1	
	Y = BUS; CKMR; $X_{TC} * Y_{US}$	1	0	1	X	0	0	
	Y = BUS; CKMR; $-X_{TC} * Y_{US}$	1	0	1	X	0	1	
	Y = BUS; CKMR; $X_{TC} * Y_{US} + MR$	1	0	1	0	1	0	
	Y = BUS; CKMR; $-X_{TC} * Y_{US} + MR$	1	0	1	0	1	1	
	Y = BUS; CKMR; $X_{TC} * Y_{US} - MR$	1	0	1	1	1	0	
	Y = BUS; CKMR; $-X_{TC} * Y_{US} - MR$	1	0	1	1	1	1	
	Y = BUS; CKMR; $X_{US} * Y_{TC}$	1	1	0	X	0	0	
	Y = BUS; CKMR; $-X_{US} * Y_{TC}$	1	1	0	X	0	1	
	Y = BUS; CKMR; $X_{US} * Y_{TC} + MR$	1	1	0	0	1	0	
	Y = BUS; CKMR; $-X_{US} * Y_{TC} + MR$	1	1	0	0	1	1	
	Y = BUS; CKMR; $X_{US} * Y_{TC} - MR$	1	1	0	1	1	0	
	Y = BUS; CKMR; $-X_{US} * Y_{TC} - MR$	1	1	0	1	1	1	
	Y = BUS; CKMR; $X_{TC} * Y_{TC}$	1	1	1	X	0	0	
	Y = BUS; CKMR; $-X_{TC} * Y_{TC}$	1	1	1	X	0	1	
	Y = BUS; CKMR; $X_{TC} * Y_{TC} + MR$	1	1	1	0	1	0	
	Y = BUS; CKMR; $-X_{TC} * Y_{TC} + MR$	1	1	1	0	1	1	
	Y = BUS; CKMR; $X_{TC} * Y_{TC} - MR$	1	1	1	1	1	0	
	Y = BUS; CKMR; $-X_{TC} * Y_{TC} - MR$	1	1	1	1	1	1	

Mnemonic Definitions

=	Assign right side to left.	sl	Shift left.
BUS	16-bit external data bus used for all I/O operations.	sat	Conditional on overflow, saturate the outputted value.
X	Input register for multiplier.	TC	Twos complement number.
Y	Input register for multiplier.	US	Unsigned magnitude number.
EX	8-bit extension register for accumulator.	SIGN	Sign bit (MSB) of specified register.
MS	16-bit most significant product register.	CKMR	Clock product into EX, MS and LS.
LS	16-bit least significant product register.	*	Multiply
MR	40-bit accumulator comprising EX, MS and LS.	X	Microcode instruction bit can be either a 0 or 1.

Table 2. ADSP-1110A Instruction Set

1.1 Scope.

This specification covers the requirements for a CMOS monolithic program sequencer.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	ADSP-1401SD/883B
- 2	ADSP-1401TD/883B

1.2.3 Case Outline.

See Appendix I of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	- 0.3V to 7V
Input Voltage	- 0.3V to V_{DD}
Output Voltage	- 0.3V to V_{DD}
Operating Temperature Range (Ambient)	- 55°C to + 125°C
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1401 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Clock Input High Voltage	V _{IHC}	– 1, 2	3.0	3.0	3.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	– 1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = – 1mA	V min
Digital Output Low Voltage	V _{OL}	– 1, 2	0.6	0.6	0.6			V _{DD} = min I _{OL} = + 3mA	V max
Digital Input High Current	I _{IH}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = + 5.0V	μA max
Digital Input Low Current	I _{IL}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0V	μA max
Three-State Leakage Current Low	I _{OZL}	– 1, 2	50	50	50			V _{DD} = max V _{IN} = 0V	μA max
Three-State Leakage Current High	I _{OZH}	– 1, 2	50	50	50			V _{DD} = max V _{IN} = max	μA max
Supply Current*	I _{DD1}	– 1, 2	90	115	115			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	– 1, 2	35	65	65			All V _{IN} = 2.4V	mA max
Clock HI*	t _{HI}	– 1	50			60	60	Note 2	ns min
		– 2	40			50	50	Note 2	ns min
Clock LO*	t _{LO}	– 1	40			50	50	Note 2	ns min
		– 2	30			40	40	Note 2	ns min
Instruction Setup Time*	t _{IS}	– 1	36			45	45	Note 2	ns min
		– 2	30			40	40	Note 2	ns min
Data Setup Time*	t _{DS}	– 1, 2	10			15	15	Note 2	ns min
Input Signal Hold Time	t _{IH}	– 1, 2	3			3	3	Note 2	ns min
Address Delay* ³	t _{AD}	– 1	35			45	45	Note 2, C = 50pF	ns max
		– 2	25			35	35	Note 2, C = 50pF	ns max
Address Hold Time*	t _{AH}	– 1, 2	3			1	1	Note 2	ns min
Output Data Delay*	t _{ODD}	– 1	50			60	60	Note 2, C = 30pF	ns max
		– 2	35			45	45	Note 2, C = 30pF	ns max
Output Data Disable Time*	t _{ODIS}	– 1	20			25	25	Note 2	ns max
		– 2	15			20	20	Note 2	ns max
Input Flag Setup Time (IR0 Masked)	t _{IFSM}	– 1	15			20	20	Note 2, IR0 Masked	ns min
		– 2	10			15	15	Note 2, IR0 Masked	ns min
Input Flag Setup Time* (No Constraints)	t _{IFSU}	– 1	30			35	35	Note 2	ns min
		– 2	26			30	30		

Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Upper Interrupts Setup Time* (IR8-5)	t _{UIRS}	– 1	30			35	35	Note 2	ns min
		– 2	25			30	30		
Lower Interrupts Setup Time* (IR4-1)	t _{LIRS}	– 1	20			25	25	Note 2	ns min
		– 2	15			20	20		
Three-State (TTR) Setup Time*	t _{TSS}	– 1, 2	10			15	15	Note 2	ns min
Three-State (TTR) Overlap Time (with Trap)*	t _{TSOV}	– 1, 2	15			5	5	Note 2	ns max
Three-State (TTR) Disable Delay*	t _{TSE}	– 1	20			25	25	Notes 2, 4	ns max
		– 2	15			20	20		
Idle-to-Three-State Enable Delay*	t _{IDL3}	– 1	20			25	25	Notes 2, 4	ns max
		– 2	15			20	20		
Trap (TTR) Overlap Time (with Three-State)	t _{TROV}	– 1, 2	10			10	10	Notes 2, 4	ns max
Trap (TTR) to Address Delay*	t _{TRAD}	– 1	60			70	70	Notes 2, 4	ns max
		– 2	45			55	55		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

¹T_A = +25°C; V_{DD} = +4.5V min to +5.5V max (unless otherwise noted).

²Input levels are GND and +3.0V; V_{DD} = +4.5V. Rise times are 5ns. Input timing reference levels and output reference levels are measured at +1.5V except for three-state reference levels, which are shown in Figure 2.

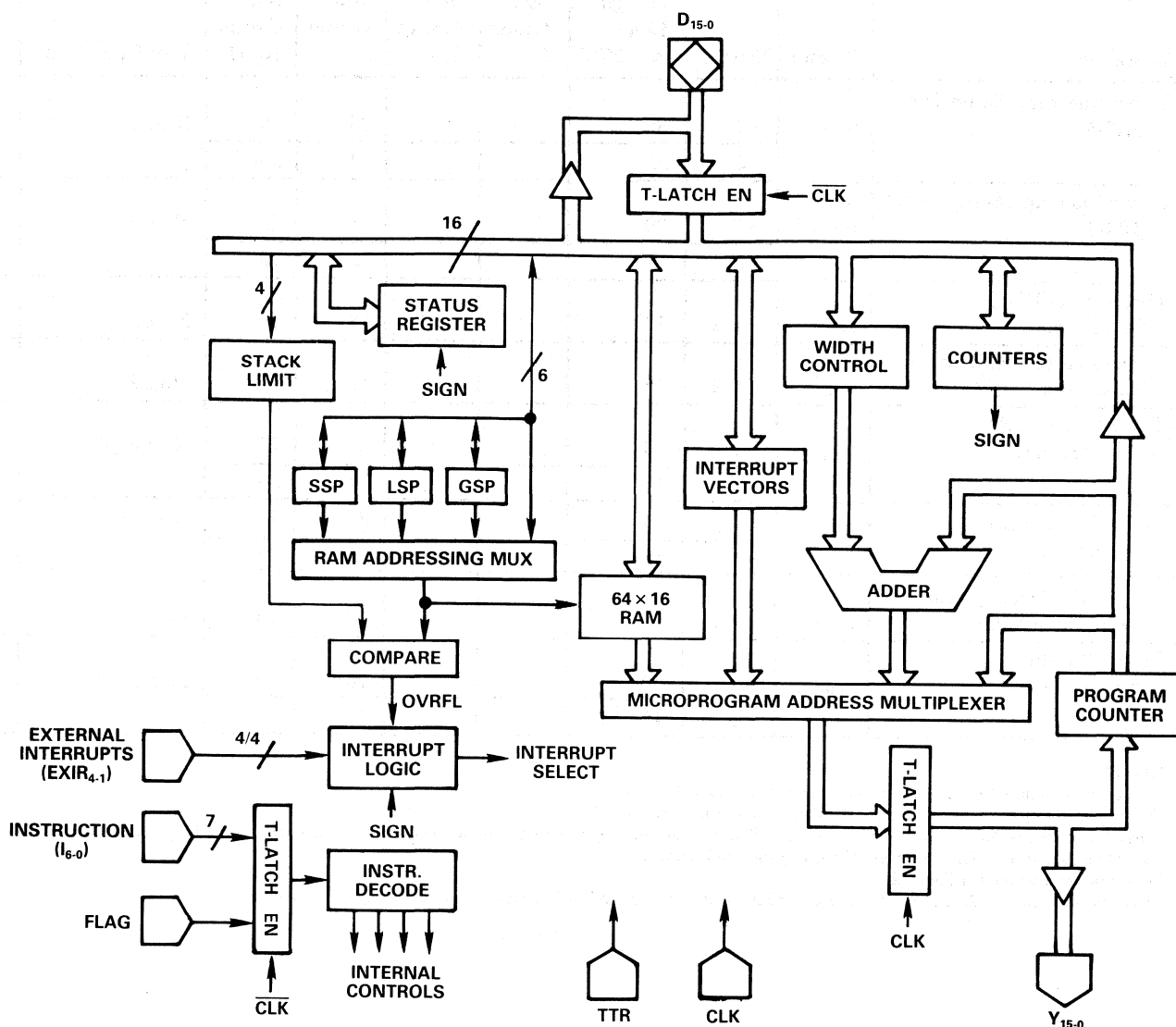
³Transitions measured per Figure 2.

⁴Address delays may be derated from the specified 50pF test loading by adding 7ns/50pF for increased capacitive loading.

Table 1.

ADSP-1401

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

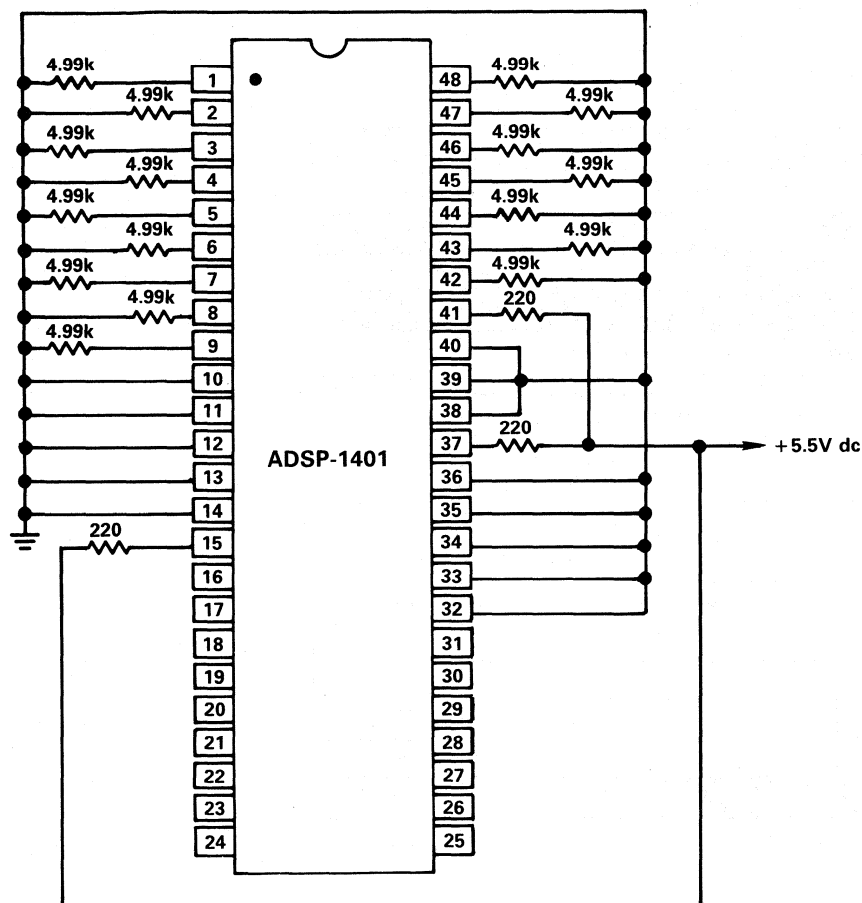
PIN	FUNCTION	PIN	FUNCTION
1	D7	25	Y6
2	D8	26	Y5
3	D9	27	Y4
4	D10	28	Y3
5	D11	29	Y2
6	D12	30	Y1
7	D13	31	Y0
8	D14	32	I0
9	D15	33	I1
10	EXIR1	34	I2
11	EXIR2	35	I3
12	GND	36	I4
13	EXIR3	37	V _{DD}
14	EXIR4	38	I5
15	TTR	39	I6
16	Y15	40	FLAG
16	Y14	41	CLK
18	Y13	42	D0
19	Y12	43	D1
20	Y11	44	D2
21	Y10	45	D3
22	Y9	46	D4
23	Y8	47	D5
24	Y7	48	D6

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



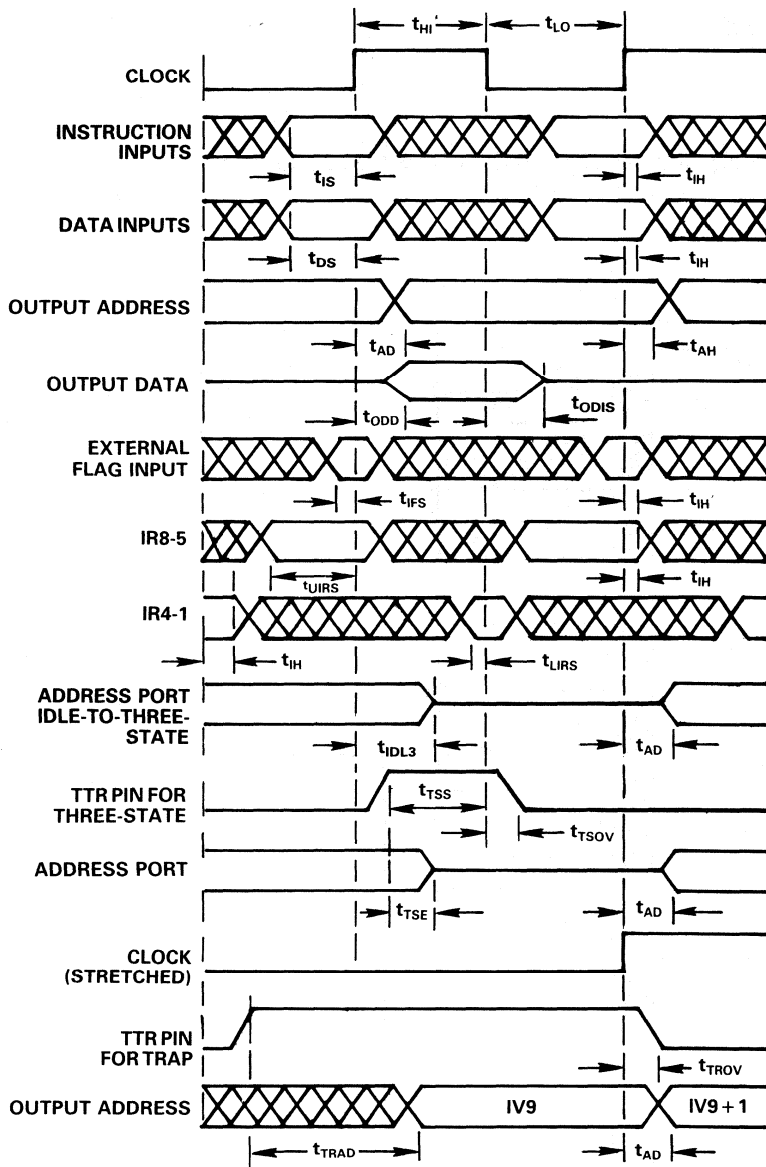


Figure 1. ADSP-1401 Timing Diagram

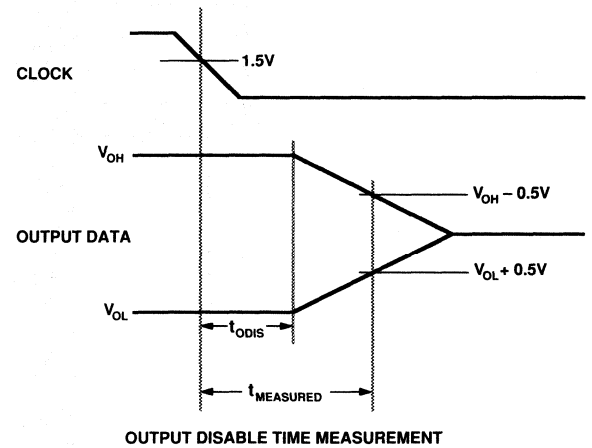


Figure 2. Three-State Reference Levels

Output disable time is measured from the time CLK reaches 1.5V to the time when all outputs have ceased driving. This is calculated by measuring the time, t_{MEASURED} , from the same starting point to when the output voltages have changed by 0.5V toward +1.5V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{\text{DECAY}} = \frac{C_L \cdot 0.5V}{i_L}$$

from which

$$t_{\text{ODIS}} = t_{\text{MEASURED}} - t_{\text{DECAY}}$$

is calculated. Disable times are longest at the highest specified temperature.

Mnemonic	Opcode (I ₆₋₀)	Description
Jump and Branch Instructions:		
JPCOF	001 0101	IF FLAG: JUMP PC (<i>self</i>)
JPCNF	011 0101	IF NOT FLAG: JUMP PC (<i>self</i>)
JTWO	101 cc01	IF COND: JUMP PC+2 (<i>skip</i>)
JDA	111 cc11	IF COND: JUMP DATA, ABSOLUTE
JDR	111 cc01	IF COND: JUMP DATA, RELATIVE
JDI	101 cc10	IF COND: JUMP DATA, INDIRECT
JDRST	100 11ii	IF SIGN OF C _i : JUMP DATA, C _i <= R _i ; ELSE, C _i <= C _i - 1
*JRC	110 ccii	IF COND: JUMP R _i
JRS	110 11ii	IF SIGN OF C _i : JUMP R _i , C _i <= C _i - 1
JSA	111 cc00	IF COND: JUMP SUB, ABSOLUTE
JSR	111 cc10	IF COND: JUMP SUB, RELATIVE
RTN	101 cc11	IF COND: RETURN FROM SUB
*BRANCH	100 ccii	IF SIGN OF C _i : JUMP R _i ; ELSE, C _i <= C _i - 1, IF COND: JUMP DATA
Stack Operations:		
<i>Subroutine Stack</i>		
PSDSS	001 1110	PUSH DATA ONTO SS
PPSSD	011 1110	POP SS TO DATA PORT
WRSSP	000 1110	WRITE SSP
RDSSP	010 1100	READ SSP
DSSP	000 0010	DECREMENT SSP
<i>Register Stack</i>		
SGSP	000 0111	SELECT GSP
SLSP	000 0110	SELECT LSP
RDRSP	010 1111	READ RSP
WRRSP	000 1100	WRITE RSP
PSPC	010 0011	PUSH PC ONTO RS
PSGSP	000 0101	PUSH GSP ONTO SS
PPGSP	000 0100	POP GSP FROM SS
PSDRS	001 1111	PUSH DATA ONTO RS
PPRSR	011 1111	POP RS TO DATA PORT
AIRSP	010 10ii	ADD i TO RSP
SIRSP	000 1111	SUBTRACT 1 FROM RSP
S4RSP	011 1100	SUBTRACT 4 FROM RSP
Status Register Operations:		
RDSR	010 1110	READ SR
WRSR	001 1100	WRITE SR
PSSR	010 0001	PUSH SR ONTO SS
PPSR	010 0010	POP SR FROM SS
Counter Operations:		
WRCNTR	011 10ii	WRITE C _i
CLRS	001 0100	CLEAR SIGN BIT
SETS	011 0100	SET SIGN BIT
PSCNTR	000 10ii	PUSH C _i ONTO SS
PPCNTR	001 10ii	POP C _i FROM SS
DCCNTR	011 00ii	DECREMENT C _i
IFCDEC	101 cc00	IF COND: DECREMENT C ₀
Interrupt Control:		
CCIR	001 0001	CLEAR CURRENT INTERRUPT
CAIR	000 0001	CLEAR ALL INTERRUPTS
RTNIR	000 0011	RETURN FROM INTERRUPT
RDIV	010 1101	READ INTERRUPT VECTOR AND INCREMENT IVP
WRIV	000 1101	WRITE INTERRUPT VECTOR AND INCREMENT IVP
IRMBC	001 0011	IR MASK BITWISE CLEAR
IRMBS	001 0010	IR MASK BITWISE SET
DISIR	001 0110	DISABLE INTERRUPTS
ENAIR	011 0110	ENABLE INTERRUPTS
SLIR	001 0111	SELECT LATCHED INTERRUPTS
STIR	011 0111	SELECT TRANSPARENT INTERRUPTS
SLRIVP	001 1101	WRITE SLR <= D ₅₋₂ AND IVP <= D ₁₅₋₁₂
Relative Address Width Controls:		
REL16	010 0100	SELECT 16-BIT RELATIVE ADDRESSING
REL12	010 0111	SELECT 12-BIT RELATIVE ADDRESSING
REL8	010 0110	SELECT 8-BIT RELATIVE ADDRESSING
Miscellaneous Instructions:		
CONT	000 0000	CONTINUE
IDLE	001 0000	IDLE
IHC	010 0101	ENABLE INSTRUCTION HOLD CONTROL
WCS	010 0000	WRITE CONTROL STORE

The SIGN condition is precluded from instructions prefixed with “*.”

Table 2. ADSP-1401 Instruction Set

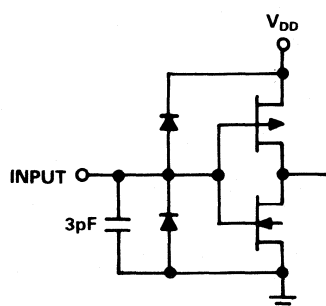


Figure 3. Equivalent Input Circuit

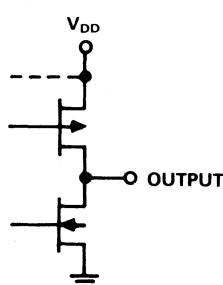


Figure 4. Equivalent Output Circuit

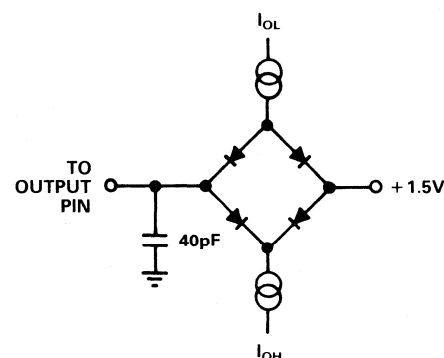


Figure 5. Normal Load for AC Measurements

1.1 Scope.

This specification covers the requirements for a CMOS monolithic address generator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	ADSP-1410SD/883B
– 2	ADSP-1410TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	– 0.3V to 7V
Input Voltage	– 0.3V to V_{DD}
Output Voltage	– 0.3V to V_{DD}
Operating Temperature Range (Ambient)	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1410 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Clock Input High Voltage*	V _{IHC}	– 1, 2	3.0	3.5	3.5			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	– 1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = – 1mA	V min
Digital Output Low Voltage*	V _{OL}	– 1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = + 3mA	V max
Digital Input High Current	I _{IH}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = + 5.0V	μA max
Digital Input Low Current	I _{IL}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0V	μA max
Three-State Leakage Current Low	I _{OZL}	– 1, 2	50	50	50			V _{DD} = max V _{IN} = 0V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	– 1, 2	50	50	50			V _{DD} = max V _{IN} = max (High Z)	μA max
Supply Current*	I _{DD1}	– 1, 2	75	100	100			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	– 1, 2	35	50	50			All V _{IN} = 2.4V	mA max
Instruction Setup Time*	t _{IS}	– 1	20			30	30	Note 2	ns min
		– 2	15			20	20		
Instruction Hold Time*	t _{IH}	– 1	5			5	5	Note 2	ns min
		– 2	4			4	4		
Instruction Cycle Time*	t _{CY}	– 1	100			125	125	Note 2	ns min
		– 2	90			100	100		
Input Data Setup Time	t _{IDS}	– 1, 2	10			10	10	Note 2	ns min
Input Data Hold Time*	t _{IDH}	– 1, 2	5			6	6	Note 2	ns min
Guaranteed Clock-to-Data Delay*	t _{ODD}	– 1	35			45	45	Notes 2, 3	ns min
		– 2	30			40	40		
		– 1	55			70	70		ns max
		– 2	50			60	60		
Output Data Disable Time*	t _{DDIS}	– 1	20			25	25	Note 2	ns max
		– 2	20			20	20		
Output Address Disable Time* (Latched Mode)	t _{ADISL}	– 1	30			45	45	Note 2	ns max
		– 2	25			40	40		
Output Address Disable Time* (Transparent Mode)	t _{ADIST}	– 1	40			55	55	Note 2	ns max
		– 2	35			50	50		
LATCHED MODE, GUARANTEED CLOCK-TO-OUTPUT DELAYS									
Pre-Update Address Delay*	t _{LAN}	– 1	35			40	40	Notes 2, 3	ns min
		– 2	30			35	35		
		– 1	45			55	55		ns max
		– 2	35			45	45		
Pre-Update CMP/Z Flag Delay*	t _{LFN}	– 1	45			60	60	Notes 2, 3; C = 25pF	ns min
		– 2	35			45	45		
		– 1	55			75	75		ns max
		– 2	45			60	60		

Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Output Data Enable Time	t _{DENA}	− 1	30			40	40	Notes 2, 4	ns min
		− 2	25			35	35		
		− 1	50			65	65	Notes 2, 4	ns max
		− 2	45			55	55		
Post-Update Address Delay*	t _{LAP}	− 1	35			40	40	Notes 2, 3	ns min
		− 2	30			35	35		
		− 1	60			75	75	Notes 2, 4	ns max
		− 2	50			55	55		
Post-Update CMP/Z Flag Delay*	t _{LFP}	− 1	45			60	60	Notes 2, 3; C = 25pF	ns min
		− 2	35			45	45		
		− 1	70			95	95		ns max
		− 2	55			75	75		
TRANSPARENT MODE, VALID-INSTRUCTION-TO-OUTPUT DELAYS									
Pre-Update Address Delay*	t _{TAN}	− 1	50			65	65	Note 2	ns max
		− 2	45			55	55		
Pre-Update CMP/Z Flag Delay*	t _{TFN}	− 1	65			90	90	Note 2; C = 25pF	ns max
		− 2	55			70	70		
Post-Update Address Delay*	t _{TAP}	− 1	75			95	95	Note 2	ns max
		− 2	65			80	80		
Post-Update CMP/Z Flag Delay* ⁴	t _{TFP}	− 1	90			115	115	Note 2; C = 25pF	ns max
		− 2	75			95	95		
SUPPLEMENTAL PARAMETERS FOR DOUBLE-CHIP/DOUBLE-PRECISION OPERATIONS ⁵									
Valid Instruction to Carry/Shift Output Delay*	t _{CSD}	− 1	65			80	80	Note 2	ns max
		− 2	57			72	72		
Carry/Shift Input Setup Time*	t _{CSS}	− 1	35			40	40	Note 2	ns min
		− 2	28			35	35		
Carry/Shift Input to Valid MS Address (Post-Update Only)*	t _{MSD}	− 1	45			55	55	Note 2	ns max
		− 2	40			48	48		
Valid Instruction to MS CMP/Z Flag Delay	t _{CZD_C}	− 1	115			120	120	Note 2	ns max
		− 2	105			115	115		
Clock High to CMP/Z (Compare) Invalid Delay	t _{CZI}	− 1, 2	4			4	4	Note 2	ns min
Valid Instruction to CMP/Z (Zero) Flag Delay	t _{CZD_Z}	− 1	80			85	85	Note 2	ns max
		− 2	70			80	80		
Instruction Valid to CMP/Z (Zero) Invalid Delay	t _{IID}	− 1, 2	10			10	10	Note 2	ns min

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

¹T_A = +25°C; V_{DD} = +4.5V min to +5.5V max (unless otherwise noted).

²Input levels are GND and +3.0V; V_{DD} = +4.5V. Rise times are 5ns. Input timing reference levels and output reference levels are measured at +1.5V per Figure 1.

³Measured with the maximum usable instruction setup time before the rising edge of the clock. This max usable setup time may be calculated for any timing spec as:

Maximum usable instruction setup time = max (t_{SPEC}) - min (t_{SPEC}) + min (t_{IS}). For example, Maximum usable setup time for t_{LAN} for the - 2 part is:

max (t_{LAN}) - min (t_{LAN}) + min (t_{IS}) = 45 - 35 + 20 = 30ns.

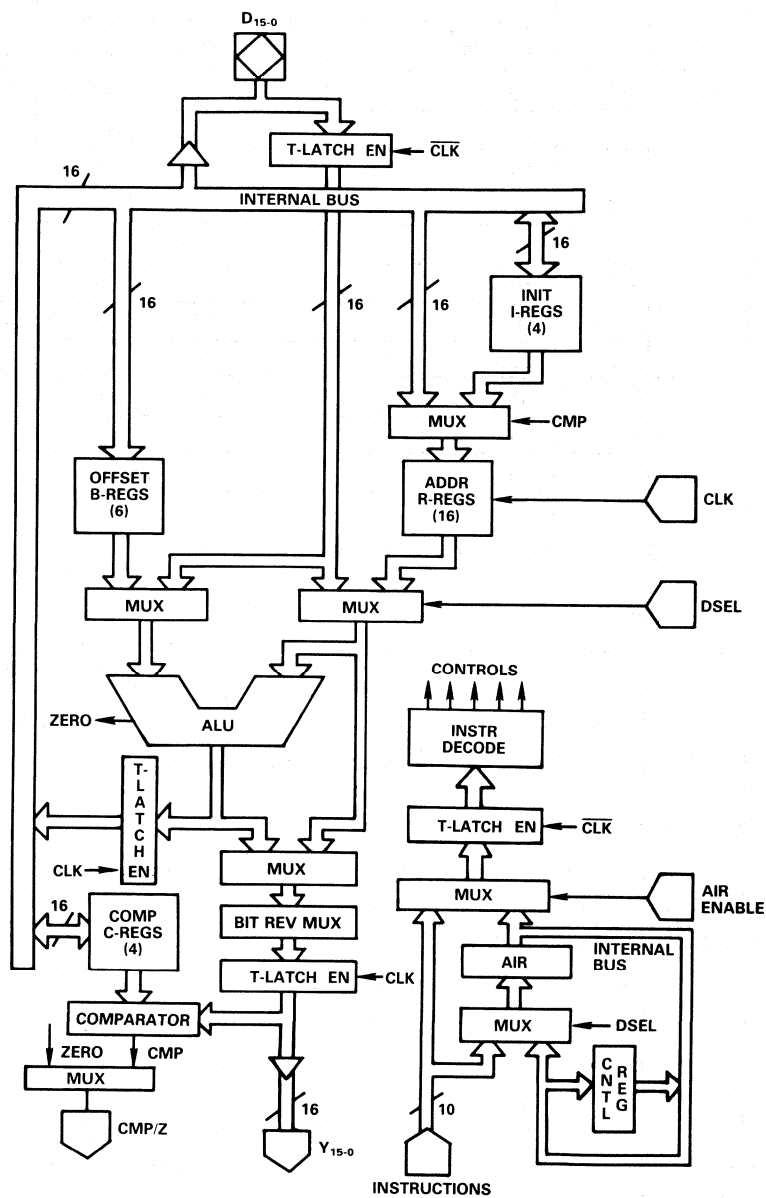
⁴Measured with the minimum instruction setup time for the respective - 1 or - 2 part.

⁵The Instruction Cycle Time, t_{CY}, does not apply to DCDP operation. Clock HI and LO relationships for DCDP operation are described in the text below under DCDP Parameters: t_{HI} is derived from the t_{CSD}, t_{CSS}, t_{MSD} and t_{IS} parameters, and the inequality t_{LO} ≥ t_{IS} must also hold.

Table 1.

ADSP-1410

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

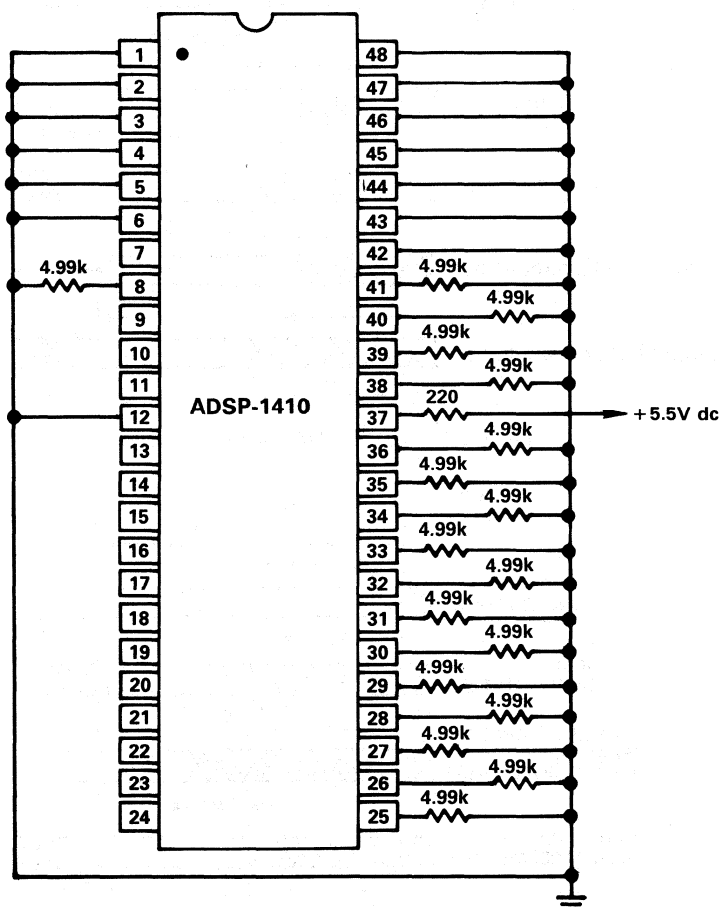
PIN	FUNCTION	PIN	FUNCTION
1	I4	48	I5
2	I3	47	I6
3	I2	46	I7
4	I1	45	I8
5	I0	44	I9
6	CLK	43	DSEL
7	CMP/Z	42	AIRE
8	Y15	41	D15
9	Y14	40	D14
10	Y13	39	D13
11	Y12	38	D12
12	GND	37	V _{DD}
13	Y11	36	D11
14	Y10	35	D10
15	Y9	34	D9
16	Y8	33	D8
17	Y7	32	D7
18	Y6	31	D6
19	Y5	30	D5
20	Y4	29	D4
21	Y3	28	D3
22	Y2	27	D2
23	Y1	26	D1
24	Y0	25	D0

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



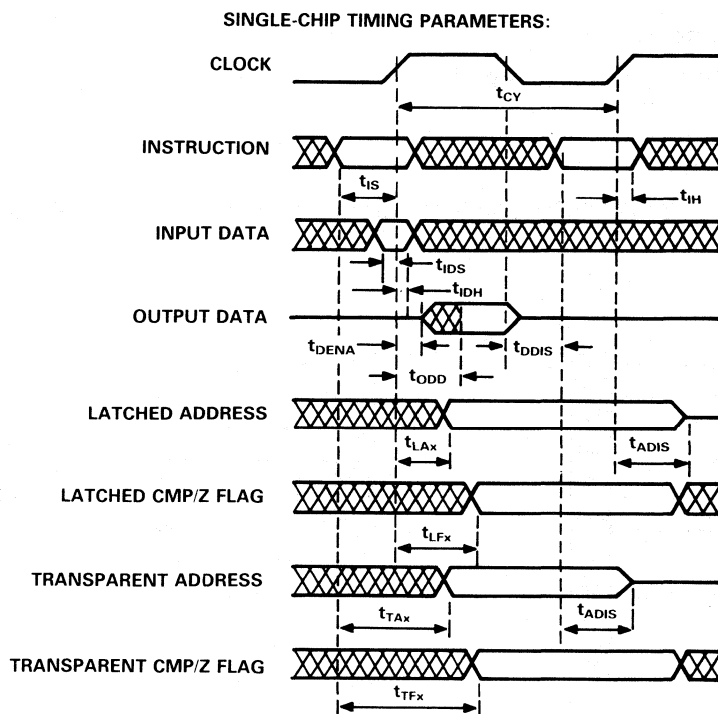


Figure 1. ADSP-1410 Timing Diagram

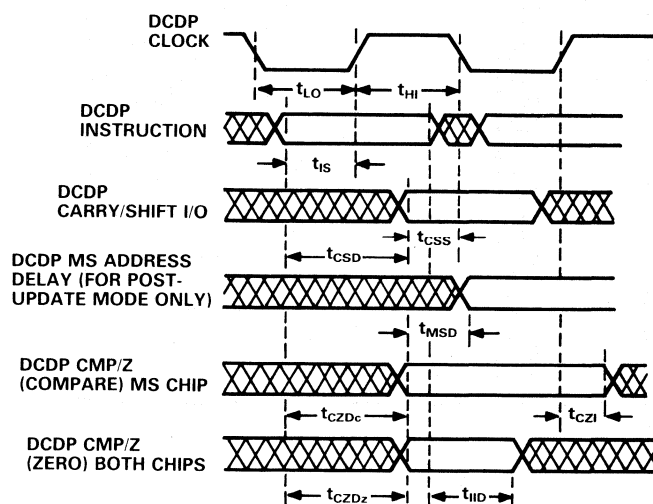


Figure 2. Supplemental Parameters for Double-Chip/Double-Precision Operation

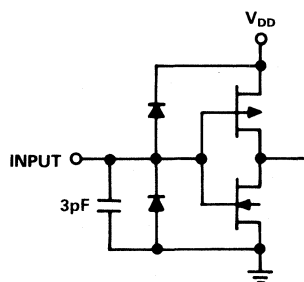


Figure 3. Equivalent Input Circuit

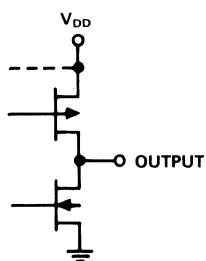


Figure 4. Equivalent Output Circuits

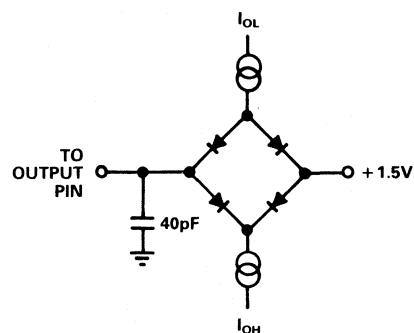


Figure 5. Normal Load for AC Measurements

Instr.	Opcode (I ₉₋₀)	Description
Looping Instructions		
YINC*†:	1011ccrrrr	output & increment/init
YDEC*†:	1010ccrrrr	output & decrement/init
YADD*†:	11ccbb1rrr	output & add offset/init
YSUB*†:	11ccbb0rrr	output & subtract offset/init
Register Transfer Instructions		
YRTR*:	000101rrrr	output & xfr R to R
YRTB*:	0011bbrrrr	output & xfr R to B
YRTC*:	0010ccrrrr	output & xfr R to C
DTI:	00001111ii	xfr D to I
ITR:	1000ii rrrr	xfr I to R
BTR:	0100bbrrrr	xfr B to R
RTD:	000100rrrr	xfr R to D
CTD:	00001100cc	xfr C to D
BTD:	00001101bb	xfr B to D
ITD:	00001110ii	xfr I to D
Logical and Shift Instructions		
YOR*†:	0111bbrrrr	output & OR B with/to R
YAND*†:	0110bbrrrr	output & AND B with/to R
YXOR*†:	0101bbrrrr	output & XOR B with/to R
YASR*†:	000111rrrr	output & arith SR R to R
YLSL*†:	000110rrrr	output & logical SL R to R
Control Register Instructions		
RST:	0000000001	reset CR
DTCR:	0000101110	xfr D to CR
CRTD:	0000101111	xfr CR to D
SETI:	0000100iix	set cond re-init on CMP mode
SETP:	00001010pp	set chip precision
SETY:	000001001x	set Y port to trans/latched mode
SELR:	000001101x	select upper/lower R bank
SELB:	000001100x	select upper/lower B bank
SETU:	000001011x	set post/pre update mode
SETA:	000001010x	set cond AIR mode
AIR Instructions		
WRA:	0000101100	write AIR with D
RDA:	0000101101	read AIR at D
LDA:	0000011110	load AIR on next cycle
Misc. Instructions		
YDTY:	0000011111	pass D to Y port
YREV*†:	1001bbrrrr	output R in bit-reverse format
NOP:	0000000000	no operation

*External data may substitute for R using DSEL.

†Operable in either pre- or post-update mode.

Table 2. ADSP-1410 Instruction Set



12.5 MIPS DSP Microprocessor

ADSP-2100/ADSP-2100A

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16-bit fixed-point DSP microprocessor.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADSP-2100S(X)/883B
-2	ADSP-2100AS(X)/883B
-2	ADSP-2100AT(X)/883B
-4	ADSP-2100AU(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

G	G-100A	100-Lead Pin Grid Array
Z	F-100A	100-Contact Ceramic Quad Flat Pack

1.3 Absolute Maximum Ratings.

Supply Voltage		-0.3 V to 7 V
Input Voltage		-0.3 V to $V_{DD} + 0.3$ V
Output Voltage		-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range (Ambient)		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C
Maximum Power Dissipation		0.750 W

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-2100/ADSP-2100A – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage ²	V _{IH1}	–1, 2, 3, 4	2.0	2.2	2.2			V _{DD} = max	V min
Digital Input High Voltage at CLKIN	V _{IH2}	–2, 3, 4	2.2	2.4	2.4			V _{DD} = max	V min
Digital Input Low Voltage ²	V _{IL}	–1, 2, 3, 4	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage ³	V _{OH}	–1, 2, 3, 4	2.4	2.4	2.4			V _{DD} = max I _{OH} = –1 mA	V min
Digital Output Low Voltage ³	V _{OL}	–1, 2, 3, 4	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current ⁴	I _{IH}	–1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = max	μA max
Digital Input Low Current ⁴	I _{IL}	–1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage ⁵ Current High	I _{OZH}	–1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = max ⁸	μA max
Three-State Leakage ⁶ Current Low	I _{OZL1}	–1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = 0.0 V ⁸	μA max
Three-State Pullup Current ⁷	I _{OZL2}	–1	150	150	150			V _{DD} = max V _{IN} = 0.0 V ⁸	μA max
		–2, 3, 4	180	180	180				
Supply Current, Dynamic	I _{DD1}	–1	90	100	100			V _{DD} = max Max Clock Rate ⁹	mA max
		–2	150	130	130				
		–3		180	180				
		–4		200	200				
Supply Current, Power-Down ¹⁰	I _{DD2}	–1	10	15	15			V _{DD} = max V _{IN} = 0.0 V ^{7, 8}	mA max
		–2, 3, 4	10	10	10				
CLKIN Period	1 ¹²	–1	40.5			40.5	40.5	A	ns min
		–2	24.4			30.5	30.5		
		–3	20			24.4	24.4		
		–4	20			20	20		
CLKIN Width Low	2	–1	11			11	11	A	ns min
		–2	7			8	8		
		–3	4			7	7		
		–4	4			4	4		
CLKIN Width High	3	–1	18			18	18	A	ns min
		–2	9			12	12		
		–3	8			9	9		
		–4	8			8	8		
CLKIN Low (3–4) to CLKOUT Low	4	–1	13			11	11	B	ns min
			34			34	34		ns max
		–2	24			29	29		
		–3	22			24	24		
		–4	22			22	22		
CLKIN LOW (7–8) to CLKOUT High	5	–1	6			5	5	B	ns min
			24			24	24		ns max
		–2	20			20	20		
		–3	18			20	20		
		–4	18			18	18		

Table 1. (Continued on next page)

REV. A

ADSP-2100/ADSP-2100A

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
CLKOUT Width Low	6	-1 -2 -3 -4	60 36 28 28			60 45 36 28	60 45 36 28	A	ns min
RESET Low to CLKIN High	7	-1, 2, 3, 4	2			2	2	B	ns min
CLKIN High to RESET High	8	-1 -2 -3 -4	36 6 20 6 16 4 16 4			36 6 26 6 20 4 16 4	36 6 26 6 20 4 16 4	B	ns max ns min ns max ns min ns max ns min ns max ns min
RESET Width Low	9	-1 -2 -3 -4	162 98 80 80			170 128 98 80	170 128 98 80	A	ns min
HALT Valid to CLKIN Low (3-4)	10	-1 -2, 3, 4	0 2			0 2	0 2	B	ns min
CLKIN Low (3-4) to HALT Invalid	11	-1 -2 -3 -4	12 10 8 8			12 10 10 8	12 10 10 8	B	ns min
CLKIN Low (7-8) to TRAP Valid	12	-1 -2 -3 -4	25 18 16 16			25 20 18 16	25 20 18 16	B	ns max
CLKIN Low (7-8) to IRQ Valid	13	-1 -2, 3, 4	2 1			1 1	1 1	B	ns max
CLKIN Low (7-8) to IRQ Invalid	14	-1 -2 -3, 4	21 14 14			21 17 14	21 17 14	B	ns min
BR Valid to CLKIN Low (3-4)	15	-1 -2 -3, 4	1 4 4			1 1 4	1 1 4	B	ns min
CLKIN Low (3-4) to BR Invalid	16	-1 -2 -3, 4	10 4 4			10 7 4	10 7 4	B	ns min
CLKIN Low (3-4) to BG Low	17	-1 -2 -3 -4	38 26 24 24			38 30 26 24	38 30 26 24	B	ns max

Table 1. (Continued on next page)

ADSP-2100/ADSP-2100A

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
CLKIN Low (7-8) to $\overline{\text{BG}}$ High	18	-1 -2 -3 -4	31 24 20 20			31 25 24 20	31 25 24 20	B	ns max
$\overline{\text{BG}}$ Low to xMxx Disable	19 ¹³	-1 -2 -3, 4	22 16 16			22 17 16	22 17 16	D	ns max
xMxx Enable to $\overline{\text{BG}}$ High	20 ¹³	-1 -2 -3 -4	12 10 8 8			12 10 10 8	12 10 10 8	F	ns max
$\overline{\text{BR}}$ Low to $\overline{\text{BG}}$ Low During Reset	21	-1 -2 -3 -4	28 18 16 16			28 23 18 16	28 23 18 16	A	ns max
$\overline{\text{BR}}$ High to $\overline{\text{BG}}$ High During Reset	22	-1 -2 -3 -4	21 16 14 14			21 18 16 14	21 18 16 14	A	ns max
$\overline{\text{PMRD}}$ Width Low	31	-1 -2 -3 -4	60 36 28 28			60 45 36 28	60 45 36 28	A	ns min
PMA Valid to $\overline{\text{PMRD}}$ Low	32	-1 -2 -3 -4	18 6 4 4			18 14 6 4	18 14 6 4	A	ns min
$\overline{\text{PMRD}}$ High to PMA Invalid	33	-1 -2 -3 -4	20 8 6 6			20 10 8 6	20 10 8 6	A	ns min
PMDA Valid to $\overline{\text{PMRD}}$ Low	34	-1 -2 -3 -4	41 20 18 18			41 24 20 15	41 24 20 15	A	ns min
$\overline{\text{PMRD}}$ High to PMDA Invalid	35	-1 -2 -3, 4	23 10 10			22 12 10	22 12 10	A	ns min
$\overline{\text{PMS}}$ Valid to $\overline{\text{PMRD}}$ Low	36	-1 -2 -3 -4	55 32 26 26			55 40 32 26	55 40 32 26	A	ns min

Table 1. (Continued on next page)

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ADSP-2100/ADSP-2100A

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
PMRD High to PMS Invalid	37	-1	16			16	16	A	ns min
		-2	8			8	8		
		-3	6			8	8		
		-4	6			6	6		
PMWR Width Low	40	-1	60			60	60	A	ns min
		-2	36			45	45		
		-3	28			36	36		
		-4	28			28	28		
PMA Valid to PMWR Low	41	-1	16			16	16	A	ns min
		-2	8			12	12		
		-3	4			8	8		
		-4	4			4	4		
PMWR High to PMA Invalid	42	-1	19			19	19	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		
PMDA Valid to PMWR Low	43	-1	39			39	39	A	ns min
		-2	20			28	28		
		-3	16			20	20		
		-4	15			16	16		
PMWR High to PMDA Invalid	44	-1	20			21	21	A	ns min
		-2	10			12	12		
		-3	8			10	10		
		-4	8			8	8		
PMS Valid to PMWR Low	45	-1	54			54	54	A	ns min
		-2	32			40	40		
		-3	26			32	32		
		-4	26			26	26		
PMWR High to PMS Invalid	46	-1	15			14	14	A	ns min
		-2	6			8	8		
		-3	4			6	6		
		-4	4			4	4		
PMWR Low to PMD Out Enable	51	-1	15			15	15	F	ns min
		-2	8			8	8		
		-3	6			8	8		
		-4	6			6	6		
PMWR High to PMD Out Disable	52	-1	43			43	43	D	ns max
		-2	32			38	38		
		-3	29			32	32		
		-4	29			29	29		
PMWR Low to PMD Out Valid	53	-1	40			40	40	A	ns max
		-2	29			32	32		
		-3	26			29	29		
		-4	26			26	26		

Table 1. (Continued on next page)

ADSP-2100/ADSP-2100A

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
PMWR High to PMD Out Invalid	54	-1	23			21	21	A	ns min
		-2	10			12	12		
		-3	8			10	10		
		-4	8			8	8		
PMD Out Valid to to PMWR High	55	-1	33			33	33	A	ns min
		-2	16			25	25		
		-3	13			16	16		
		-4	13			13	13		
PMRD Low to PMD Input Valid	58	-1	45			45	45	A	ns max
		-2	28			33	33		
		-3	20			28	28		
		-4	20			18	18		
PMA Valid to PMD Input Valid	59	-1	57			57	57	A	ns max
		-2	46			50	50		
		-3	32			46	46		
		-4	32			32	32		
PMS Valid to PMD Input Valid	60	-1	90			90	90	A	ns max
		-2	50			65	65		
		-3	45			50	50		
		-4	45			35	35		
DMRD Width Low	67	-1	60			60	60	A	ns min
		-2	36			45	45		
		-3	28			36	36		
		-4	28			28	28		
DMA Valid to DMRD Low	68	-1	21			21	21	A	ns min
		-2	6			14	14		
		-3	4			6	6		
		-4	4			4	4		
DMRD High to DMA Invalid	69	-1	19			19	19	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		
DMS Valid to DMRD Low	70	-1	35			35	35	A	ns min
		-2	18			27	27		
		-3	14			18	18		
		-4	14			14	14		
DMRD High to DMS Invalid	71	-1	22			21	21	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		

Table 1. (Continued on next page)

ADSP-2100/ADSP-2100A

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
$\overline{\text{DMRD}}$ Low to DMACK Valid	74	-1	31 0			31 0	31 0	A	ns max ns min
		-2	16 0			21 0	21 0		ns max ns min
		-3	10 0			16 0	16 0		ns max ns min
		-4	10 0			10 0	10 0		ns max ns min
DMA Valid to DMACK Valid	75	-1	57 0			57 0	57 0	A	ns max ns min
		-2	30 0			42 0	42 0		ns max ns min
		-3	20 0			30 0	30 0		ns max ns min
		-4	20 0			20 0	20 0		ns max ns min
$\overline{\text{DMWR}}$ Width Low	78	-1	60			60	60	A	ns min
		-2	36			45	45		
		-3	28			36	36		
		-4	28			28	28		
DMA Valid to $\overline{\text{DMWR}}$ Low	79	-1	24			24	24	A	ns min
		-2	8			17	17		
		-3	4			8	8		
		-4	4			4	4		
$\overline{\text{DMWR}}$ High to DMA Invalid	80	-1	20			19	19	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		
DMS Valid to $\overline{\text{DMWR}}$ Low	81	-1	37			37	37	A	ns min
		-2	20			28	28		
		-3	16			20	20		
		-4	16			16	16		
$\overline{\text{DMWR}}$ High to DMS Invalid	82	-1	22			22	22	A	ns min
		-2	6			8	8		
		-3	4			6	6		
		-4	4			4	4		
$\overline{\text{DMWR}}$ Low to DMD Out Enable	87	-1	14			14	14	F	ns min
		-2	8			8	8		
		-3	6			8	8		
		-4	6			6	6		
$\overline{\text{DMWR}}$ High to DMD Out Disable	88	-1	40			40	40	D	ns max
		-2	32			38	38		
		-3	29			32	32		
		-4	29			29	29		

Table 1. (Continued on next page)

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ADSP-2100/ADSP-2100A

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
DMWR Low to DMD Out Valid	89	-1	38			38	38	A	ns max
		-2	29			32	32		
		-3	26			29	29		
		-4	26			26	26		
DMWR High to DMD Out Invalid	90	-1	21			19	19	A	ns min
		-2	10			12	12		
		-3	8			10	10		
		-4	8			8	8		
DMD Out Valid to DMWR High	91	-1	33			33	33	A	ns min
		-2	18			25	25		
		-3	13			16	16		
		-4	13			13	13		
DMRD Low to DMD Input Valid	94	-1	57			55	55	A	ns max
		-2	30			37	37		
		-3	20			28	28		
		-4	20			18	18		
DMA Valid to DMD Input Valid	95	-1	82			79	79	A	ns max
		-2	48			59	59		
		-3	32			46	46		
		-4	32			32	32		
DMS Valid to DMD Input Valid	96	-1	96			96	96	A	ns max
		-2	52			67	67		
		-3	45			50	50		
		-4	45			35	35		
PMRD High to PMD Input Valid	97	-1, 2, 3, 4	0			0	0	A	ns min
DMRD High to DMD Input Invalid	98	-1, 2, 3, 4	0			0	0	A	ns min
DMWR Low to DMACK Valid	99	-1	31			31	31	A	ns max
			0			0	0		ns min
		-2	16			20	20		ns max
			0			0	0		ns min
		-3	10			16	16		ns max
			0			0	0		ns min
		-4	10			10	10		ns max
			0			0	0		ns min
CLKOUT High to DMACK Invalid	103	-1	60			60	60	A	ns max
			0			0	0		ns min
		-2	36			45	45		ns max
			0			0	0		ns min
		-3	28			36	36		ns max
			0			0	0		ns min
		-4	28			28	28		ns max
			0			0	0		ns min

Table 1. (Continued on next page)

REV. A

NOTES

- ¹T_A = 25°C; V_{DD} = +4.5 V to +5.5 V max (unless otherwise noted).
- ²Applies to pins: PMD₀₋₂₃, DMD₀₋₁₅, $\overline{\text{BR}}$, $\overline{\text{IRQ}}_{0-3}$, DMACK, RESET, HALT, (48 input pins for ADSP-2100A). Includes CLKIN for ADSP-2100 (49 input only pins).
- ³Applies to pins: PMA₀₋₁₃, $\overline{\text{PMS}}$, PMD₀₋₂₃, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMDA, $\overline{\text{BG}}$, DMA₀₋₁₃, $\overline{\text{DMS}}$, DMD₀₋₁₅, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$, TRAP, CLKOUT (78 output pins).
- ⁴Applies to pins: $\overline{\text{BR}}$, $\overline{\text{IRQ}}_{0-3}$, DMACK, RESET, HALT, CLKIN (9 input only pins).
- ⁵Applies to pins: PMA₀₋₁₃, $\overline{\text{PMS}}$, PMD₀₋₂₃, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMDA, DMA₀₋₁₃, $\overline{\text{DMS}}$, DMD₀₋₁₅, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ (75 tristateable pins).
- ⁶Applies to pins: PMA₀₋₁₃, PMDA, DMA₀₋₁₃ (29 tristateable pins w/o pullup).
- ⁷Applies to pins: PMD₀₋₂₃, $\overline{\text{PMS}}$, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, DMD₀₋₁₅, $\overline{\text{DMS}}$, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ (46 tristateable pins w/pullup).
- ⁸Additional Test Conditions: V_{IN} = 0 V on $\overline{\text{BR}}$ and RESET, CLKIN active forces tristate condition.
- ⁹Additional Test Conditions: Outputs loaded TTL loads w/100 pF capacitance, V_{IH} = 2.4 V, V_{IL} = 0.4 V, clock rate = max.
- ¹⁰"Power-down" refers to an idle state. While the processor does not have any special standby or low power mode, these conditions represent the lowest power consumption state.
- ¹¹Input levels are GND and +3.0 V; V_{DD} = +4.5 V, and timing transitions per Figures 1 through 10b, measured at 1.5 V.
- ¹²Rise and fall times ≤ 4 ns for ADSP-2100A, 5 ns for ADSP-2100.
- ¹³"xMxx" refers to PMA₀₋₁₃, $\overline{\text{PMS}}$, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMDA, DMA₀₋₁₃, $\overline{\text{DMS}}$, $\overline{\text{DMRD}}$ and $\overline{\text{DMWR}}$.

Table 1.

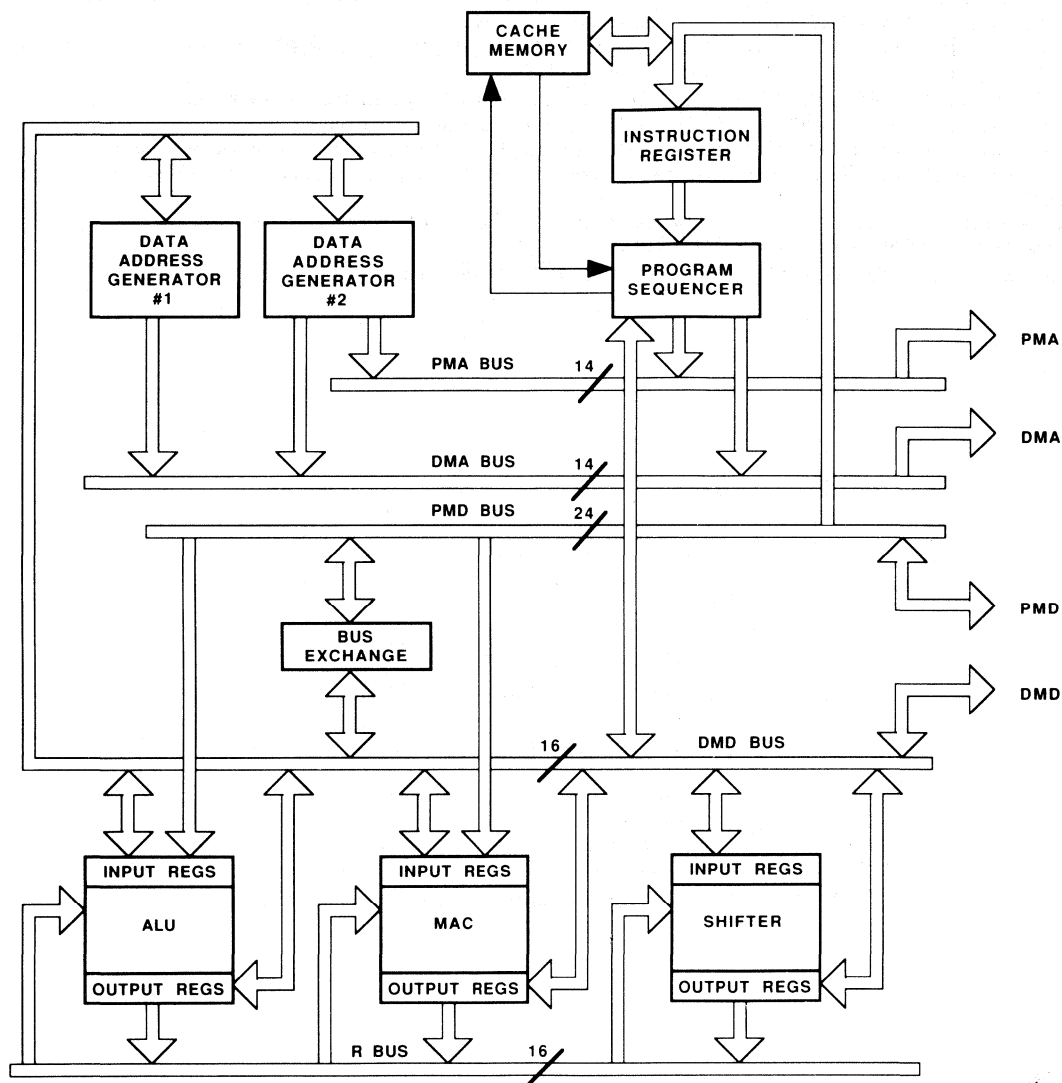
TEST CODES

Code	Test Type	Level Reference
A	Inputs, Outputs	Low = 0.8V, High = 2.0V
B	CLKIN to/from	1.5V
	Inputs, Outputs	Low = 0.8V, High = 2.0V
D	Output to	Low = 0.8V, High = 2.0V
	Output Disable	Low = V _{OL} + 0.5V, High = V _{OH} - 0.5V
F	Output to/from	Low = 0.8V, High = 2.0V
	Output Enable	Low = VT - 0.1V, High = VT + 0.1V

VT = 1.5 V, the voltage to which tristated outputs are forced.

ADSP-2100/ADSP-2100A

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

G-100A

Function	Location	Function	Location	Function	Location	Function	Location
V _{DD}	A7	PMA1	B13	PMD12	K13	DMA9	G1
V _{DD}	G13	PMA2	C12	PMD13	K12	DMA10	G3
V _{DD}	H1	PMA3	A13	PMD14	L13	DMA11	G2
V _{DD}	N8	PMA4	B12	PMD15	L12	DMA12	F1
GND	A1	PMA5	A12	PMD16	M13	DMA13	F2
GND	A6	PMA6	B11	PMD17	M12	DMD0	A5
GND	A11	PMA7	B10	PMD18	N13	DMD1	B5
GND	E13	PMA8	A10	PMD19	M11	DMD2	A4
GND	H13	PMA9	B9	PMD20	N12	DMD3	B4
GND	J1	PMA10	A9	PMD21	N11	DMD4	A3
GND	M2	PMA11	C8	PMD22	M10	DMD5	A2
GND	N6	PMA12	B8	PMD23	N10	DMD6	B3
GND	N7	PMA13	A8	PMS	N5	DMD7	B2
CLKIN	L7	PMD0	D12	PMWR	L6	DMD8	B1
CLKOUT	L8	PMD1	D13	PMRD	M9	DMD9	C2
BR	M8	PMD2	E12	PMDA	M4	DMD10	C1
BG	N9	PMD3	F11	DMA0	N1	DMD11	D2
IRQ0	C6	PMD4	F12	DMA1	L2	DMD12	D1
IRQ1	B6	PMD5	F13	DMA2	M1	DMD13	E2
IRQ2	C7	PMD6	G11	DMA3	L1	DMD14	E1
IRQ3	B7	PMD7	G12	DMA4	K2	DMD15	F3
RESET	N2	PMD8	H12	DMA5	K1	DMS	M5
TRAP	N4	PMD9	H11	DMA6	J2	DMWR	M6
HALT	N3	PMD10	J13	DMA7	H3	DMRD	M7
INDEX PIN	NC	PMD11	J12	DMA8	H2	DMACK	M3
PMA0	C13						

F-100A

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	PMD6	21	PMA10	41	DMD9	61	DMA2	81	BG
2	V _{DD}	22	PMA11	42	DMD10	62	DMA1	82	PMRD
3	PMD5	23	PMA12	43	DMD11	63	DMA0	83	PMD23
4	PMD4	24	PMA13	44	DMD12	64	GND	84	PMD22
5	PMD3	25	IRQ3	45	DMD13	65	RESET	85	PMD21
6	GND	26	IRQ2	46	DMD14	66	DMACK	86	PMD20
7	PMD2	27	V _{DD}	47	DMD15	67	HALT	87	PMD19
8	PMD1	28	GND	48	DMA13	68	PMDA	88	PMD18
9	PMD0	29	IRQ1	49	DMA12	69	TRAP	89	PMD17
10	PMA0	30	IRQ0	50	DMA11	70	DMS	90	PMD16
11	PMA1	31	DMD0	51	DMA10	71	PMS	91	PMD15
12	PMA2	32	DMD1	52	DMA9	72	PMWR	92	PMD14
13	PMA3	33	DMD2	53	V _{DD}	73	DMWR	93	PMD13
14	PMA4	34	DMD3	54	DMA8	74	GND	94	PMD12
15	PMA5	35	DMD4	55	DMA7	75	DMRD	95	PMD11
16	PMA6	36	DMD5	56	GND	76	CLKIN	96	PMD10
17	GND	37	DMD6	57	DMA6	77	GND	97	PMD9
18	PMA7	38	GND	58	DMA5	78	V _{DD}	98	PMD8
19	PMA8	39	DMD7	59	DMA4	79	BR	99	GND
20	PMA9	40	DMD8	60	DMA3	80	CLKOUT	100	PMD7

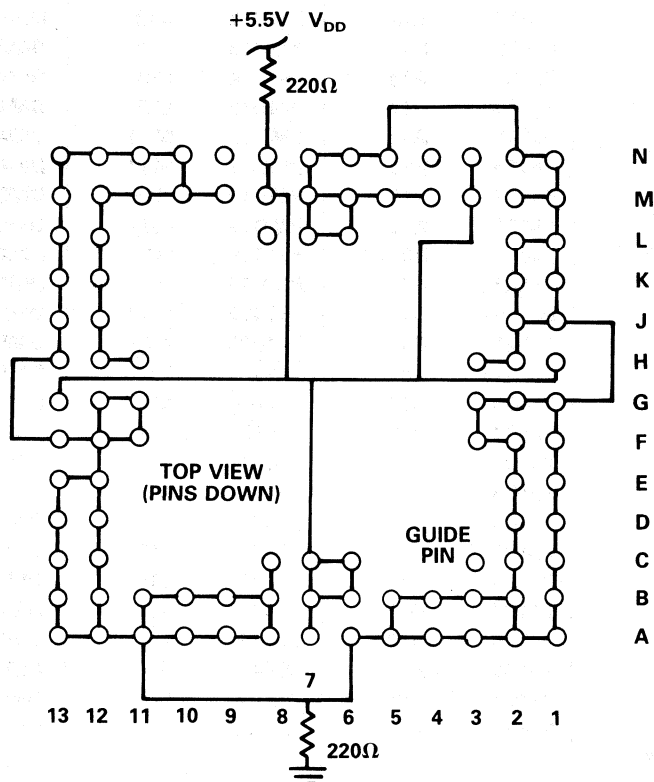
ADSP-2100/ADSP-2100A

3.2.4. Microcircuit Technology Group.

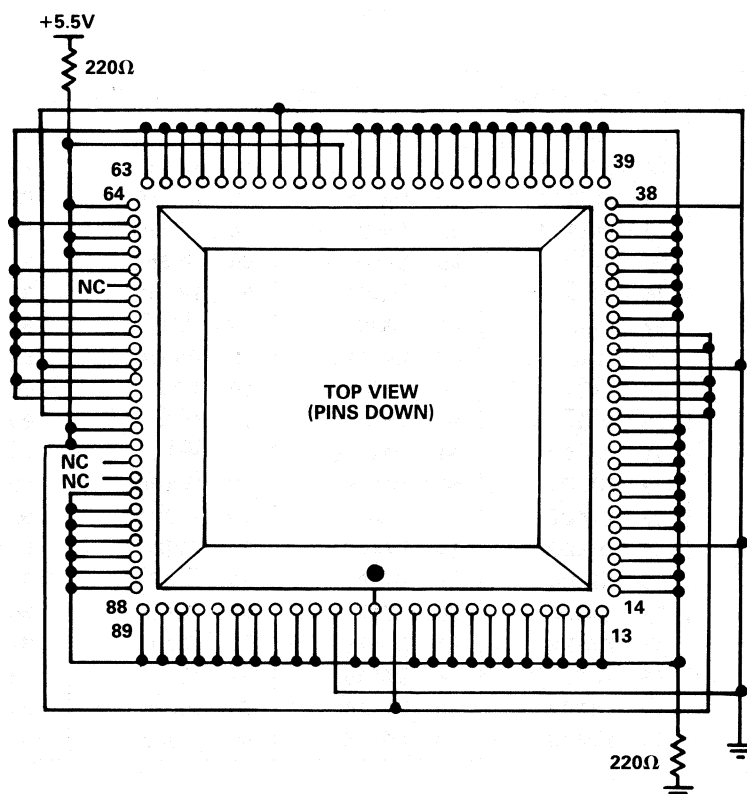
This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

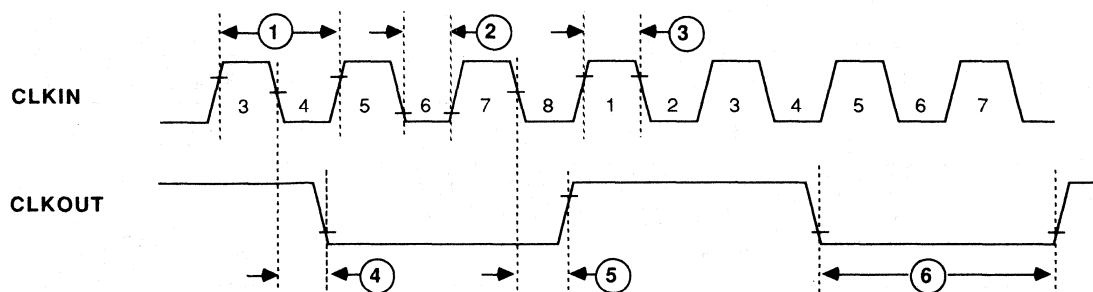


ADSP-2100G/ADSP-2100AG Life Test and Burn-In Circuit



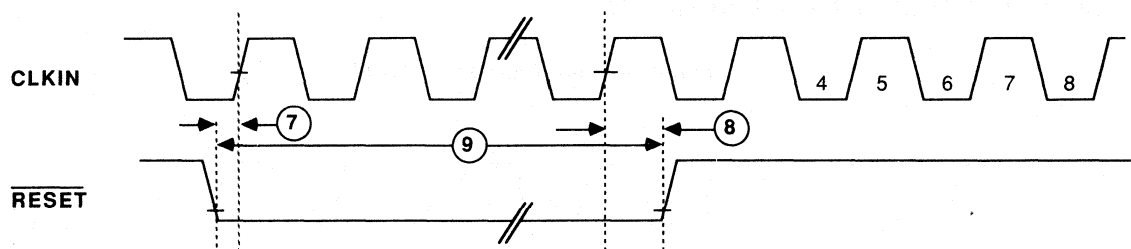
ADSP-2100Z/ADSP-2100AZ Life Test and Burn-In Circuit

REV. A



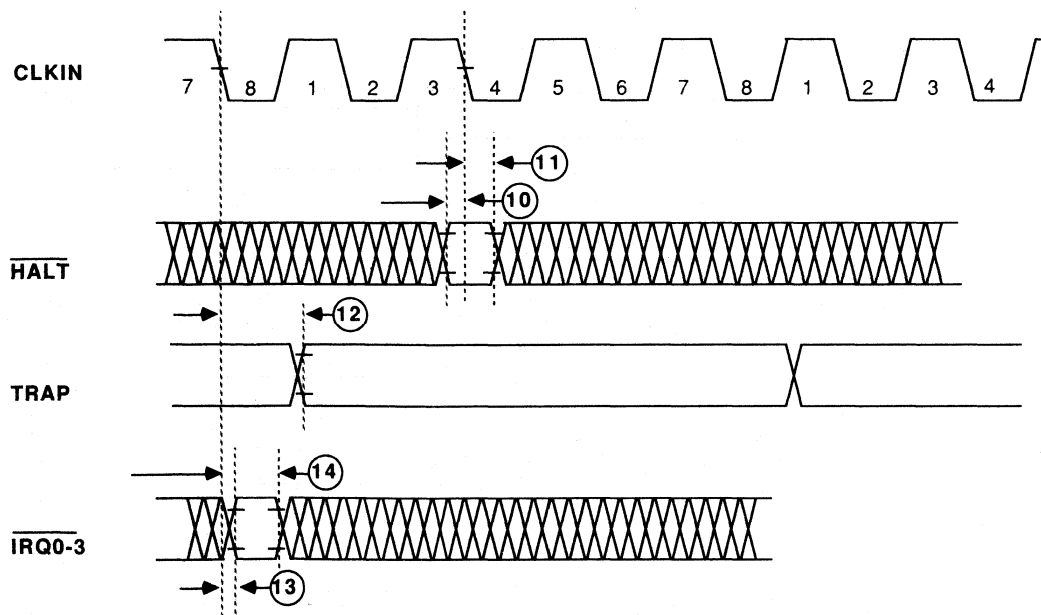
NOTE
The Processor Cycle is Divided into 8 Internal States Determined by the Rising and Falling Edges of CLKIN. CLKOUT is Synchronized to the Processor States as Shown Above.

Figure 1. Clock Signals



NOTE
The Reset signal determines the phase of the processor cycle. The processor starts from state 4 after the release of the Reset signal.

Figure 2. $\overline{\text{RESET}}$ Signal



NOTE
The Control Signals are Shown in Relationship to the Processor States in Which They are Recognized or Asserted as Defined by CLKIN. There is No Implied Relationship between HALT, TRAP, and IRQ₀₋₃.

Figure 3. Control Signals

ADSP-2100/ADSP-2100A

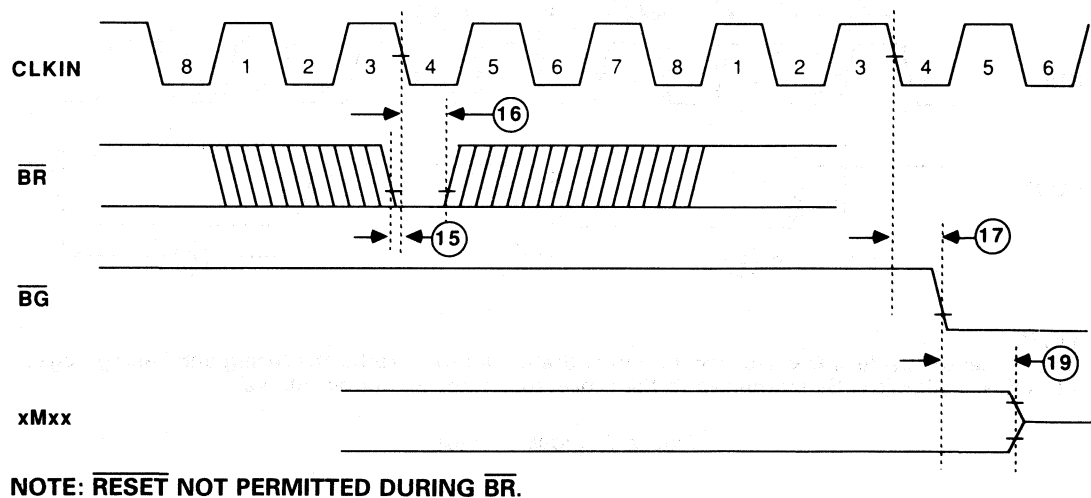


Figure 4. Bus Request Asserted

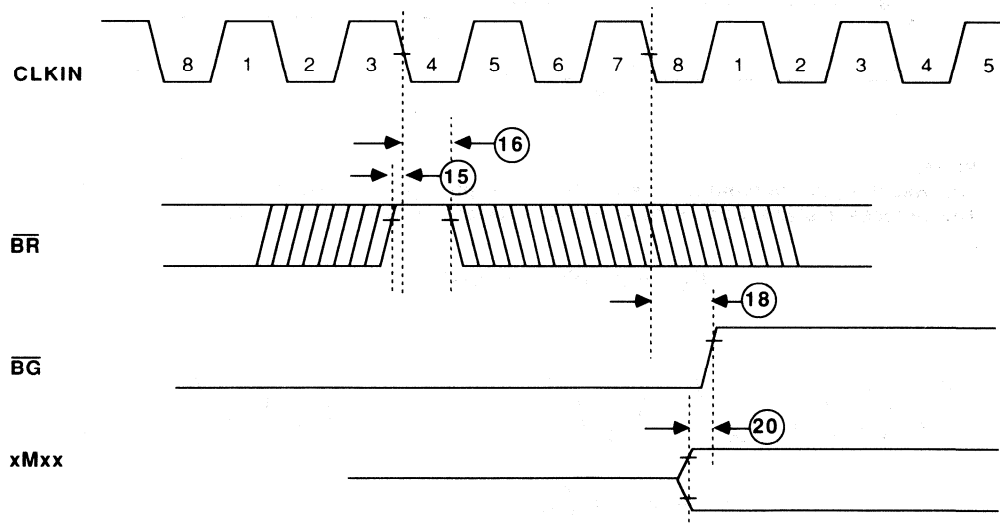
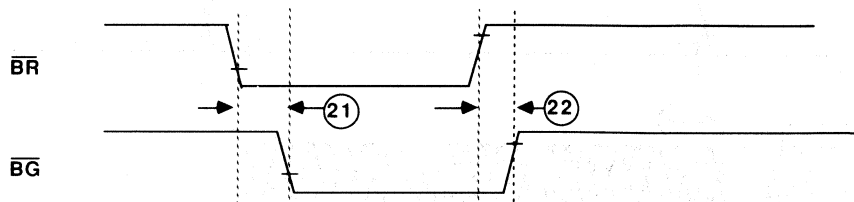


Figure 5. Bus Request Negated



NOTE
During Reset, the Processor Bus Ignores the CLKIN Signal and Therefore the Bus Request/Grant Signals Operate Asynchronously.

Figure 6. Bus Request/Grant with $\overline{\text{RESET}}$ Low

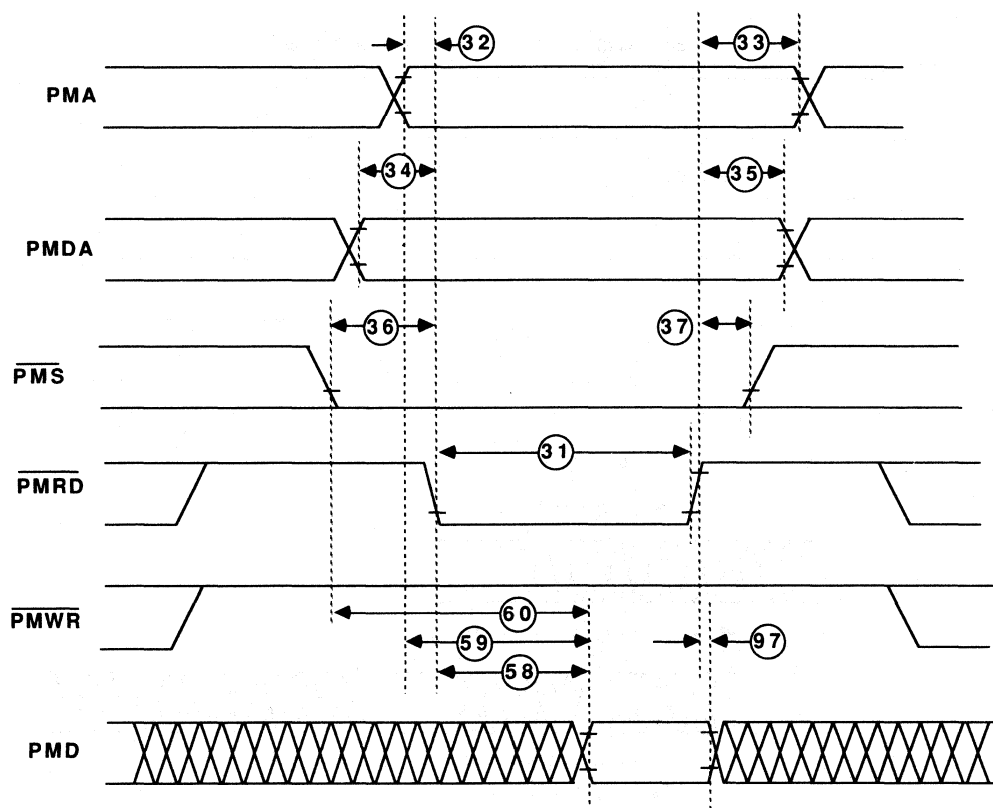


Figure 7. Program Memory Read

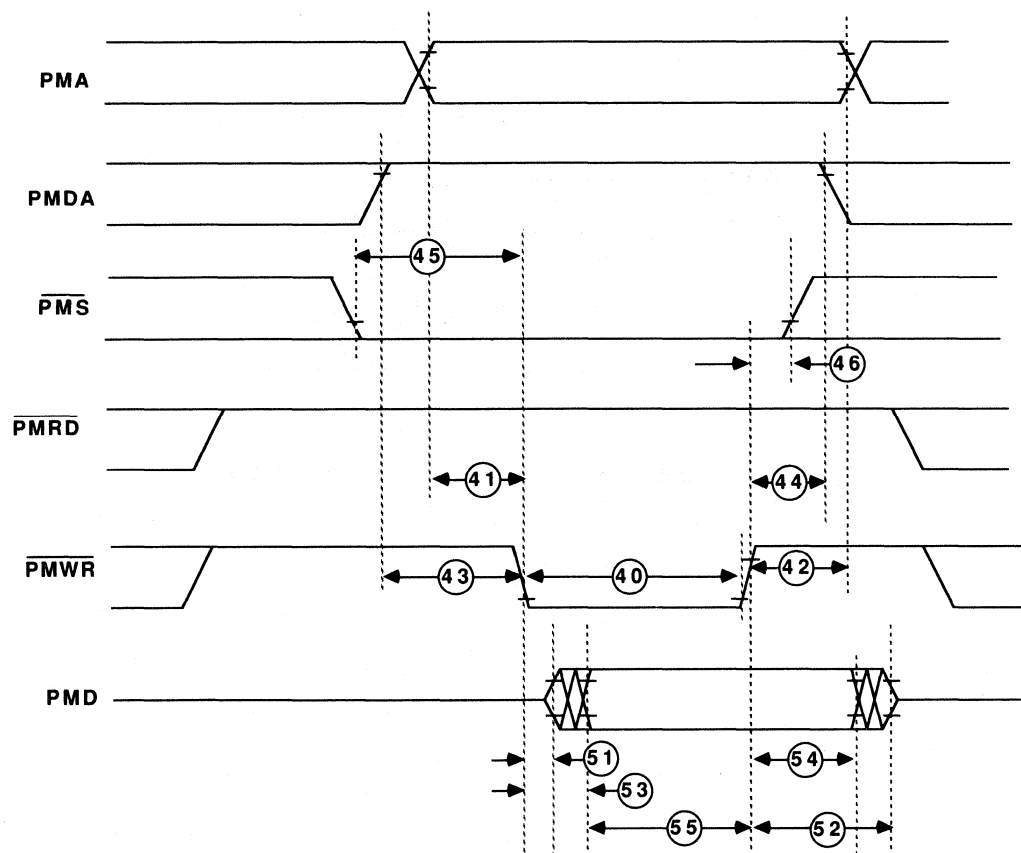


Figure 8. Program Memory Write

ADSP-2100/ADSP-2100A

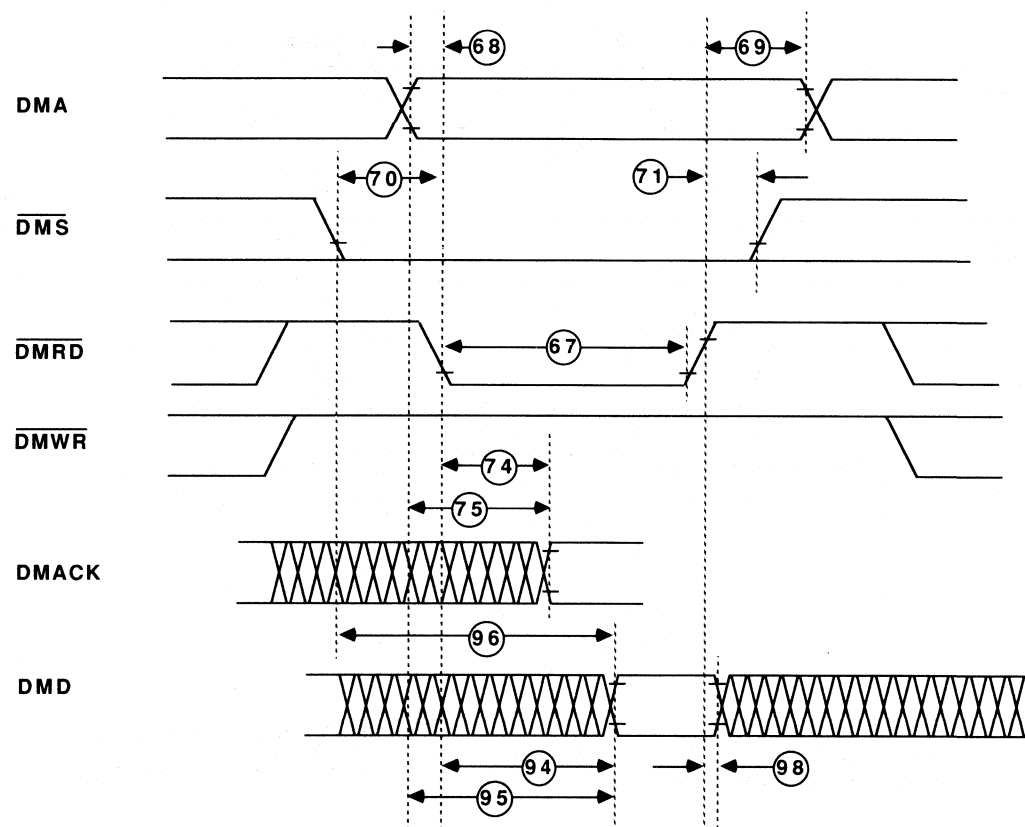


Figure 9a. Data Memory Read

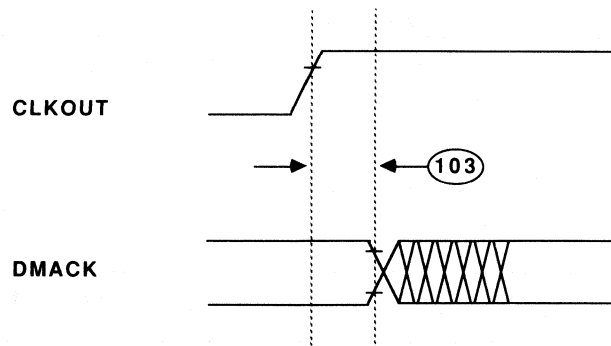


Figure 9b. Data Memory Wait States Extended with DMACK

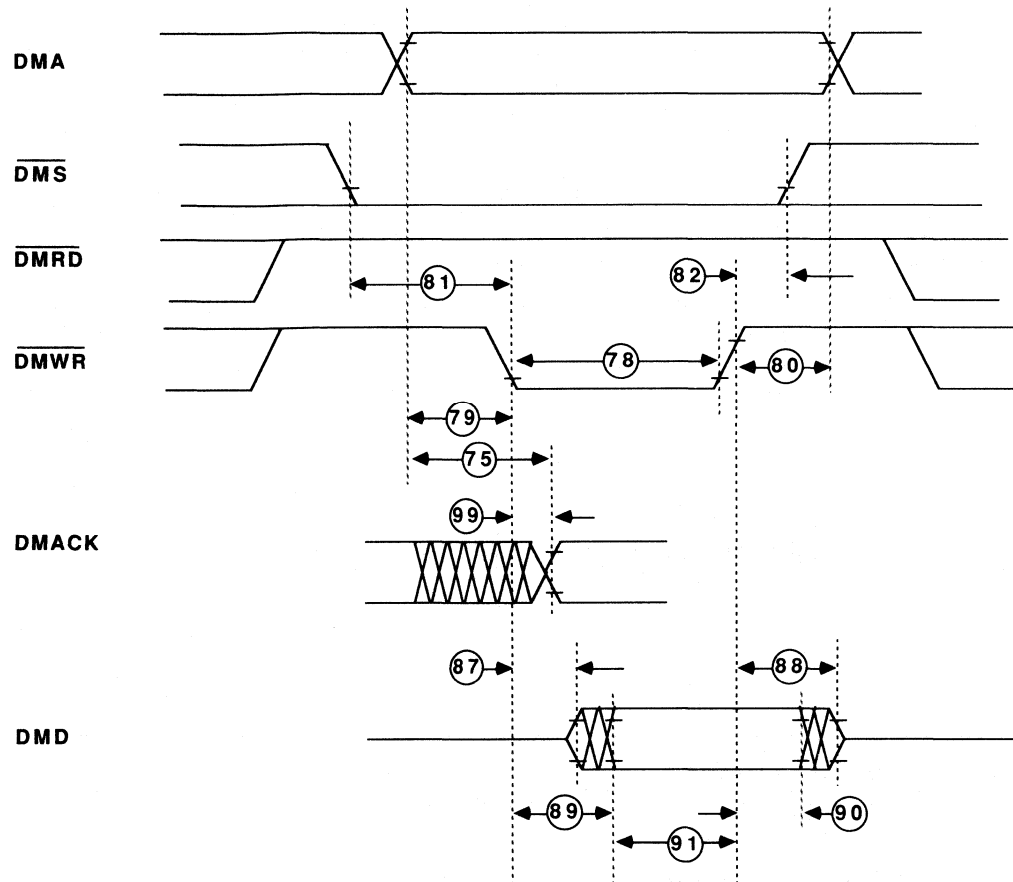


Figure 10a. Data Memory Write

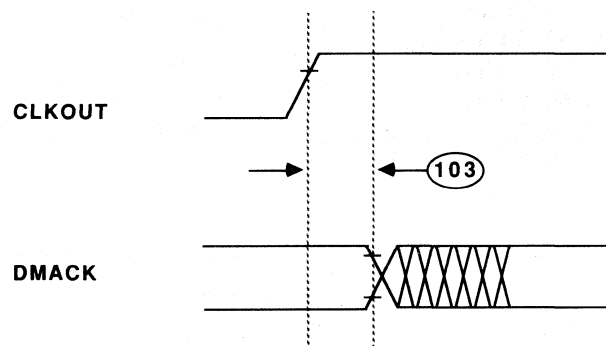


Figure 10b. Data Memory Wait States Extended with DMACK

ADSP-2100/ADSP-2100A

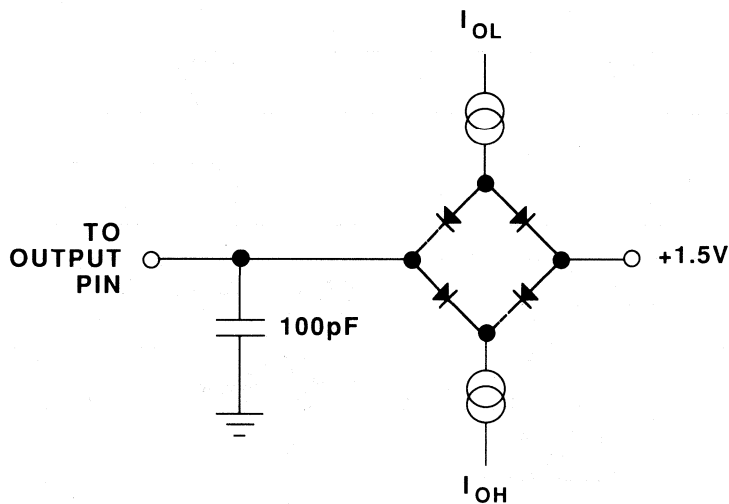


Figure 11. Normal Load for AC Measurements

Code	Status Condition	True If:
EQ	ALU Equal Zero	AZ = 1
NE	ALU Not Equal Zero	AZ = 0
LT	ALU Less Than Zero	AN .XOR. AV = 1
GE	ALU Greater Than or Equal Zero	AN .XOR. AV = 0
LE	ALU Less Than or Equal Zero	(AN .XOR. AV) .OR. AZ = 1
GT	ALU Greater Than Zero	(AN .XOR. AV) .OR. AZ = 0
AC	ALU Carry	AC = 1
NOT AC	Not ALU Carry	AC = 0
AV	ALU Overflow	AV = 1
NOT AV	Not ALU Overflow	AV = 0
MV	MAC Overflow	MV = 1
NOT MV	Not MAC Overflow	MV = 0
NEG	ALU X Input Sign Negative	AS = 1
POS	ALU X Input Sign Positive	AS = 0
NOT CE	Not Counter Expired	CE $\neq$ 0
TRUE	True	Always True

Table 2. Condition Codes

AX0, AX1	Data Registers (dreg)	
AY0, AY1		
AR		
MX0, MX1		
MY0, MY1		
MR0, MR1, MR2		
SI		
SE		
SR0, SR1		
SB		
PX	Accessible Registers (reg)	
I0, I1, I2, I3, I4, I5, I6, I7		
M0, M1, M2, M3, M4, M5, M6, M7		
L0, L1, L2, L3, L4, L5, L6, L7		
CNTR		
ASTAT		
MSTAT		
SSTAT		
IMASK		
ICNTL		

Table 3. Register Classification

ALU		
Source for X input port (xop)	Source for Y input port (yop)	Destination for output port R
AX0, AX1 AR MR0, MR1, MR2 SR0, SR1	AY0, AY1 AF	AR AF
MAC		
Source for X input port (xop)	Source for Y input port (yop)	Destination for output port R
MX0, MX1 AR MR0, MR1, MR2 SR0, SR1	MY0, MY1 MF	MR (MR2, MR1, MR0) MF
Shifter		
Source for Shifter input (xop)		Destination for Shifter output
SI AR MR0, MR1, MR2 SR0, SR1		SR (SR1, SR0)

Table 4. Computational Input/Output Registers

ADSP-2100/ADSP-2100A

These conventions are used in Table 5.

1. All keywords are shown in capital letters.
2. Brackets enclose optional parts of the syntax.
3. Vertical lines indicate that one parameter must be chosen from those enclosed.
4. Table 2 defines the conditions for *condition*.
5. Table 3 defines the set of registers for *dreg* and *reg*.
6. Table 4 defines the set of registers for *xop* and *yop*.
7. <data> represents an immediate value.
8. <address> may be an immediate value or label.
9. <comp>, in a multifunction instruction, represents all legal ALU, MAC or Shifter operations with these restrictions:
 - All operations are performed unconditionally
 - Shift Immediate operations are not allowed
 - ALU division (DIVS, DIVQ) is not allowed.

DATA MOVE INSTRUCTIONS

Register Move

reg = reg;

Load Register Immediate

reg = <data>;

Data Memory Read (direct address)

reg = DM (<address>;

Data Memory Read (indirect address)

dreg = DM (

I0	M0
I1	M1
I2	M2
I3	M3
I4	M4
I5	M5
I6	M6
I7	M7

);

Program Memory Read (indirect address)

dreg = PM (

I4	M4
I5	M5
I6	M6
I7	M7

);

Data Memory Write (direct address)

DM (<address>) = reg;

Data Memory Write (indirect address)

DM (

I0	M0
I1	M1
I2	M2
I3	M3
I4	M4
I5	M5
I6	M6
I7	M7

) = dreg; <data>

Program Memory Write (Indirect address)

PM (

I4	M4
I5	M5
I6	M6
I7	M7

) = dreg;

COMPUTATIONAL INSTRUCTIONS: ALU

Add/Add with Carry

[IF condition]

AR
AF

 = xop

+yop
+C
+ yop + C

 ;

Subtract X-Y/Subtract X-Y with Borrow

[IF condition]

AR
AF

 = xop

-yop
-yop + C - 1

 ;

Subtract Y-X/Subtract with Borrow

[IF condition]

AR
AF

 = yop

-xop
-xop + C - 1

 ;

AND, OR, Exclusive OR

[IF condition]

AR
AF

 = xop

AND
OR
XOR

 yop ;

Pass/Clear

[IF condition]

AR
AF

 = PASS

xop
yop

 ;

Negative

[IF condition]

AR
AF

 = -

xop
yop

 ;

NOT

[IF condition]

AR
AF

 = NOT

xop
yop

 ;

Absolute Value

[IF condition]

AR
AF

 = ABS

xop
yop

 ;

Increment

[IF condition]

AR
AF

 = yop + 1 ;

Decrement

[IF condition]

AR
AF

 = yop - 1 ;

Divide

DIVS yop, xop ;
DIVQ xop ;

COMPUTATIONAL INSTRUCTIONS: SHIFTER

Arithmetic Shift

[IF condition] $SR = [SR \text{ OR}] \text{ ASHIFT } xop \begin{pmatrix} (HI) \\ (LO) \end{pmatrix} ;$

Logical Shift

[IF condition] $SR = [SR \text{ OR}] \text{ LSHIFT } xop \begin{pmatrix} (HI) \\ (LO) \end{pmatrix} ;$

Normalize

[IF condition] $SR = [SR \text{ OR}] \text{ NORM } xop \begin{pmatrix} (HI) \\ (LO) \end{pmatrix} ;$

Derive Exponent

[IF condition] $SE = \text{EXP } xop \begin{pmatrix} (HI) \\ (LO) \\ (HIX) \end{pmatrix} ;$

Block Exponent Adjust

[IF condition] $SB = \text{EXPADJ } xop ;$

Arithmetic Shift Immediate

$SR = [SR \text{ OR}] \text{ ASHIFT } xop \text{ BY } \langle \text{data} \rangle \begin{pmatrix} (HI) \\ (LO) \end{pmatrix} ;$

Logical Shift Immediate

$SR = [SR \text{ OR}] \text{ LSHIFT } xop \text{ BY } \langle \text{data} \rangle \begin{pmatrix} (HI) \\ (LO) \end{pmatrix} ;$

COMPUTATIONAL INSTRUCTIONS: MAC

Multiply

[IF condition] $\begin{pmatrix} MR \\ MF \end{pmatrix} = xop * yop \begin{pmatrix} SS \\ SU \\ US \\ UU \\ RND \end{pmatrix} ;$

Multiply Accumulate

[IF condition] $\begin{pmatrix} MR \\ MF \end{pmatrix} = MR + xop * yop \begin{pmatrix} SS \\ SU \\ US \\ UU \\ RND \end{pmatrix} ;$

Multiply Subtract

[IF condition] $\begin{pmatrix} MR \\ MF \end{pmatrix} = MR - xop * yop \begin{pmatrix} SS \\ SU \\ US \\ UU \\ RND \end{pmatrix} ;$

Clear

[IF condition] $\begin{pmatrix} MR \\ MF \end{pmatrix} = 0 ;$

Transfer MR

[IF condition] $\begin{pmatrix} MR \\ MF \end{pmatrix} = MR [RND] ;$

Conditional MR Saturation

IF MV SAT MR ;

PROGRAM FLOW CONTROL INSTRUCTION

Jump

[IF condition] Jump ($\begin{pmatrix} I4 \\ I5 \\ I6 \\ I7 \\ \langle \text{address} \rangle \end{pmatrix}) ;$

Call

[IF condition] CALL ($\begin{pmatrix} I4 \\ I5 \\ I6 \\ I7 \\ \langle \text{address} \rangle \end{pmatrix}) ;$

Return from Subroutine

[IF condition] RTS ;

Return from Interrupt

[IF condition] RTI ;

Do Until

DO $\langle \text{address} \rangle$ [UNTIL condition] ;

Trap

[IF condition] TRAP ;

MULTIFUNCTION INSTRUCTIONS

Computation with Memory Read

$\langle \text{comp} \rangle, dreg = \begin{pmatrix} DM \\ \begin{pmatrix} I0 \\ I1 \\ I2 \\ I3 \\ I4 \\ I5 \\ I6 \\ I7 \end{pmatrix} \\ PM \end{pmatrix} \begin{pmatrix} M0 \\ M1 \\ M2 \\ M3 \\ M4 \\ M5 \\ M6 \\ M7 \end{pmatrix} ;$

Computation with Data Register Move

$\langle \text{comp} \rangle, dreg = dreg ;$

Computation with Memory Write

$DM \begin{pmatrix} I0 \\ I1 \\ I2 \\ I3 \\ I4 \\ I5 \\ I6 \\ I7 \end{pmatrix} \begin{pmatrix} M0 \\ M1 \\ M2 \\ M3 \\ M4 \\ M5 \\ M6 \\ M7 \end{pmatrix} = dreg, \langle \text{comp} \rangle ;$

ADSP-2100/ADSP-2100A

Data & Program Memory Read

$$\begin{array}{|c|} \hline \text{AX0} \\ \hline \text{AX1} \\ \hline \text{MX0} \\ \hline \text{MX1} \\ \hline \end{array} = \text{DM} \left(\begin{array}{|c|} \hline \text{I0} \\ \hline \text{I1} \\ \hline \text{I2} \\ \hline \text{I3} \\ \hline \end{array}, \begin{array}{|c|} \hline \text{M0} \\ \hline \text{M1} \\ \hline \text{M2} \\ \hline \text{M3} \\ \hline \end{array} \right), \begin{array}{|c|} \hline \text{AY0} \\ \hline \text{AY1} \\ \hline \text{MY0} \\ \hline \text{MY1} \\ \hline \end{array} = \text{PM} \left(\begin{array}{|c|} \hline \text{I4} \\ \hline \text{I5} \\ \hline \text{I6} \\ \hline \text{I7} \\ \hline \end{array}, \begin{array}{|c|} \hline \text{M4} \\ \hline \text{M5} \\ \hline \text{M6} \\ \hline \text{M7} \\ \hline \end{array} \right);$$

ALU/MAC Operation with Data & Program Memory Read*

$$\begin{array}{|c|} \hline <\text{ALU}> \\ \hline <\text{MAC}> \\ \hline \end{array}, \begin{array}{|c|} \hline \text{AX0} \\ \hline \text{AX1} \\ \hline \text{MX0} \\ \hline \text{MX1} \\ \hline \end{array} = \text{DM} \left(\begin{array}{|c|} \hline \text{I0} \\ \hline \text{I1} \\ \hline \text{I2} \\ \hline \text{I3} \\ \hline \end{array}, \begin{array}{|c|} \hline \text{M0} \\ \hline \text{M1} \\ \hline \text{M2} \\ \hline \text{M3} \\ \hline \end{array} \right), \begin{array}{|c|} \hline \text{AY0} \\ \hline \text{AY1} \\ \hline \text{MY0} \\ \hline \text{MY1} \\ \hline \end{array} = \text{PM} \left(\begin{array}{|c|} \hline \text{I4} \\ \hline \text{I5} \\ \hline \text{I6} \\ \hline \text{I7} \\ \hline \end{array}, \begin{array}{|c|} \hline \text{M4} \\ \hline \text{M5} \\ \hline \text{M6} \\ \hline \text{M7} \\ \hline \end{array} \right);$$

*ALU Division operations not allowed.

MISCELLANEOUS INSTRUCTIONS

Stack Control

[[PUSH] STS] [, POP CNTR] [, POP PC] [, POP LOOP] ;
[[POP]]

Mode Control

[[ENA] BIT_REV] [[ENA] AV_LATCH] [[ENA] AR_SAT] [[ENA] SEC_REG] ;
[[DIS]] [[DIS]] [[DIS]] [[DIS]]

Modify Address Register

MODIFY ($\begin{array}{|c|} \hline \text{I0} \\ \hline \text{I1} \\ \hline \text{I2} \\ \hline \text{I3} \\ \hline \end{array}, \begin{array}{|c|} \hline \text{M0} \\ \hline \text{M1} \\ \hline \text{M2} \\ \hline \text{M3} \\ \hline \end{array} \right) ;$

No Operation

NOP ;

Table 5. Instruction Set Summary

1.1 Scope.

This specification covers the detail requirements for a CMOS monolithic 32-bit and 64-bit IEEE Standard 754 format floating-point multiplier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	ADSP-3210SG/883B
–2	ADSP-3210TG/883B
–3	ADSP-3210UG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-100A.

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3V to 7V
Input Voltage	–0.3V to V_{DD}
Output Voltage	–0.3V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-3210 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	– 1, 2, 3	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input High Voltage, CLK and Asynchronous Controls (RESET, MSWSEL, OEN)	V _{IHA}	– 1, 2, 3	3.0	3.0	3.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	– 1, 2, 3	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	– 1, 2, 3	2.4	2.4	2.4			V _{DD} = min I _{OH} = – 1mA	V min
Digital Output Low Voltage*	V _{OL}	– 1, 2, 3	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4mA	V max
Digital Input High Current	I _{IH}	– 1, 2, 3	10	10	10			V _{DD} = max V _{IN} = +5.0V	μA max
Digital Input Low Current	I _{IL}	– 1, 2, 3	10	10	10			V _{DD} = max V _{IN} = 0.0V	μA max
Three-State Leakage Current	I _{OZ}	– 1, 2, 3	50	50	50			V _{DD} = max High Z, V _{IN} = 0V or max	μA max
Supply Current	I _{DD1}	– 1	150	200	200			@ max Clock Rate, TTL Inputs All V _{IN} = 2.4V	mA max
	I _{DD2}	– 2, 3	50	60	60				mA max
Clock Cycle	t _{CY}	– 1	125			150	150	Note 2	ns max
		– 2	100			125	125		
		– 3	60			75	75		
Clock LO	t _{CL}	– 1, 2, 3	20			30	30	Note 2	ns min
Clock HI	t _{CH}	– 1, 2, 3	20			30	30	Note 2	ns min
Data & Control Setup	t _{DS}	– 1	20			25	25	Note 2	ns min
		– 2, 3	15			20	20		
Data & Control Hold	t _{DH}	– 1, 2, 3	3			3	3	Note 2	ns min
Data Output Delay	t _{DO}	– 1	30			35	35	Note 2	ns max
		– 2, 3	25			30	30		
Status Output Delay	t _{SO}	– 1	30			35	35	Note 2	ns max
		– 2, 3	25			30	30		
MSWSEL-to-Data Delay	t _{ENO}	– 1	25			30	30	Note 2	ns max
		– 2, 3	20			25	25		
Three-State Disable Delay*	t _{DIS}	– 1	18			25	25	Notes 2 & 3	ns max
		– 2, 3	15			20	20		
Three-State Enable Delay*	t _{ENA}	– 1	25			30	30	Notes 2, 3 & 4	ns max
		– 2, 3	20			25	25		
RESET Setup*	t _{SU}	– 1	20			25	25	Note 2	ns min
		– 2, 3	15			25	25		
RESET Pulse Duration*	t _{RS}	– 1, 2, 3	50			75	75	Note 2	ns min

Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units	
Operation Time (With or Without Direct Operand Feed): 32-Bit Multiplication	t _{OPD}	– 1	125			150	150	Note 2	ns max	
		– 2	100			125	125			
		– 3	60			75	75			
		64-Bit Multiplication	– 1	500			600	600	Note 2	ns max
			– 2	400			500	500		
			– 3	240			300	300		
Hold Setup	t _{HS}	– 1	20			22	22	Note 2	ns min	
		– 2, 3	15			18	18			
Hold Hold	t _{HH}	– 1, 2, 3	3			3	3	Note 2	ns min	
Total Latency ⁵ (With Direct Operand Feed): 32-Bit Multiplication	t _{LAD}	– 1	363			435	435	Note 2	ns max	
		– 2	290			363	363			
		– 3	190			238	238			
		64-Bit Multiplication	– 1	738			885	885	Note 2	ns max
			– 2	590			738	738		
			– 3	370			463	463		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

¹T_A = +25°C; V_{DD} = +4.5V min to +5.5V max (unless otherwise noted).

²Input levels are GND and +3.0V; V_{DD} = +4.5V, and timing transitions per Figures 1 through 7, measured at +1.5V.

³Transitions measured per Figure 1.

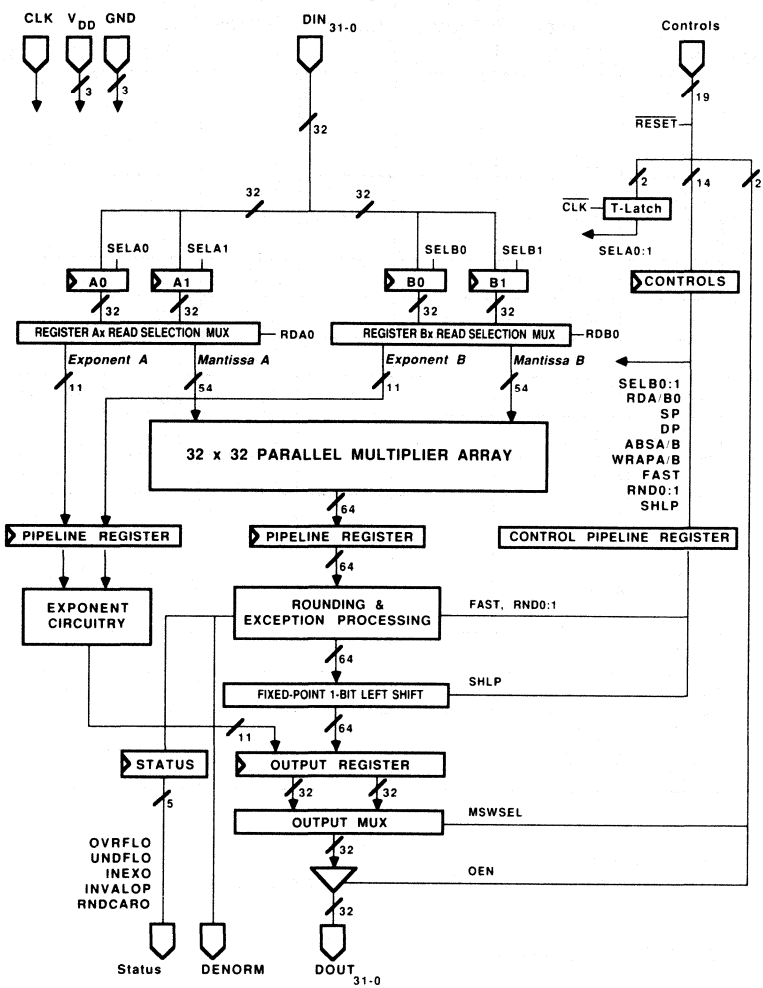
⁴3ns min.

⁵Total latency = (data setup + processing + output delay of MSW) in Direct Operand Feed Mode.

Table 1.

ADSP-3210

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

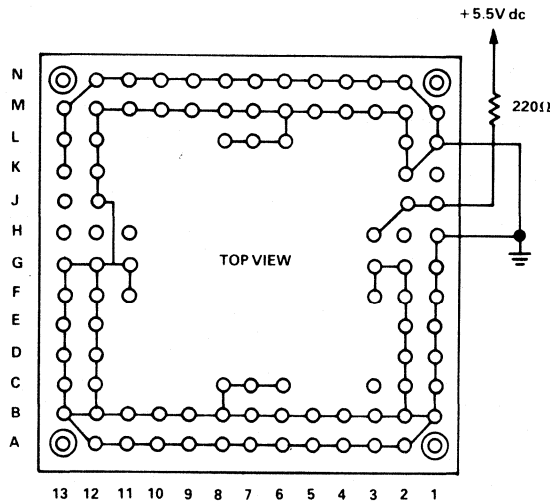
PIN	FUNCTION	PIN	FUNCTION
B2	DIN3	M12	DOUT28
B1	DIN2	M13	DOUT29
C2	DIN1	L12	DOUT30
C1	DIN0	L13	DOUT31
D2	WRAPB	K12	GND
D1	RDB0	K13	GND
E2	SELB0	J12	GND
E1	SELB1	J13	DENORM
F3	ABSB	H11	INVALOP
F2	DP	H12	OVRFLO
F1	SP	H13	UNDFLO
G2	CLK	G12	OEN
G3	RESET	G11	MSWSEL
G1	RND1	G13	SHLP
H1	RND0	F13	FAST
H2	RNDCARO	F12	ABSA
H3	VDD	F11	SELA1
J1	VDD	E13	SELA0
J2	VDD	E12	RDA0
K1	INEXO	D13	WRAPA
K2	DOUT0	D12	DIN31
L1	DOUT1	C13	DIN30
M1	DOUT2	B13	DIN29
L2	DOUT3	C12	DIN28
N1	N/C	A13	N/C
M2	DOUT4	B12	DIN27
N2	DOUT5	A12	DIN26
M3	DOUT6	B11	DIN25
N3	DOUT7	A11	DIN24
M4	DOUT8	B10	DIN23
N4	DOUT9	A10	DIN22
M5	DOUT10	B9	DIN21
N5	DOUT11	A9	DIN20
L6	DOUT12	C8	DIN19
M6	DOUT13	B8	DIN18
N6	DOUT14	A8	DIN17
M7	DOUT15	B7	DIN16
L7	DOUT16	C7	DIN15
N7	DOUT17	A7	DIN14
M8	DOUT18	A6	DIN13
N8	DOUT19	B6	DIN12
L8	DOUT20	C6	DIN11
N9	DOUT21	A5	DIN10
M9	DOUT22	B5	DIN9
N10	DOUT23	A4	DIN8
M10	DOUT24	B4	DIN7
N11	DOUT25	A3	DIN6
M12	DOUT26	A2	DIN5
N13	DOUT27	B3	DIN4
N13	N/C	A1	N/C

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



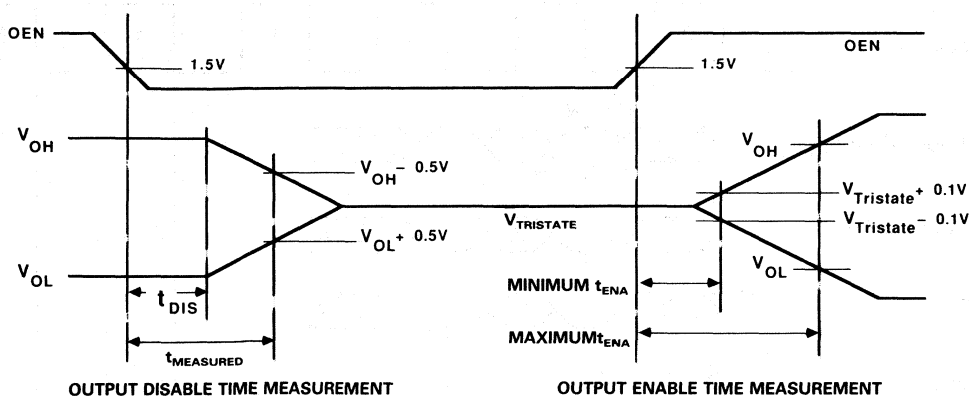


Figure 1. ADSP-3210 Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA} , is the earliest that outputs begin to drive. It is measured from the control signal OEN reaching 1.5 V to the point at which the fastest outputs have changed by 0.1 V from $V_{TRISTATE}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

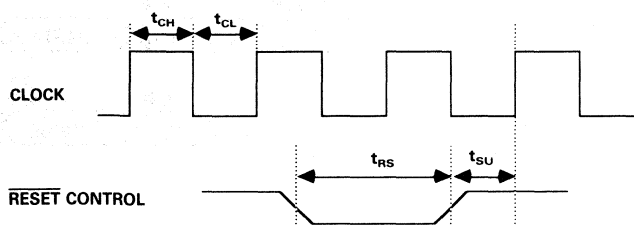


Figure 2. ADSP-3210 Reset Timing

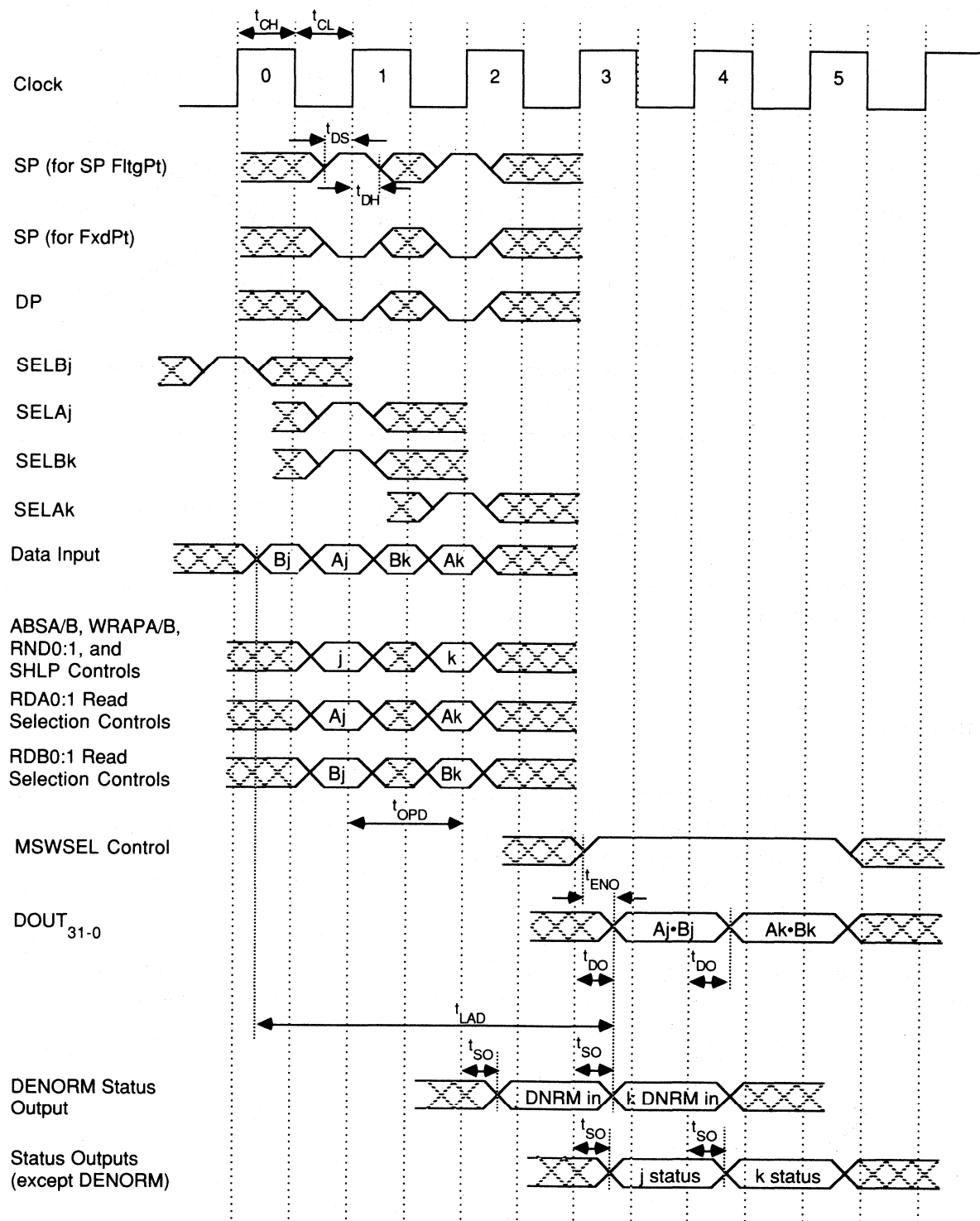


Figure 3. ADSP-3210 32-Bit Single-Precision Floating-Point and Fixed-Point Multiplications

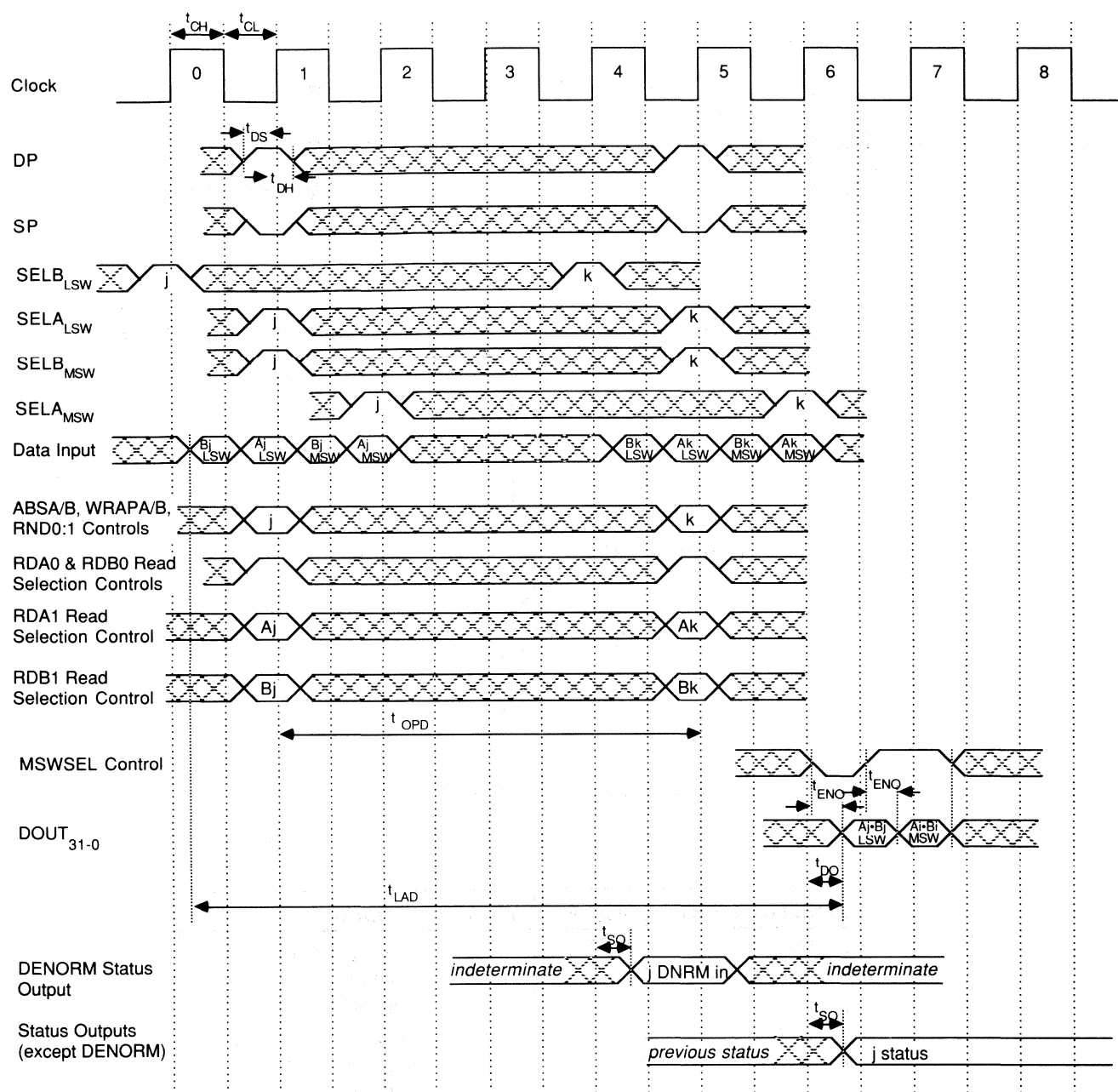


Figure 4. ADSP-3210 64-Bit Double-Precision Floating-Point Multiplications

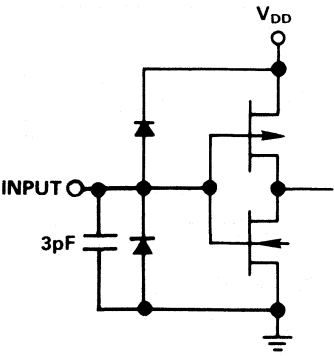


Figure 5. Equivalent Input Circuits

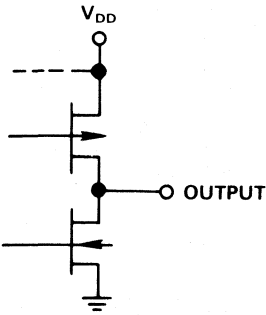


Figure 6. Equivalent Output Circuits

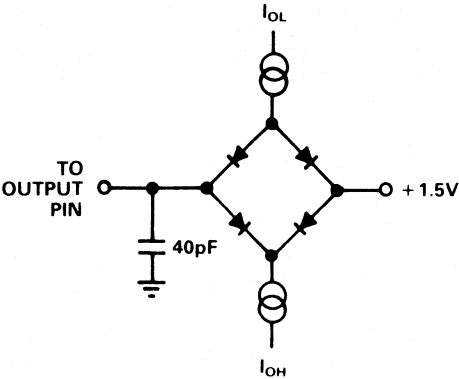


Figure 7. Normal Load for AC Measurements

INSTRUCTION	WRAPA	WRAPB	COMMENT
A*B	0	0	Multiply Normalized Floating Point Operands A Times B.
WA*B	1	0	Multiply Wrapped Operand A Times Operand B.
A*WB	0	1	Multiply Operand A Times Wrapped Operand B.
WA*WB	1	1	Multiply Wrapped Operand A Times Wrapped Operand B.

Table 2. ADSP-3210 Instruction Set

5.0 Notation Used in the Tables Below:

RN = Round to the Nearest Number
 RP = Round toward Plus Infinity
 RM = Round toward Minus Infinity
 RZ = Round toward Zero

NORM = Normalized number

DNRM = Denormalized number. A Denormalized number is treated as zero internally.

WNRM = Wrapped number. A wrapped number is a number with a normalized fraction and an exponent that has been decremented through zero to take on a twos complement negative value.

UNRM = Unnormalized number. An Unnormal is an Underflowed and Wrapped Number. An UNRM can result from a multiplication of 1 or 2 Wrapped Numbers.

NORM.MAX = Maximum Normalized Number Representable in the Destination Format

NORM.MIN = Minimum Normalized Number Representable in the Destination Format

OVF = Overflowed Number

UNDF = Underflowed Number

INV = Invalid Operand

INF = Infinity

OK = No Exception Status Generated

In the tables below, the first mnemonic in each box describes the flag that is set, the second is the result on the DOUT pins.

		B operand		ZERO		DNRM		WRAP		NORM		INF		NAN	
		result	status	result	status	result	status	result	status	result	status	result	status	result	status
A operand	ZERO	ZERO		ZERO		ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
	DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	ZERO	DENORM	ZERO	DENORM	INF		NAN	INVALOP
	WRAP	ZERO		ZERO	DENORM	UNRM	UNDFLO	NORM WRAP UNRM	UNDFLO UNDFLO			INF		NAN	INVALOP
	NORM	ZERO		ZERO	DENORM	NORM WRAP UNRM	UNDFLO UNDFLO	INF.NORM.MAX ¹ NORM WRAP	OVRFLO UNDFLO	INF				NAN	INVALOP
	INF	NAN	INVALOP	INF		INF		INF		INF		INF		NAN	INVALOP
	NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."

Table 3. ADSP-3210 Floating-Point Multiplication (IEEE Mode)

		B operand		ZERO		DNRM		NORM		INF		NAN	
		result	status	result	status	result	status	result	status	result	status	result	status
A operand	ZERO	ZERO		ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
	DNRM	ZERO		ZERO	DENORM	ZERO	DENORM			NAN	INVALOP	NAN	INVALOP
	NORM	ZERO		ZERO	DENORM	INF.NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	INF				NAN	INVALOP
	INF	NAN	INVALOP	INF	INVALOP	INF		INF		INF		NAN	INVALOP
	NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."

2. In FAST mode, WRAP inputs are illegal.

Table 4. ADSP-3210 Floating-Point Multiplication (FAST Mode)

1.1 Scope.

This specification covers the detail requirements for a CMOS monolithic 32-bit and 64-bit IEEE Standard 754 format floating-point multiplier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-3211SG/883B
-2	ADSP-3211TG/883B
-3	ADSP-3211UG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-144A.

1.3 Absolute Maximum Ratings.

Supply Voltage	 -0.3 V to 7 V
Input Voltage	 -0.3 V to V_{DD}
Output Voltage	 -0.3 V to V_{DD}
Operating Temperature Range (Ambient)	 -55°C to +125°C
Storage Temperature Range	 -65°C to +150°C
Lead Temperature (Soldering 10 sec)	 +300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-3211 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	-1, 2, 3	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input High Voltage, CLK and Asynchronous Controls RESET, MSWSEL, OEN	V _{IHA}	-1, 2, 3	3.0	3.0	3.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	-1, 2, 3	2.4	2.4	2.4			V _{DD} = min I _{OH} = -1 mA	V min
Digital Output Low Voltage	V _{OL}	-1, 2, 3	0.4	0.6	0.6			V _{DD} = min I _{OH} = +4 mA	V max
Digital Input High Current	I _{IH}	-1, 2, 3	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	-1, 2, 3	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current	I _{OZ}	-1, 2, 3	50	50	50			V _{DD} = max High Z, V _{IN} = 0 V or max	μA max
Supply Current	I _{DD1}	-1, 2, 3	150	200	200			@ max Clock Rate, TTL Inputs	mA max
	I _{DD2}		50	60	60			All V _{IN} = 2.4 V	mA max
Clock Cycle	t _{CY}	-1	125			150	150	Note 2	ns max
		-2	100			125	125		
		-3	60			75	75		
Clock LO	t _{CL}	-1, 2, 3	20			30	30	Note 2	ns min
Clock HI	t _{CH}	-1, 2, 3	20			30	30	Note 2	ns min
Data & Control Setup	t _{DS}	-1	20			25	25	Note 2	ns min
		-2, 3	15			20	20		
Data & Control Hold	t _{DH}	-1, 2, 3	3			3	3	Note 2	ns min
Data Output Delay	t _{DO}	-1	30			35	35	Note 2	ns max
		-2, 3	25			30	30		
Status Output Delay	t _{SO}	-1	30			35	35	Note 2	ns max
		-2, 3	25			30	30		
MSWSEL-to-Data Delay	t _{ENO}	-1	25			30	30	Note 2	ns max
		-2, 3	20			25	25		
Three-State Disable Delay	t _{DIS}	-1	18			25	25	Notes 2 & 3	ns max
		-2, 3	15			20	20		
Three-State Enable Delay	t _{ENA}	-1	25			30	30	Notes 2, 3 & 5	ns max
		-2, 3	20			25	25		
RESET Setup	t _{SU}	-1	20			25	25	Note 2	ns min
		-2, 3	15			25	25		
RESET Pulse Duration	t _{RS}	-1, 2, 3	50			75	75	Note 2	ns min

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Operation Time (With or Without Direct Operand Feed): 32-Bit Multiplication 64-Bit Multiplication	t_{OPD}	-1	125			150	150	Note 2	ns max
		-2	100			125	125	Note 2	ns max
		-3	60			70	70		
		-1	500			600	600		
		-2	400			500	500		
		-3	240			280	280		
Hold Setup	t_{HS}	-1	20			22	22	Note 2	ns min
		-2	15			18	18	Note 2	ns min
		-3	15			20	20		
Hold Hold	t_{HH}	-1, 2, 3	3			3	3	Note 2	ns min
Total Latency ⁴ (With Direct Operand Feed): 32-Bit Multiplication 64-Bit Multiplication	t_{LAD}	-1	300			360	360	Note 2	ns max
		-2	240			300	300	Note 2	ns max
		-3	140			190	190		
		-1	738			885	885		
		-2	590			738	738		
		-3	315			400	400		

NOTES

¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²Input levels are GND and +3.0 V; V_{DD} = +4.5 V, and timing transitions, per Figures 1 through 7, measured at +1.5 V.

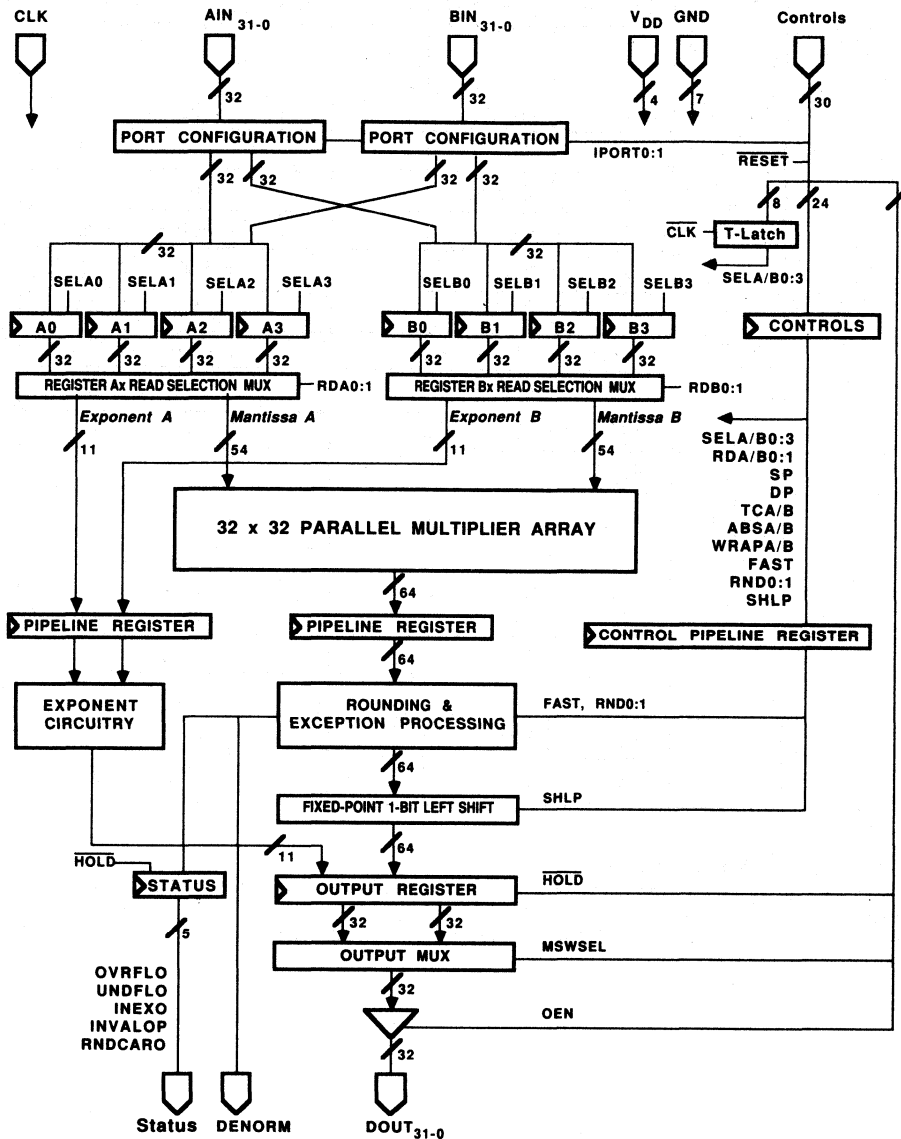
³Transitions measured per Figure 1.

⁴Total latency = (data setup + processing + output delay of MSW) in Direct Operand Feed Mode.

⁵3 ns minimum.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

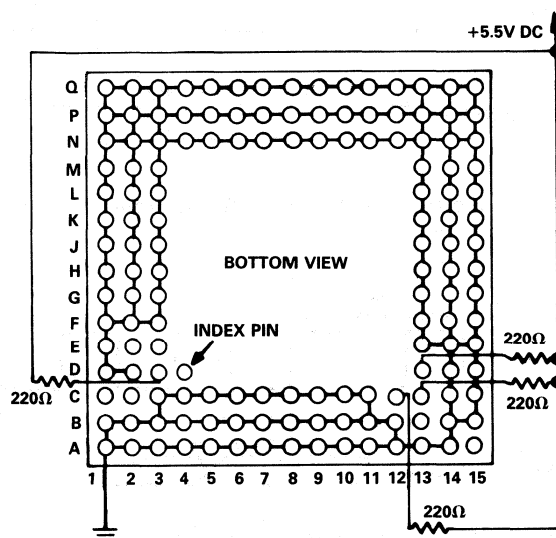
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	DOUT31	P5	AIN11	G13	RDB1
A2	DOUT27	N5	AIN13	F15	WRAPB
A3	DOUT23	O6	AIN4	F14	CLK
B1	GND	P6	AIN8	F13	GND
B2	DOUT30	N6	AIN9	E15	SP
B3	DOUT26	Q7	AIN3	E14	DP
C1	OVRFLO	P7	AIN6	E13	GND
C2	DENORM	N7	AIN5	D15	RND1
C3	DOUT29	Q8	AIN1	D14	RESET
D1	TCA	P8	AIN2	D13	V _{DD}
D2	GND	N8	AIN0	C15	RND0
D3	V _{DD}	Q9	BIN30	C14	GND
E1	SHLP	P9	BIN28	C13	V _{DD}
E2	UNDFLO	N9	BIN31	B15	TCB
E3	INVALOP	Q10	BIN29	B14	HOLD
F1	ABSA	P10	BIN27	B13	INEXO
F2	MSWSEL	N10	BIN26	A15	RNDCARO
F3	OEN	Q11	BIN25	A14	DOUT0
G1	RDA0	P11	BIN24	A13	DOUT3
G2	FAST	N11	BIN20	A12	DOUT5
G3	WRAPA	Q12	BIN23	B12	DOUT1
H1	SELA0	P12	BIN21	C12	V _{DD}
H2	RDA1	N12	BIN17	A11	DOUT8
H3	SELA2	Q13	BIN22	B11	DOUT4
J1	SELA3	P13	BIN19	C11	DOUT2
J2	IPOINT1	N13	BIN16	A10	DOUT11
J3	SELA1	Q14	BIN18	B10	DOUT7
K1	IPOINT0	P14	BIN15	C10	DOUT6
K2	AIN31	N14	BIN12	A9	DOUT12
K3	AIN30	Q15	BIN14	B9	DOUT9
L1	AIN29	P15	BIN11	C9	DOUT10
L2	AIN28	N15	BIN8	A8	DOUT14
L3	AIN24	M15	BIN6	B8	DOUT13
M1	AIN27	M14	BIN10	C8	GND
M2	AIN25	M13	BIN13	A7	DOUT15
M3	AIN21	L15	BIN3	B7	DOUT17
N1	AIN26	L14	BIN7	C7	GND
N2	AIN23	L13	BIN9	A6	DOUT16
N3	AIN20	K15	BIN0	B6	DOUT18
P1	AIN22	K14	BIN4	C6	DOUT19
P2	AIN19	K13	BIN5	A5	DOUT20
P3	AIN16	J15	SELB3	B5	DOUT21
Q1	AIN18	J14	BIN2	C5	DOUT25
Q2	AIN15	J13	BIN1	A4	DOUT22
Q3	AIN12	H15	SELB2	B4	DOUT24
Q4	AIN10	H14	SELB1	C4	DOUT26
P4	AIN14	H13	SELB0	D4	INDEX
N4	AIN17	G15	RDB0		
Q5	AIN7	G14	ABSB		

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



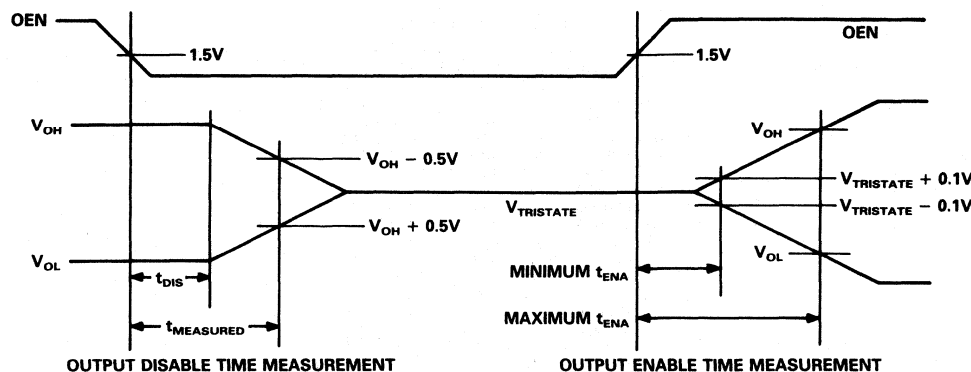


Figure 1. ADSP-3211 Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA} , is the earliest that outputs begin to drive. It is measured from the control signal OEN reaching 1.5 V to the point at which the fastest outputs have changed by 0.1 V from $V_{TRISTATE}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

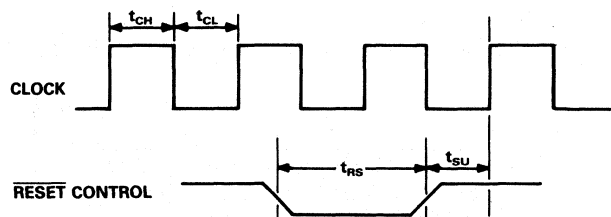


Figure 2. ADSP-3211 Reset Timing

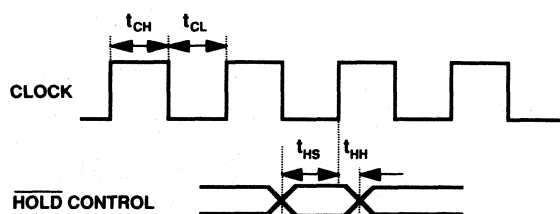


Figure 3. ADSP-3211 Multiplier Output Register Hold Timing

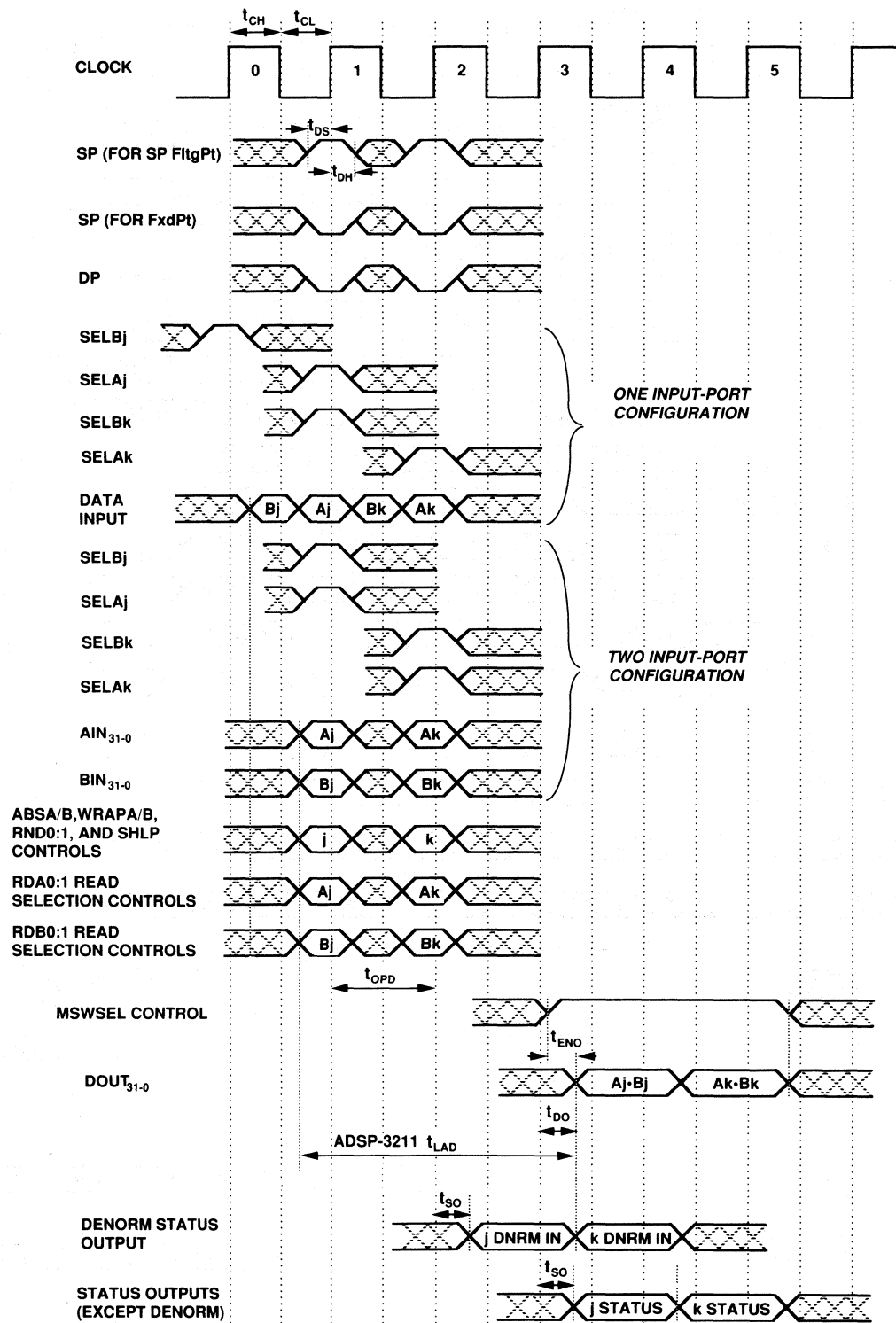


Figure 4. ADSP-3211 32-Bit Single-Precision Floating-Point and Fixed-Point Multiplications

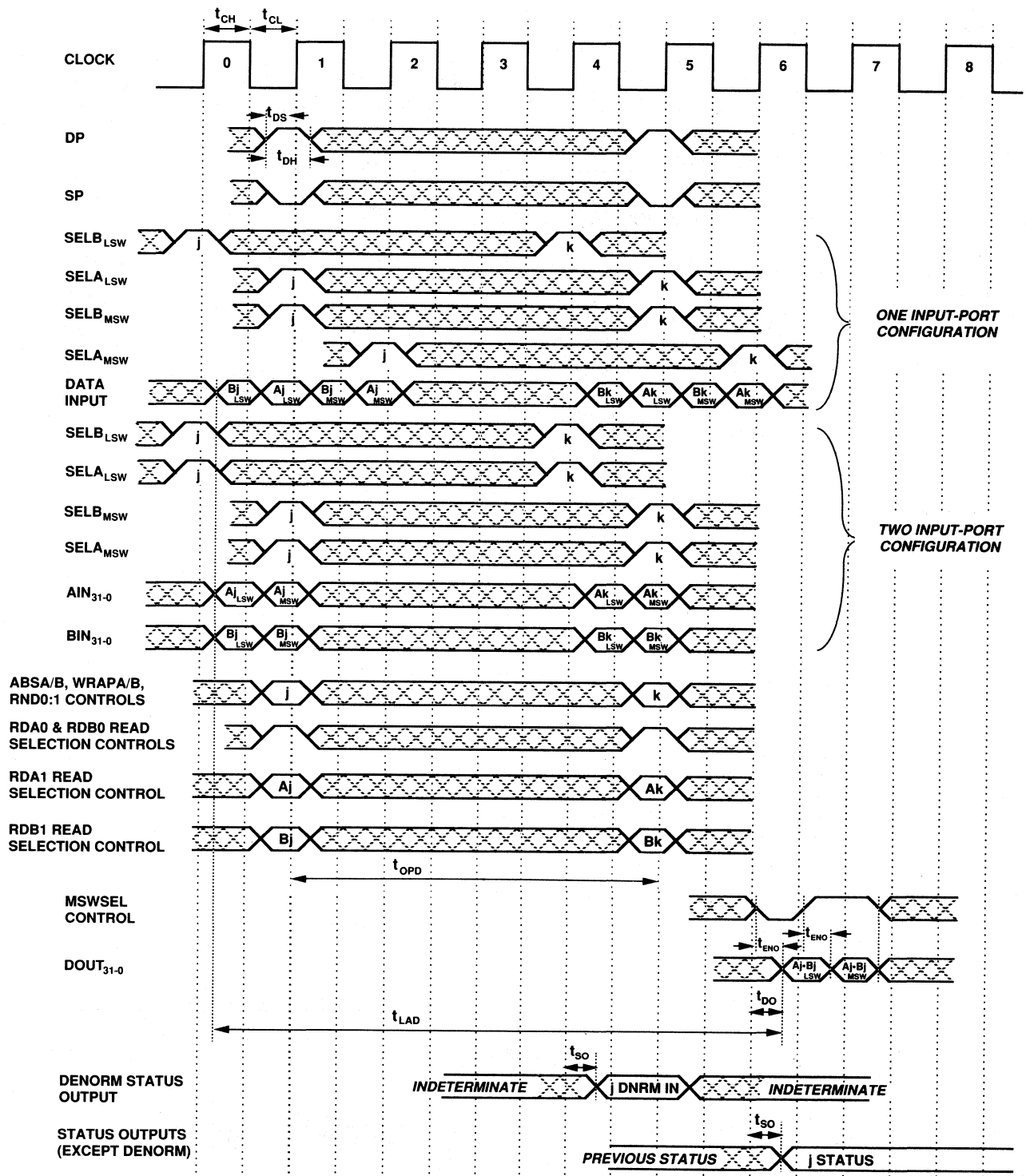


Figure 5. ADSP-3211 64-Bit Double-Precision Floating-Point Multiplications

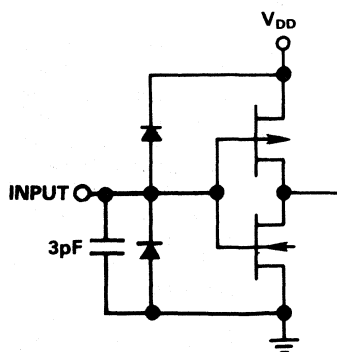


Figure 6. Equivalent Input Circuits

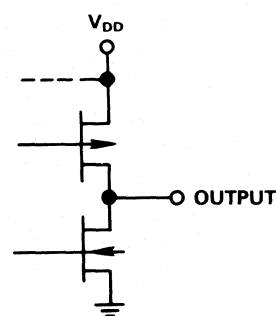


Figure 7. Equivalent Output Circuits

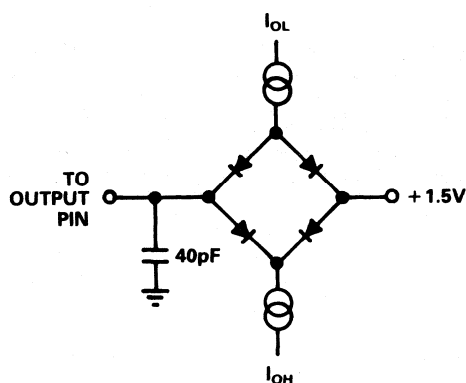


Figure 8. Normal Load for AC Measurements

INSTRUCTION	WRAPA	WRAPB	COMMENT
A*B	0	0	Multiply Normalized Floating Point Operands A times B.
WA*B	1	0	Multiply Wrapped Operand A Times Operand B.
A*WB	0	1	Multiply Operand A Times Wrapped Operand B.
WA*WB	1	1	Multiply Wrapped Operand A Times Wrapped Operand B.

Table 2. ADSP-3211 Instruction Set

5.0 Notation Used in the Tables Below:

RN	=	Round to the Nearest Number	UNRM	=	Unnormalized Number. An Unnormal Is an Underflowed and Wrapped Number. An UNRM Can Result from a Multiplication of 1 or 2 Wrapped Numbers.
RP	=	Round toward Plus Infinity			
RM	=	Round toward Minus Infinity			
RZ	=	Round toward Zero			
NORM	=	Normalized Number	NORM.MAX	=	Maximum Normalized Number Representable in the Destination Format
DNRM	=	Denormalized Number. A Denormalized Number Is Treated as Zero Internally.	NORM.MIN	=	Minimum Normalized Number Representable in the Destination Format
WNRM	=	Wrapped Number. A Wrapped Number Is a Number with a Normalized Fraction and an Exponent that Has Been Decrementd through Zero to Take on a Twos Complement Negative Value.	OVF	=	Overflowed Number
			UNDF	=	Underflowed Number
			INV	=	Invalid Operand
			INF	=	Infinity
			OK	=	No Exception Status Generated

In the tables below, the first mnemonic in each box describes the flag that is set, the second is the result on the DOUT pins.

B operand		ZERO		DNRM		WRAP		NORM		INF		NAN	
		result	status	result	status	result	status	result	status	result	status	result	status
A operand	ZERO	ZERO		ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
	DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	ZERO	DENORM	INF		NAN	INVALOP
	WRAP	ZERO		ZERO	DENORM	UNRM	UNDFLO	NORM WRAP UNRM	UNDFLO UNDFLO	INF		NAN	INVALOP
	NORM	ZERO		ZERO	DENORM	NORM WRAP UNRM	UNDFLO UNDFLO	INF,NORM.MAX ¹ NORM WRAP	OVRFLO UNDFLO	INF		NAN	INVALOP
	INF	NAN	INVALOP	INF		INF		INF		INF		NAN	INVALOP
	NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode.

Table 3. ADSP-3211 Floating-Point Multiplication (IEEE Mode)

B operand		ZERO		DNRM		NORM		INF		NAN	
		result	status	result	status	result	status	result	status	result	status
A operand	ZERO	ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
	DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	NAN	INVALOP	NAN	INVALOP
	NORM	ZERO		ZERO	DENORM	INF,NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	INF		NAN	INVALOP
	INF	NAN	INVALOP	INF	INVALOP	INF		INF		NAN	INVALOP
	NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."

2. In FAST mode, WRAP inputs are illegal.

Table 4. ADSP-3211 Floating-Point Multiplication (FAST Mode)

1.1 Scope.

This specification covers the detail requirements for a CMOS monolithic 32-bit and 64-bit IEEE Standard 754 format floating-point arithmetic and logic unit (ALU).

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-3220SG/883B
-2	ADSP-3220TG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-144A.

1.3 Absolute Maximum Ratings.

Supply Voltage		-0.3V to 7V
Input Voltage		-0.3V to V_{DD}
Output Voltage		-0.3V to V_{DD}
Operating Temperature Range (Ambient)		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10sec)		+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-3220 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input High Voltage, CLK and Asynchronous Controls (RESET, MSWSEL, OEN & IPORT0:1)	V _{IHA}	– 1, 2	3.0	3.0	3.0			V _{DD} = max	V max
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	– 1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = – 1mA	V min
Digital Output Low Voltage*	V _{OL}	– 1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = + 4mA	V max
Digital Input High Current	I _{IH}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = + 5.0V	μA max
Digital Input Low Current	I _{IL}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0V	μA max
Three-State Leakage Current	I _{OZH}	– 1, 2	50	50	50			V _{DD} = max High Z, V _{IN} = 0V or max	μA max
	I _{OZL}		50	50	50				
Supply Current*	I _{DD1}	– 1, 2	150	200	200			@ max Clock Rate, TTL Inputs All V _{IN} = 2.4V	mA max
	I _{DD2}	– 1, 2	50	60	60				
Clock Cycle	t _{CY}	– 1	125			150	150	Note 2	ns max
		– 2	100			125	125		
Clock LO	t _{CL}	– 1, 2	20			30	30	Note 2	ns min
Clock HI	t _{CH}	– 1, 2	20			30	30	Note 2	ns min
Data & Control Setup	t _{DS}	– 1	20			25	25	Note 2	ns min
		– 2	15			20	20		
Data & Control Hold	t _{DH}	– 1, 2	3			3	3	Note 2	ns min
Data Output Delay	t _{DO}	– 1	30			35	35	Note 2	ns max
		– 2	25			30	30		
Status Output Delay	t _{SO}	– 1	30			35	35	Note 2	ns max
		– 2	25			30	30		
MSWSEL-to-Data Delay	t _{ENO}	– 1	25			30	30	Note 2	ns max
		– 2	20			25	25		
Three-State Disable Delay*	t _{DIS}	– 1	18			25	25	Notes 2 & 3	ns max
		– 2	15			20	20		
Three-State Enable Delay	t _{ENA}	– 1	25			30	30	Notes 2, 3 & 4	ns max
		– 2	20			25	25		
RESET Setup*	t _{SU}	– 1, 2	25			25	25	Note 2	ns min
RESET Pulse Duration*	t _{RS}	– 1, 2	75			75	75	Note 2	ns min
Operation Time (With or Without Direct Operand Feed): 32-Bit ALU Operation 64-Bit ALU Operation	t _{OPD}	– 1	125			150	150	Note 2	ns max
		– 2	100			125	125		
		– 1	125			150	150		
		– 2	100			125	125		

Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Hold Setup	t_{HS}	-1	20			22	22	Note 2	ns min
		-2	15			18	18		
Hold Hold	t_{HH}	-1, 2	3			3	3	Note 2	ns min
Total Latency ⁵ (With Direct Operand Feed): 32-Bit ALU Operation	t_{LAD}	-1	300			360	360	Note 2	ns max
		-2	240			300	300		
64-Bit ALU Operation		-1	363			435	435		
		-2	290			363	363		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

¹ $T_A = +25^\circ\text{C}$; $V_{DD} = +4.5\text{V min to } +5.5\text{V max}$ (unless otherwise noted).

²Input levels are GND and +3.0V; $V_{DD} = +4.5\text{V}$, and timing transitions per Figures 1 through 8, measured at +1.5V.

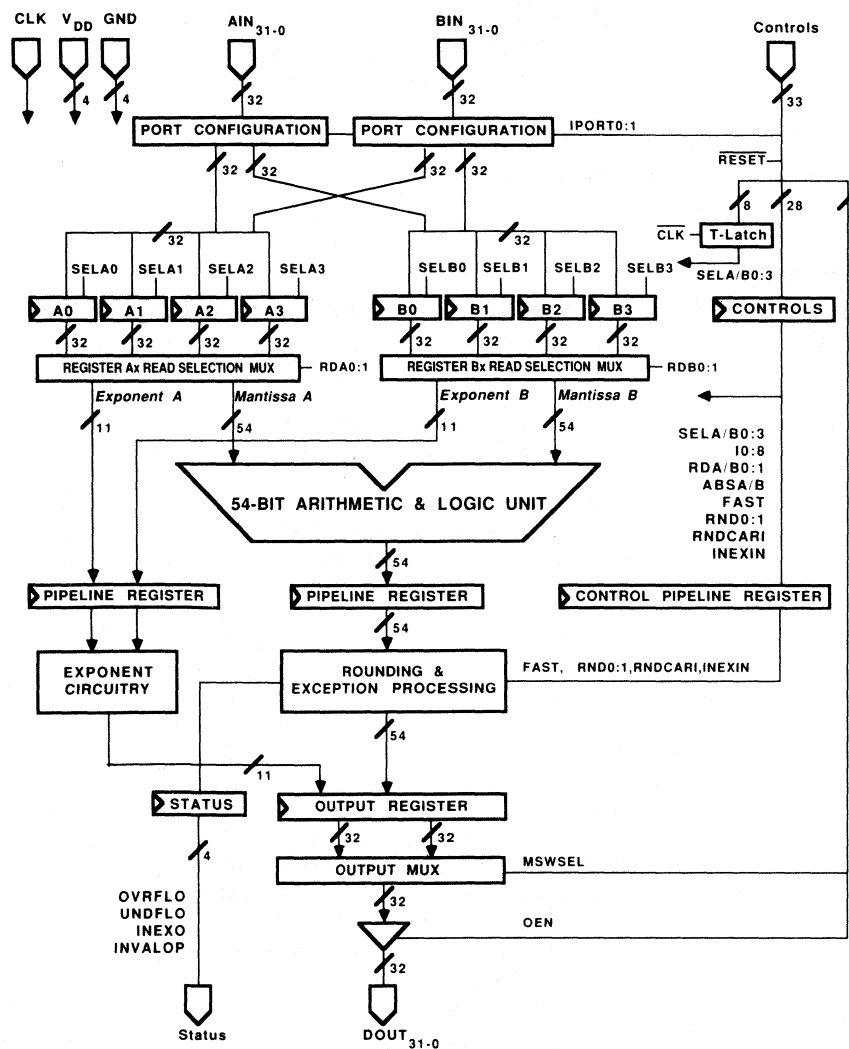
³Transitions measured per Figure 1.

⁴3ns minimum.

⁵Total latency = (data setup + processing + output delay of MSW) in Direct Operand Feed Mode.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

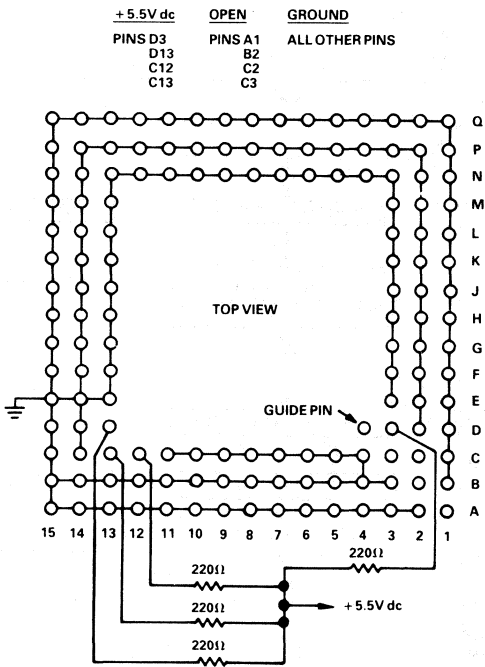
PIN	FUNCTION	PIN	FUNCTION
B2	DIN3	M12	DOUT28
B1	DIN2	M13	DOUT29
C2	DIN1	L12	DOUT30
C1	DIN0	L13	DOUT31
D2	WRAPB	K12	GND
D1	RDB0	K13	GND
E2	SELB0	J12	GND
E1	SELB1	J13	DENORM
F3	ABSB	H11	INVALOP
F2	DP	H12	OVRFLO
F1	SP	H13	UNDFLO
G2	CLK	G12	OEN
G3	RESET	G11	MSWSEL
G1	RND1	G13	SHLP
H1	RND0	F13	FAST
H2	RNDCARO	F12	ABSA
H3	VDD	F11	SELA1
J1	VDD	E13	SELA0
J2	VDD	E12	RDA0
K1	INEXO	D13	WRAPA
K2	DOUT0	D12	DIN31
L1	DOUT1	C13	DIN30
M1	DOUT2	B13	DIN29
L2	DOUT3	C12	DIN28
N1	N/C	A13	N/C
M2	DOUT4	B12	DIN27
N2	DOUT5	A12	DIN26
M3	DOUT6	B11	DIN25
N3	DOUT7	A11	DIN24
M4	DOUT8	B10	DIN23
N4	DOUT9	A10	DIN22
M5	DOUT10	B9	DIN21
N5	DOUT11	A9	DIN20
L6	DOUT12	C8	DIN19
M6	DOUT13	B8	DIN18
N6	DOUT14	A8	DIN17
M7	DOUT15	B7	DIN16
L7	DOUT16	C7	DIN15
N7	DOUT17	A7	DIN14
N8	DOUT18	A6	DIN13
M8	DOUT19	B6	DIN12
L8	DOUT20	C6	DIN11
N9	DOUT21	A5	DIN10
M9	DOUT22	B5	DIN9
N10	DOUT23	A4	DIN8
M10	DOUT24	B4	DIN7
N11	DOUT25	A3	DIN6
N12	DOUT26	A2	DIN5
M11	DOUT27	B3	DIN4
N13	N/C	A1	N/C

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



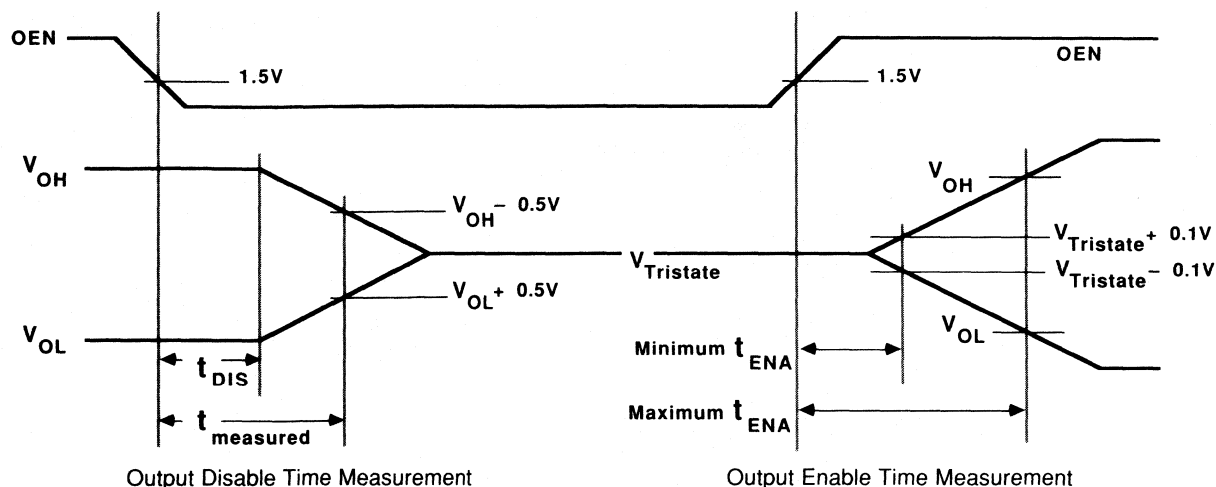


Figure 1. ADSP-3220 Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA} , is the earliest that outputs begin to drive. It is measured from the control signal OEN reaching 1.5 V to the point at which the fastest outputs have changed by 0.1 V from $V_{TRISTATE}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as “data valid.” Maximum enable times are longest at the highest specified temperature.

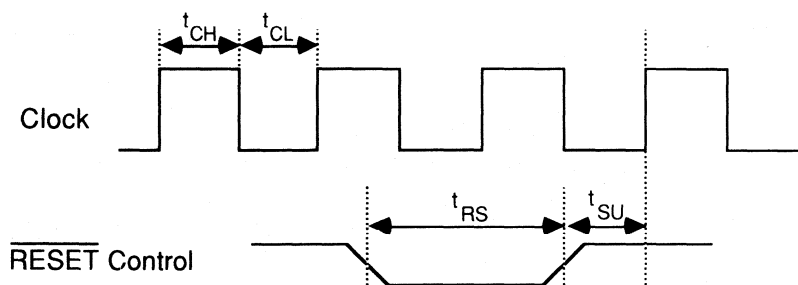
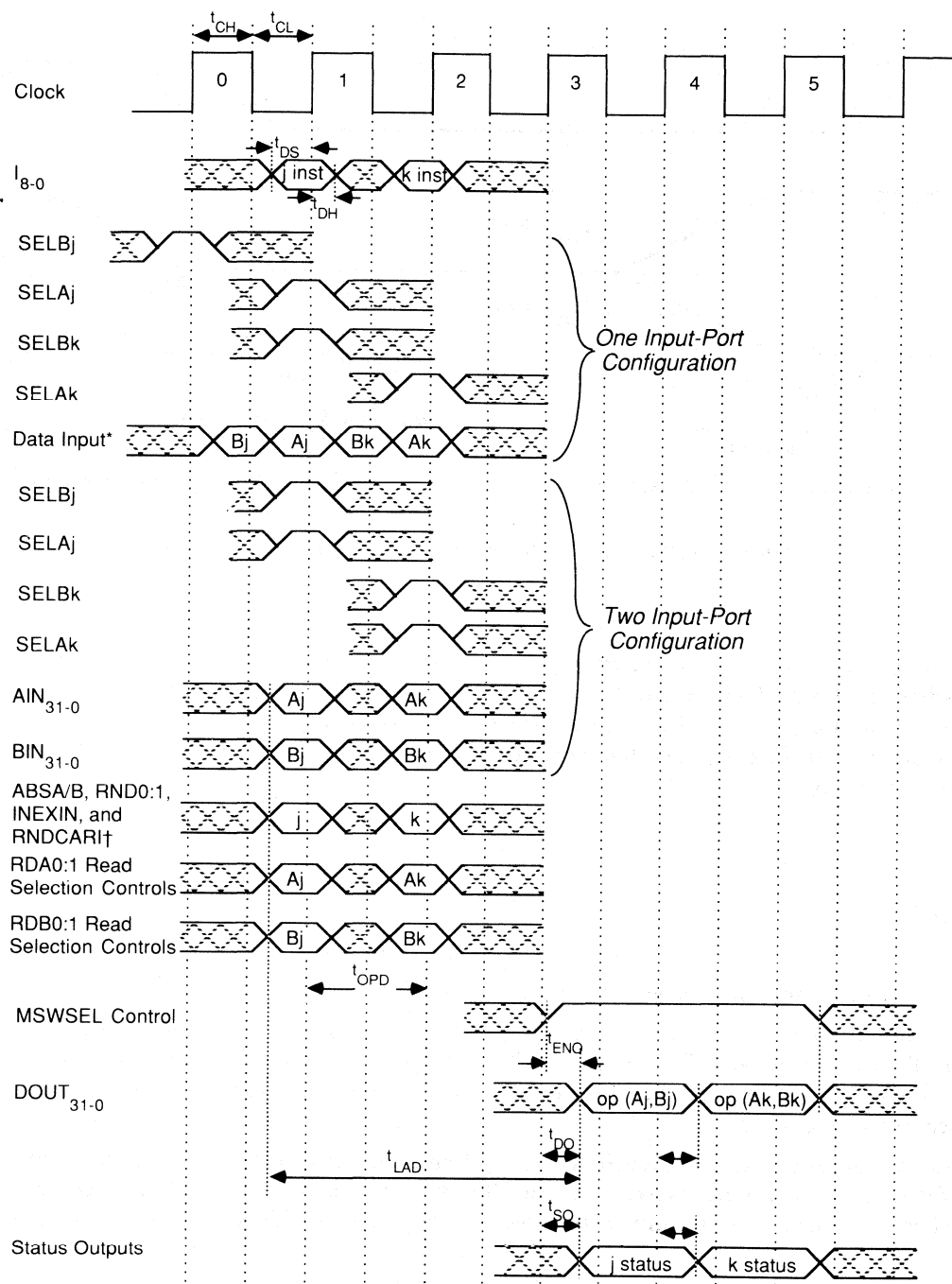
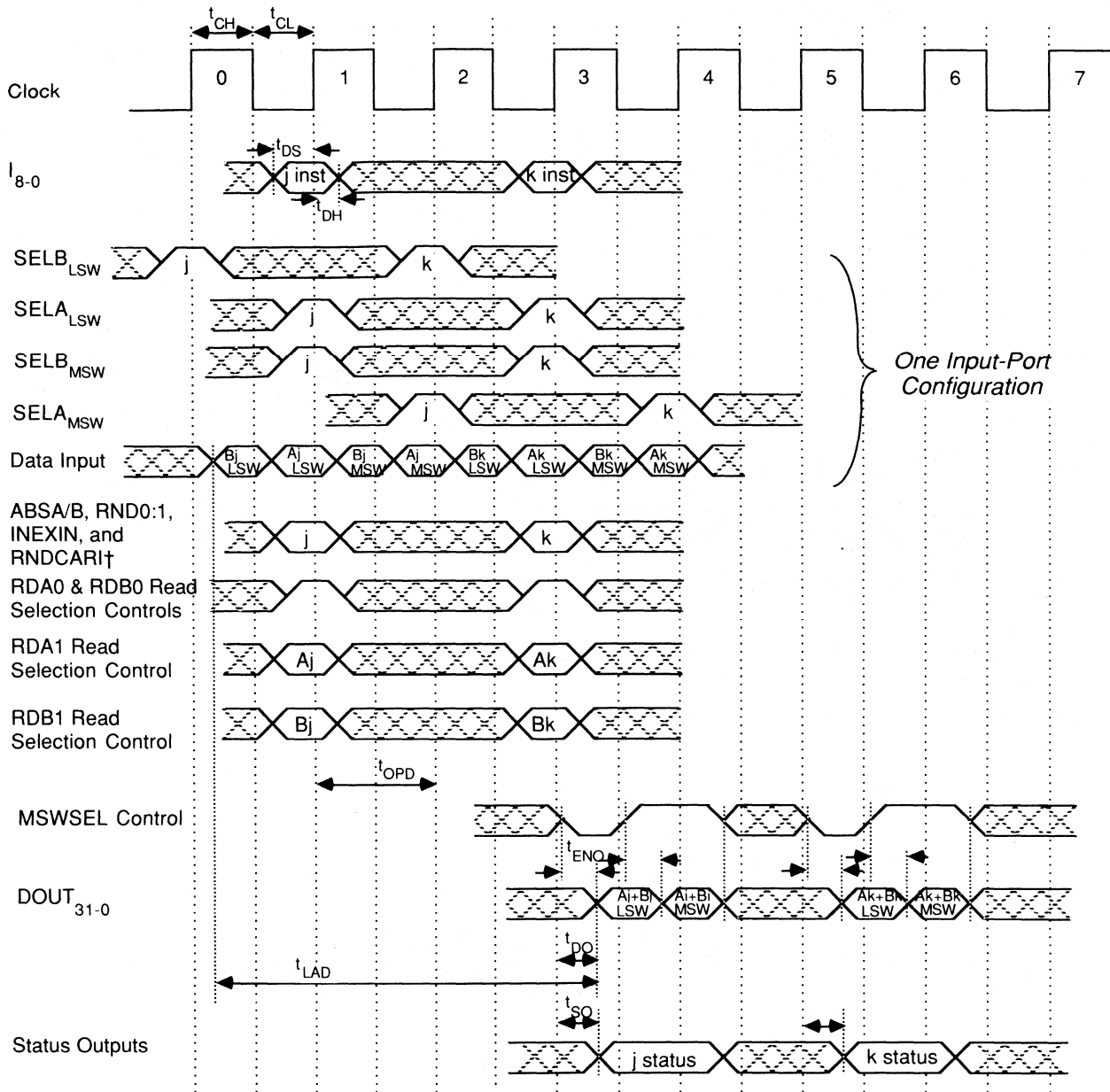


Figure 2. ADSP-3220 Reset Timing



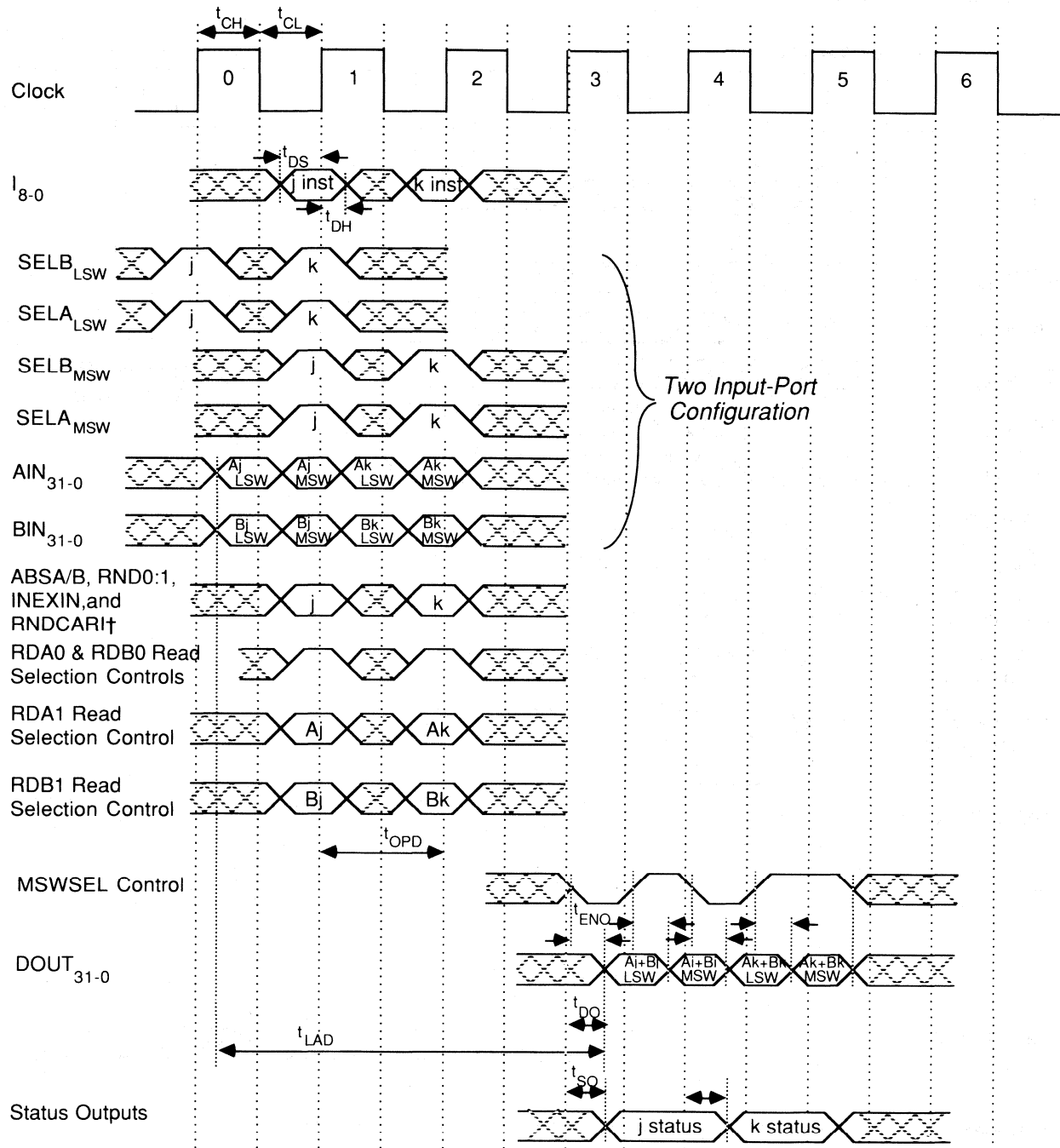
† RNDCARIT and INEXIN should be LO except for unwrap, division, and square root operations.

Figure 3. ADSP-3220 32-Bit Single-Precision Floating-Point Logical, and Fixed-Point ALU Operations



† RNDCAI and INEXIN should be LO except for unwrap, division, and square root operations.

Figure 4. ADSP-3220 64-Bit Double-Precision Floating-Point ALU Operations – One-Port Configuration



† RNDCARI and INEXIN should be LO except for unwrap, division, and square root operations.

Figure 5. ADSP-3220 64-Bit Double-Precision Floating-Point ALU Operations – Two-Port Configuration

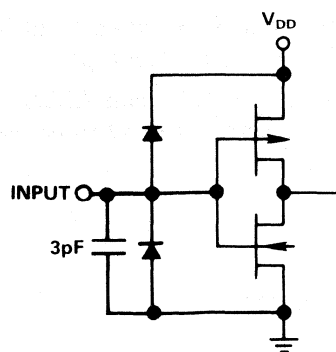


Figure 6. Equivalent Input Circuits

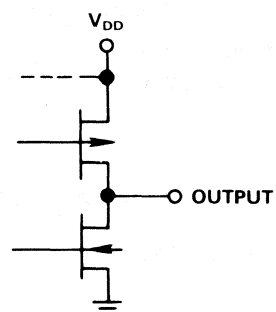


Figure 7. Equivalent Output Circuits

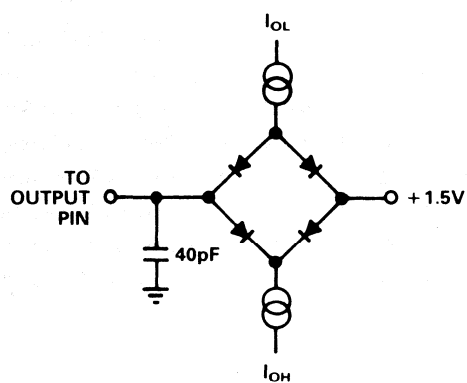


Figure 8. Normal Load for AC Measurements

ADSP-3220

5.0 ADSP-3220 Floating Point ALU Instructions

For all operations involving two operands, the operands may be in SP Floating point format. DP Floating point, or 32-bit FIXED point, but both operands must be of the same data type.

Note that for all arithmetic operations (SP, DP, and FIXED), the ABSA and ABSB controls can be used with the input operands, causing the absolute value of the respective operand to be used in the operation.

ADSP-3220 Fixed Point Arithmetic Operations

INSTRUCTION	OPCODE										COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
IADD	0	0	1	0	0	0	0	1	1	Integer Add (A + B)	
ISUBA	0	0	1	0	0	0	1	1	1	Integer Subtract (B – A)	
ISUBB	0	0	1	0	0	1	0	1	1	Integer Subtract (A – B)	
IADDWC	0	0	1	0	1	0	0	1	1	Integer Add With Carry (A + B) ¹	
ISUBWBA	0	0	1	0	1	0	1	1	1	Integer Subtract With Borrow (B – A) ¹	
ISUBWBB	0	0	1	0	1	1	0	1	1	Integer Subtract With Borrow (A – B) ¹	
INEGA	0	0	1	0	0	0	1	0	1	Perform Twos Complement Negation of the A Operand	
INEGB	0	0	1	0	0	1	0	1	0	Perform Twos Complement Negation of the B Operand	
IADDAS	0	0	1	1	0	0	0	1	1	Absolute Value of (A + B)	
ISUBAAS	0	0	1	1	0	0	1	1	1	Absolute Value of (B – A)	
ISUBBAS	0	0	1	1	0	1	0	1	1	Absolute Value of (A – B)	

ADSP-3220 Logical Operations

INSTRUCTION	OPCODE										COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
COMPLA	0	0	0	0	0	0	1	0	1	Ones Complement the A Operand	
COMPLB	0	0	0	0	0	1	0	1	0	Ones Complement the B Operand	
PASSA	0	0	0	0	0	0	0	0	1	Passes the A Operand (selected with RDA1, RDA0) unmodified to the output.	
PASSB	0	0	0	0	0	0	0	1	0	Passes the B Operand (selected with RDB1, RDB0) unmodified to the output.	
AANDB	0	0	0	0	1	0	0	1	0	Bitwise AND	
AORB	0	0	0	1	0	0	0	1	0	Bitwise OR	
AXORB	0	0	0	1	1	0	0	1	0	Bitwise Exclusive OR	
NOP	0	0	0	0	0	0	0	0	0	No Operation. Preserves status flags but does not preserve the contents of the output register.	
CLR	1	0	0	0	0	0	0	0	0	Clear. Sets the UNDFLO, OVERFLO, INVALID, and INEXO flags to zero The Output Register result is not meaningful.	

NOTE

¹The Carry bit in fixed point arithmetic is latched internally, for one-cycle only, to act as a Carry-In pin for the operations. Add with Carry or Subtract with Borrow. These instructions are used in performing 64-bit addition or subtraction. See note on Special Instructions in the commercial data sheet.

Table 2. ADSP-3220 Instruction Set

ADSP-3220 Single-Precision Floating Point Operations

INSTRUCTION	OPCODE									COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	
SADD	1	1	1	0	0	0	0	1	1	Floating Point SP Add (A + B)
SSUBB	1	1	1	0	0	0	1	1	1	Floating SP Subtract (A – B)
SSUBA	1	1	1	0	0	1	0	1	1	Floating SP Subtract (B – A)
SCOMP	1	1	1	0	0	1	1	1	1	SP Compare. Operation is (A – B); Output Result is (A – B); Flags OVRFLO and UNDFLO generated conditional on Greater Than or Less Than conditions, respectively. If equal, output is zero and UNDFLO and OVRFLO are both LOW.
SADDAS	0	1	1	0	0	0	0	1	1	SP Absolute Value of (A + B)
SSUBBAS	0	1	1	0	0	0	1	1	1	SP Absolute Value of (A – B)
SSUBAAS	0	1	1	0	0	1	0	1	1	SP Absolute Value of (B – A)
FIX A	0	1	1	0	0	1	1	0	1	Convert 32-bit Single Precision Floating Point A operand → 32-bit Integer
FIX B	0	1	1	0	0	1	1	1	0	Convert 32-bit Single Precision Floating Point B operand → 32-bit Integer
FLOAT A	0	1	1	1	0	0	1	0	1	Convert 32-bit FIXED A operand → 32-bit Single Precision Floating Point
FLOAT B	0	1	1	1	0	0	1	1	0	Convert 32-bit FIXED B operand → 32-bit Single Precision Floating Point
DOUBLE A	0	1	1	1	0	1	1	0	1	Convert 32-bit Single Precision A operand → 64-bit Double Precision Floating ¹
DOUBLE B	0	1	1	1	0	1	1	1	0	Convert 32-bit Single Precision B operand → 64-bit Double Precision Floating ¹
SPASS A	0	1	1	1	1	0	0	0	1	Pass SP A operand. A NAN is passed unmodified but causes the INVALOP exception
SPASS B	0	1	1	1	1	0	0	1	0	Pass SP B operand. A NAN is passed unmodified but causes the INVALOP exception
SWRAPA	0	1	1	1	0	0	0	0	1	Converts SP denormalized A operand → Wrapped format ²
SWRAPB	0	1	1	1	0	0	0	1	0	Converts SP denormalized B operand → Wrapped format ²
SUNWRAPA	0	1	1	0	1	0	0	0	1	Converts Wrapped A operand → SP denormalized format ²
SUNWRAPB	0	1	1	0	1	0	0	1	0	Converts Wrapped B operand → SP denormalized format ²
SSIGN ³	0	1	1	1	1	1	1	0	1	Transfers sign of the B operand to the A operand. Result is Sign B, Expt A, Fraction A.
SXSUB ³	0	1	1	1	1	1	0	0	1	Exponent subtract. Subtracts the B exponent from the A exponent. Result is Sign A, (Expt A – Expt B), Fraction A. NANs and Infinities are operated on directly without flagging the INVALOP exception. If the Expt of the Result underflows to – 127 or less, then the Output Result returned is Zero. If the Expt of the Result overflows to + 128, then the Output Result returned is Infinity.
SITRN ³	0	1	1	0	1	0	1	0	1	Integer Shift and Truncation. The A mantissa with hidden bit restored (24 bits) is treated as a right-justified unsigned integer and shifted down logically by the unbiased B exponent. ⁴ The 32-bit right-justified result appears in the MSW and is a left-zero-filled unsigned-magnitude integer. The shift value given by the unbiased B exponent is interpreted as an unsigned number; negative unbiased exponents cause very large down shifts.

NOTES

¹Conversion from FIXED to Double format are always exact. The 32-bit FIXED source operand must be fed from one of the registers A0, A2, B0, or B2 only.

²For information on handling denormals, wrapped, and unwrapped numbers, see Application Note on “Handling IEEE Exceptions.”

³An unbiased exponent is the exponent after the proper exponent bias has been subtracted.

Table 2. ADSP-3220 Instruction Set (Continued)

REV. B

ADSP-3220

ADSP-3220 Double-Precision Floating Point Operations

INSTRUCTION	OPCODE										COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
DADD	1	1	0	0	0	0	0	1	1	DP Add (A + B)	
DSUBB	1	1	0	0	0	0	1	1	1	DP Subtract (A – B)	
DSUBA	1	1	0	0	0	1	0	1	1	DP Subtract (B – A)	
DCOMP	1	1	0	0	0	1	1	1	1	DP Compare. Operation is (A – B); Output Result is (A – B); Flags OVRFLO and UNDFLO generated conditional on Greater Than or Less Than conditions, respectively. If equal, output is zero and UNFLO and OVRFLO are both LOW.	
DADDAS	0	1	0	0	0	0	0	1	1	DP Absolute Value of (A + B)	
DSUBBAS	0	1	0	0	0	0	1	1	1	DP Absolute Value of (A – B)	
DSUBAAS	0	1	0	0	0	1	0	1	1	DP Absolute Value of (B – A)	
DFIX A	0	1	0	0	1	1	1	0	1	Convert 64-bit Double Precision A operand→32-bit Integer	
DFIX B	0	1	0	0	1	1	1	1	0	Convert 64-bit Double Precision B operand→32-bit Integer	
DFLOAT A ¹	0	1	0	1	0	0	1	0	1	Convert 32-bit FIXED A operand→64-bit Double Precision Floating Point	
DFLOAT B ¹	0	1	0	1	0	0	1	1	0	Convert 32-bit FIXED B operand→64-bit Double Precision Floating Point	
SINGLE A	1	1	0	0	1	1	1	0	1	Convert 64-bit Double Precision A operand→32-bit Single Precision	
SINGLE B	1	1	0	0	1	1	1	1	0	Convert 64-bit Double Precision B operand→32-bit Single Precision	
DPASS A	0	1	0	1	1	0	0	0	1	Pass DP A operand. A NAN is passed unmodified but causes the INVALOP exception.	
DPASS B	0	1	0	1	1	0	0	1	0	Pass DP B operand. A NAN is passed unmodified but causes the INVALOP exception.	
DWRAP A	0	1	0	1	0	0	0	0	1	Converts DP denormalized A operand→Wrapped format ²	
DWRAP B	0	1	0	1	0	0	0	1	0	Converts DP denormalized B operand→Wrapped format ²	
DUNWRAP A	0	1	0	0	1	0	0	0	1	Converts Wrapped A operand→DP denormalized format ²	
DUNWRAP B	0	1	0	0	1	0	0	1	0	Converts Wrapped B operand→DP denormalized format ²	
DSIGN	0	1	0	1	1	1	1	0	1	Transfers sign of the B operand to the A operand. Result is Sign B, Expt A, Fraction A.	
DXSUB	0	1	0	1	1	1	0	0	1	Exponent subtract. Subtracts the B exponent from the A exponent. Result is Sign A, (Expt A – Expt B), Fraction A. NANs and Infinities are operated on directly without flagging the INVALOP exception. If the Expt of the Result underflows to – 1023 or less, then the Output Result returned is Zero. If the Expt of the Result overflows to + 1024, then the Output Result returned is Infinity.	
DITRN	0	1	0	0	1	0	1	0	1	Integer Shift and Truncation. The A mantissa with hidden bit restored (53 bits) is treated as a right-justified unsigned integer and shifted down logically by the unbiased B exponent. ³ The 32-bit right-justified result appears in the MSW and is a left-zero-filled unsigned-magnitude integer. The shift value given by the unbiased B exponent is interpreted as an unsigned number; negative unbiased exponents cause very large down shifts.	

NOTES

¹Conversion from Single to Double format are always exact, so INEXO will always be LOW for these conversions.

²For information on handling denormals, wrapped, and unwrapped numbers, see Application Note on “Handling IEEE Exceptions.”

³See note on Special Instructions in the commercial data sheet.

⁴An unbiased exponent is the exponent after the proper exponent bias has been subtracted.

Table 2. ADSP-3220 Instruction Set (Continued)

REV. B

Notations Used in the Tables Below:

RN	= Round to the Nearest Number
RP	= Round toward Plus Infinity
RM	= Round toward Minus Infinity
RZ	= Round toward Zero
NORM	= Normalized number
DNRM	= Denormalized number. A Denormalized number is treated as zero internally.
WNRM	= Wrapped number. A wrapped number is a number with a normalized fraction and an exponent that has been decremented through zero to take on a twos complement negative value.
UNRM	= Unnormalized number. An Unnormal is an Underflowed and Wrapped Number. An UNRM can result from a multiplication of 1 or 2 Wrapped Numbers.
NORM.MAX	= Maximum Normalized Number Representable in the Destination Format
NORM.MIN	= Minimum Normalized Number Representable in the Destination Format
OVF	= Overflowed Number
UNDF	= Underflowed Number
INV	= Invalid Operand
INF	= Infinity
OK	= No Exception Status Generated

A operand \ B operand	ZERO		DNRM		NORM		INF		NAN	
	result	status	result	status	result	status	result	status	result	status
ZERO	ZERO ²		DNRM		NORM		INF		NAN	INVALOP
DNRM	DNRM		NORM DNRM ZERO		INF,NORM.MAX ¹ NORM DNRM	OVRFLO	INF		NAN	INVALOP
NORM	NORM		INF,NORM.MAX ¹ NORM DNRM	OVRFLO	INF,NORM.MAX ¹ NORM DNRM ZERO	OVRFLO	INF		NAN	INVALOP
INF	INF		INF		INF		INF ³ NAN ³	INVALOP	NAN	INVALOP
NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode.
2. $\pm \text{ZERO} \pm \text{ZERO} \Rightarrow \pm \text{ZERO}$
 $\pm \text{ZERO} \mp \text{ZERO} \Rightarrow +\text{ZERO}$ (RN, RZ, RP rounding modes)
 $\pm \text{ZERO} \mp \text{ZERO} \Rightarrow -\text{ZERO}$ (RM rounding mode)
3. $\pm \text{INF} \pm \text{INF} \Rightarrow \pm \text{INF}$
 $\pm \text{INF} \mp \text{INF} \Rightarrow +\text{NAN}$ (RN, RZ, RP rounding modes)
 $\pm \text{INF} \mp \text{INF} \Rightarrow -\text{NAN}$ (RM rounding mode)

Table 3. ADSP-3220 Floating-Point Addition/Subtraction (IEEE Mode)

ADSP-3220

		B operand													
A operand		ZERO		DNRM		NORM		INF		NAN					
		result	status	result	status	result	status	result	status	result	status				
ZERO		ZERO ²		ZERO		NORM		INF		NAN	INVALOP				
DNRM		ZERO		NORM ZERO		INF,NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	INF		NAN	INVALOP				
NORM		ZERO		INF,NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	INF,NORM.MAX ¹ NORM ZERO ZERO ⁴	OVRFLO UNDFLO	INF		NAN	INVALOP				
INF		INF		INF		INF		INF ³ NAN ³	INVALOP	NAN	INVALOP				
NAN		NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP				

1. Either INF or NORM.MAX, depending on rounding mode.
2. $\pm \text{ZERO} \pm \text{ZERO} \Rightarrow \pm \text{ZERO}$
 $\pm \text{ZERO} \mp \text{ZERO} \Rightarrow + \text{ZERO}$ (RN, RZ, RP rounding modes)
 $\pm \text{ZERO} \mp \text{ZERO} \Rightarrow - \text{ZERO}$ (RM rounding mode)
3. $\pm \text{INF} \pm \text{INF} \Rightarrow \pm \text{INF}$
 $\pm \text{INF} \mp \text{INF} \Rightarrow + \text{NAN}$ (RN, RZ, RP rounding modes)
 $\pm \text{INF} \mp \text{INF} \Rightarrow - \text{NAN}$ (RM rounding mode)
4. Exact result.

Table 4. ADSP-3220 Floating-Point Addition/Subtraction (FAST Mode)

Sign	HB	f22...f1	f0	Unbiased Expnt	Source Name	Sign	i30	i29	i28	i27	i26	i25	i24	i23	i22...i7	i6	i5	i4	i3	i2	i1	i0	Rounding Modes	Status Flags
0	1	X...X	X	2**	128	0	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	all	INVALOP
0	1	0...0	0	2**	128	0	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	all	INVALOP
0	1	0...0	0	2**	31	U*	U	U	U	U	U	U	U	U	U...U	U	U	U	U	U	U	U	all	OVRFLO
0	1	1...1	1	2**	30	0	1	1	1	1	1	1	1	1	1...1	1	0	0	0	0	0	0	all	
0	1	1...1	1	2**	23	0	0	0	0	0	0	0	0	1	1...1	1	1	1	1	1	1	1	all	
0	1	0...0	0	2**	23	0	0	0	0	0	0	0	0	1	0...0	0	0	0	0	0	0	0	all	
0	1	1...1	1	2**	22	0	0	0	0	0	0	0	0	1	0...0	0	0	0	0	0	0	0	RN,RP	INEXO
0	1	1...1	1	2**	22	0	0	0	0	0	0	0	0	1	1...1	1	1	1	1	1	1	1	RZ,RM	INEXO
0	1	0...0	0	2**	0	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	all	
0	1	1...1	1	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RN,RP	UNDFLO,INEXO
0	1	1...1	1	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RZ,RM	UNDFLO,INEXO
0	1	0...0	0	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RN,RP	UNDFLO,INEXO
0	1	0...0	0	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RZ,RM	UNDFLO,INEXO
0	1	0...0	0	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP	UNDFLO,INEXO
0	1	0...0	0	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RM,RN,RZ	UNDFLO,INEXO
0	1	0...0	0	2**	-126	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP	UNDFLO,INEXO
0	1	0...0	0	2**	-126	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RM,RN,RZ	UNDFLO,INEXO
0	0	0...0	0	2**	-126	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP	UNDFLO,INEXO
0	0	0...0	0	2**	-126	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RM,RN,RZ	UNDFLO,INEXO
0	0	0...0	0	2**	0	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	all	
1	0	0...0	0	2**	-126	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	0	0...0	0	2**	-126	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0...0	0	2**	-126	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	1	0...0	0	2**	-126	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0...0	0	2**	-1	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	1	0...0	0	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0...0	0	2**	-1	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	1	1...1	1	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP,RZ	UNDFLO,INEXO
1	1	1...1	1	2**	-1	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	RM,RN	UNDFLO,INEXO
1	1	1...1	1	2**	-1	0	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	RP,RZ	UNDFLO,INEXO
1	1	0...0	0	2**	0	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	all	
1	1	1...1	1	2**	22	1	1	1	1	1	1	1	1	1	1...1	0	0	0	0	0	0	0	RM,RN	INEXO
1	1	1...1	1	2**	22	1	1	1	1	1	1	1	1	1	1...1	0	0	0	0	0	0	0	RP,RZ	INEXO
1	1	0...0	0	2**	23	1	1	1	1	1	1	1	1	1	1...1	0	0	0	0	0	0	0	all	
1	1	1...1	1	2**	23	1	1	1	1	1	1	1	1	1	1...1	0	0	0	0	0	0	0	all	
1	1	1...1	1	2**	30	1	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	all	
1	1	0...0	0	2**	31	1	0	0	0	0	0	0	0	0	0...0	0	0	0	0	0	0	0	all	
1	1	0...0	0	2**	31	U	U	U	U	U	U	U	U	U	U...U	U	U	U	U	U	U	U	all	
1	1	0...0	0	2**	128	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	all	INVALOP
1	1	X...X	X	2**	128	1	1	1	1	1	1	1	1	1	1...1	1	1	1	1	1	1	1	all	INVALOP

**"U" denotes an undefined result.

Table 5. Conversion of 32-Bit Floating-Point to 32-Bit Twos-Complement Integer

Sign	HB	f51 . . . f22	f21	f20	f19 . . . f1	f0		Unbiased Expnt	Source Name	Sign	i30 . . . i1	i0	Rounding Modes	Status Flags
0	1	X . . . X	X	X	X . . . X	X	2**	1024	+ NAN	0	1 . . . 1	1	all	INVALOP
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	1024	+ INF	0	1 . . . 1	1	all	INVALOP
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	31		U*	U . . . U	U	all	OVRFLO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	30		U	U . . . U	U	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	30		0	1 . . . 1	1	RZ,RM	INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	30		U	U . . . U	U	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	30		0	1 . . . 1	1	RZ,RM	INEXO
0	1	1 . . . 1	0	1	1 . . . 1	1	2**	30		U	U . . . U	U	RP	OVRFLO,INEXO
0	1	1 . . . 1	0	1	1 . . . 1	1	2**	30		0	1 . . . 1	1	RM,RN,RZ	INEXO
0	1	1 . . . 1	0	0	0 . . . 0	1	2**	30		U	U . . . U	U	RP	OVRFLO,INEXO
0	1	1 . . . 1	0	0	0 . . . 0	1	2**	30		0	1 . . . 1	1	RM,RN,RZ	INEXO
0	1	1 . . . 1	0	0	0 . . . 0	0	2**	30		0	1 . . . 1	1	all	
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	0	one	0	0 . . . 0	1	all	
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	one - 1LSB	0	0 . . . 0	1	RN,RP	UNDFLO,INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	one - 1LSB	0	0 . . . 0	0	RZ,RM	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	1/2 + 1LSB	0	0 . . . 0	1	RN,RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	1/2 + 1LSB	0	0 . . . 0	0	RZ,RM	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	1/2	0	0 . . . 0	1	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	1/2	0	0 . . . 0	0	RM,RN,RZ	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	+ NORM.MIN	0	0 . . . 0	1	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	+ NORM.MIN	0	0 . . . 0	0	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	+ DENORM.MIN	0	0 . . . 0	1	RP	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	+ DENORM.MIN	0	0 . . . 0	0	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	0	0	0	+ ZERO	0	0 . . . 0	0	all	
1	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	- DENORM.MIN	1	1 . . . 1	1	RM	UNDFLO,INEXO
1	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	- DENORM.MIN	0	0 . . . 0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	- NORM.MIN	1	1 . . . 1	1	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	- NORM.MIN	0	0 . . . 0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	-1/2	1	1 . . . 1	1	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	-1/2	0	0 . . . 0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	-1/2 - 1LSB	1	1 . . . 1	1	RM,RN	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	-1/2 - 1LSB	0	0 . . . 0	0	RP,RZ	UNDFLO,INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	- one + 1LSB	1	1 . . . 1	1	RM,RN	UNDFLO,INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	- one + 1LSB	0	0 . . . 0	0	RP,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	0	- one	1	1 . . . 1	1	all	
1	1	1 . . . 1	0	0	0 . . . 0	0	2**	30		1	0 . . . 0	1	all	
1	1	1 . . . 1	0	0	0 . . . 0	1	2**	30		1	0 . . . 0	0	RM	INEXO
1	1	1 . . . 1	0	0	0 . . . 0	1	2**	30		1	0 . . . 0	1	RP,RN,RZ	INEXO
1	1	1 . . . 1	0	1	1 . . . 1	1	2**	30		1	0 . . . 0	0	RM	INEXO
1	1	1 . . . 1	0	1	1 . . . 1	1	2**	30		1	0 . . . 0	1	RP,RN,RZ	INEXO
1	1	1 . . . 1	1	0	0 . . . 0	0	2**	30		1	0 . . . 0	0	RM,RN	INEXO
1	1	1 . . . 1	1	0	0 . . . 0	0	2**	30		1	0 . . . 0	1	RP,RZ	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	30		1	0 . . . 0	0	RM,RN	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	30		1	0 . . . 0	1	RP,RZ	INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	31		1	0 . . . 0	0	all	
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	31		1	0 . . . 0	0	RP,RN,RZ	INEXO
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	31		U	U . . . U	U	RM	OVRFLO,INEXO
1	1	0 . . . 0	0	1	0 . . . 0	0	2**	31		1	0 . . . 0	0	RP,RZ	INEXO
1	1	0 . . . 0	0	1	0 . . . 0	0	2**	31		U	U . . . U	U	RM,RN	OVRFLO,INEXO
1	1	0 . . . 0	0	1	1 . . . 1	1	2**	31		1	0 . . . 0	0	RP,RZ	INEXO
1	1	0 . . . 0	0	1	1 . . . 1	1	2**	31		U	U . . . U	U	RM,RN	OVRFLO,INEXO
1	1	0 . . . 0	1	0	0 . . . 0	0	2**	31		U	U . . . U	U	all	OVRFLO
1	1	0 . . . 0	1	0	0 . . . 0	1	2**	31		U	U . . . U	U	all	OVRFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	32		U	U . . . U	U	all	OVRFLO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	1024	- INF	1	1 . . . 1	1	all	INVALOP
1	1	X . . . X	X	X	X . . . X	X	2**	1024	- NAN	1	1 . . . 1	1	all	INVALOP

U denotes an undefined result.

NOTE: Heavy line indicates rounding boundary in source.

Table 6. Conversion of 64-Bit Double-Precision Floating-Point to 32-Bit Twos-Complement Integer

Sign	HB	f51 . . . f30	f29	f28	f27 . . . f1	f0		Unbiased Expnt	Source Name	Sign	HB	f22 . . . f1	f0		Unbiased Expnt	Result Name	Rounding Modes	Status Flags
0	1	X . . . X	X	X	X . . . X	X	2**	1024	+NAN	0	1	1 . . . 1	1	2**	128	+NAN	all	INVALOP
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	1024	+INF	0	1	0 . . . 0	0	2**	128	+INF	all	
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	1023	+NORM.MAX	0	1	0 . . . 0	0	2**	128	+INF	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	1023	+NORM.MAX	0	1	1 . . . 1	1	2**	127	+NORM.MAX	RZ,RM	OVRFLO,INEXO
0	1	1 . . . 1	1	1	0 . . . 0	0	2**	127		1	1	1 . . . 0	0	2**	127	+INF	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	1	0 . . . 0	0	2**	127		0	1	1 . . . 1	1	2**	127	+NORM.MAX	RZ,RM	INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	127		0	1	1 . . . 1	1	2**	127	+INF	RP	OVRFLO,INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	127		0	1	1 . . . 1	1	2**	127	+NORM.MAX	RM,RN,RZ	INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	127		0	1	1 . . . 1	1	2**	127	+NORM.MAX	all	
0	1	1 . . . 1	0	0	0 . . . 0	0	2**	127		0	1	1 . . . 1	1	2**	127	+NORM.MAX	RP	INEXO
0	1	1 . . . 1	0	0	0 . . . 0	0	2**	127		0	1	1 . . . 1	0	2**	127		RM,RN,RZ	INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-126		0	1	0 . . . 0	0	2**	-126	+NORM.MIN	all	
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	-127		0	0	1 . . . 1	1	2**	-126	+NORM.MIN	RP,RN	INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	--127		0	0	1 . . . 1	1	2**	-126	+DNRM.MAX	RZ,RM	UNDFLO,INEXO
0	1	1 . . . 1	0	0	0 . . . 0	0	2**	-127		0	0	1 . . . 1	1	2**	-126	+DNRM.MAX	all	
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-149		0	0	0 . . . 0	0	2**	-126	+DNRM.MIN	all	
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	+NORM.MIN	0	0	0 . . . 0	0	2**	-126	+DNRM.MIN	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	+NORM.MIN	0	0	0 . . . 0	0	2**	-126	+ZERO	RM,RN,RZ	UNDFLO,INEXO
0	0	1 . . . 1	1	1	1 . . . 1	1	2**	-1022	+DNRM.MAX	0	0	0 . . . 0	1	2**	-126	+DNRM.MIN	RP	UNDFLO,INEXO
0	0	1 . . . 1	1	1	1 . . . 1	1	2**	-1022	+DNRM.MAX	0	0	0 . . . 0	0	2**	-126	+ZERO	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	+DNRM.MIN	0	0	0 . . . 0	1	2**	-126	+DNRM.MIN	RP	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	+DNRM.MIN	0	0	0 . . . 0	0	2**	-126	+ZERO	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	0	0		+ZERO	0	0	0 . . . 0	0	0	0	+ZERO	all	
1	0	0 . . . 0	0	0	0 . . . 0	0	0		-ZERO	1	0	0 . . . 0	0	0	0	-ZERO	all	
1	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	-DNRM.MIN	1	0	0 . . . 0	1	2**	-126	-DNRM.MIN	RM	UNDFLO,INEXO
1	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	-DNRM.MIN	1	0	0 . . . 0	0	2**	-126	-ZERO	RP,RN,RZ	UNDFLO,INEXO
1	0	1 . . . 1	1	1	1 . . . 1	1	2**	-1022	-DNRM.MAX	1	0	0 . . . 0	1	2**	-126	-DNRM.MIN	RM	UNDFLO,INEXO
1	0	1 . . . 1	1	1	1 . . . 1	1	2**	-1022	-DNRM.MAX	1	0	0 . . . 0	0	2**	-126	-ZERO	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	-NORM.MIN	1	0	0 . . . 0	1	2**	-126	-DNRM.MIN	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	-NORM.MIN	1	0	0 . . . 0	0	2**	-126	-ZERO	RP,RN,RZ	UNDFLO,INEXO
1	1	1 . . . 1	0	0	0 . . . 0	0	2**	-149		1	0	0 . . . 0	1	2**	-126	-DNRM.MIN	all	
1	1	1 . . . 1	0	0	0 . . . 0	0	2**	-127		1	0	1 . . . 1	1	2**	-126	-DNRM.MAX	all	
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	-127		1	0	1 . . . 1	1	2**	-126	-NORM.MIN	RM,RN	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	-127		1	0	1 . . . 1	1	2**	-126	-DNRM.MAX	RP,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-126		1	1	0 . . . 0	0	2**	-126	-NORM.MIN	all	
1	1	1 . . . 1	0	0	0 . . . 0	1	2**	127		1	1	1 . . . 1	1	2**	127	-NORM.MAX	RM	INEXO
1	1	1 . . . 1	0	0	0 . . . 0	1	2**	127		1	1	1 . . . 1	0	2**	127		RP,RN,RZ	INEXO
1	1	1 . . . 1	1	0	0 . . . 0	0	2**	127		1	1	1 . . . 1	1	2**	127	-NORM.MAX	all	
1	1	1 . . . 1	1	0	0 . . . 0	1	2**	127		1	1	1 . . . 1	1	2**	127	-INF	RM	OVRFLO,INEXO
1	1	1 . . . 1	1	0	0 . . . 0	1	2**	127		1	1	1 . . . 1	1	2**	127	-NORM.MAX	RP,RN,RZ	INEXO
1	1	1 . . . 1	1	1	0 . . . 0	0	2**	127		1	1	1 . . . 1	1	2**	127	-INF	RM,RN	OVRFLO,INEXO
1	1	1 . . . 1	1	1	0 . . . 0	0	2**	127		1	1	1 . . . 1	1	2**	127	-NORM.MAX	RP,RZ	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	1023	-NORM.MAX	1	1	0 . . . 0	0	2**	128	-INF	RM,RN	OVRFLO,INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	1023	-NORM.MAX	1	1	1 . . . 1	1	2**	127	-NORM.MAX	RP,RZ	OVRFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	1024	-INF	1	1	0 . . . 0	0	2**	128	-INF	all	
1	1	X . . . X	X	X	X . . . X	X	2**	1024	-NAN	1	1	1 . . . 1	1	2**	128	-NAN	all	INVALOP

NOTE: Heavy line indicates rounding boundary in source.

Table 7. Conversion of 64-Bit Double-Precision Floating-Point to 32-Bit Single-Precision Floating-Point (IEEE Mode)

1.1 Scope.

This specification covers the detail requirements for a CMOS monolithic 32-bit and 64-bit IEEE Standard 754 format floating-point arithmetic and logic unit (ALU).

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	ADSP-3221SG/883B
-2	ADSP-3221TG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-144A.

1.3 Absolute Maximum Ratings.

Supply Voltage	 -0.3 V to 7 V
Input Voltage	 -0.3 V to V_{DD}
Output Voltage	 -0.3 V to V_{DD}
Operating Temperature Range (Ambient)	 -55°C to +125°C
Storage Temperature Range	 -65°C to +150°C
Lead Temperature (Soldering 10 sec)	 +300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-3221 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	-1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Digital Input High Voltage, CLK and Asynchronous Controls (RESET, MSWSEL, OEN & IPORT0:1)	V _{IHA}	-1, 2	3.0	3.0	3.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	-1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = -1 mA	V min
Digital Output Low Voltage	V _{OL}	-1, 2	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current	I _{IH}	-1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	-1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current	I _{OZH} I _{OZL}	-1, 2	50	50	50			V _{DD} = max High Z, V _{IN} = 0 V or max	μA max
Supply Current	I _{DD1}	-1, 2	150	200	200			@ max Clock Rate, TTL Inputs	mA max
	I _{DD2}		50	60	60			All V _{IN} = 2.4 V	mA max
Clock Cycle	t _{CY}	-1	125			150	150	Note 2	ns max
		-2	100			125	125		
Clock LO	t _{CL}	-1, 2	20			30	30	Note 2	ns min
Clock HI	t _{CH}	-1, 2	20			30	30	Note 2	ns min
Data & Control Setup	t _{DS}	-1	20			25	25	Note 2	ns min
		-2	15			20	20		
Data & Control Hold	t _{DH}	-1, 2	3			3	3	Note 2	ns min
Data Output Delay	t _{DO}	-1	30			35	35	Note 2	ns max
		-2	25			30	30		
Status Output Delay	t _{SO}	-1	30			35	35	Note 2	ns max
		-2	25			30	30		
MSWSEL-to-Data Delay	t _{ENO}	-1	25			30	30	Note 2	ns max
		-2	20			25	25		
Three-State Disable Delay	t _{DIS}	-1	18			25	25	Notes 2 & 3	ns max
		-2	15			20	20		
Three-State Enable Delay	t _{ENA}	-1	25			30	30	Notes 2, 3 & 4	ns max
		-2	20			25	25		
RESET Setup	t _{SU}	-1, 2	25			25	25	Note 2	ns min
RESET Pulse Duration	t _{RS}	-1, 2	75			75	75	Note 2	ns min
Operation Time (With or Without Direct Operand Feed): 32-Bit Multiplication	t _{OPD}	-1	125			150	150	Note 2	ns max
		-2	100			125	125		
64-Bit ALU Operation	t _{OPD}	-1	125			150	150	Note 2	ns max
		-2	100			125	125		

Table 1. (Continued on next page)

REV. A

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Hold Setup	t _{HS}	−1	20			22	22	Note 2	ns min
		−2	15			18	18		
Hold Hold	t _{HH}	−1, 2	3			3	3	Note 2	ns min
Total Latency ⁵ (With Direct Operand Feed):	t _{LAD}								
32-Bit ALU Operation		−1	300			360	360	Note 2	ns max
		−2	240			300	300		
64-Bit ALU Operation		−1	363			435	435	Note 2	ns max
		−2	290			363	363		
32-Bit Division		−1	2.175			2.61	2.61	Note 2	μs max
		−2	1.74			2.175	2.175		
64-Bit Division		−1	3.925			4.71	4.71	Note 2	μs max
		−2	3.14			3.925	3.925		
32-Bit Square Root		−1	3.8			4.56	4.56	Note 2	μs max
		−2	3.04			3.8	3.8		
64-Bit Square Root		−1	7.425			8.91	8.91	Note 2	μs max
		−2	5.94			7.425	7.425		

NOTES

¹T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).

²Input levels are GND and +3.0 V; V_{DD} = +4.5 V, and timing transitions, per Figure 1 through 8, measured at +1.5 V.

³Transitions measured per Figure 1.

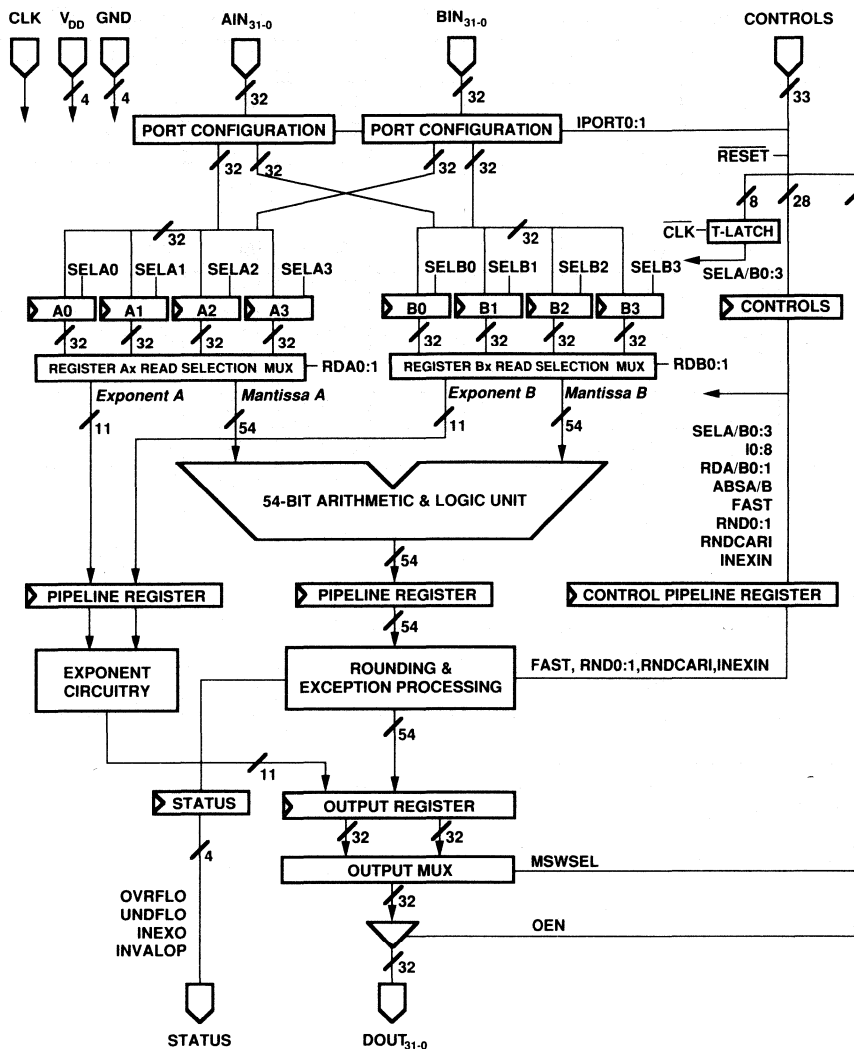
⁴3 ns minimum.

⁵Total latency = (data setup + processing + output delay of MSW) in Direct Operand Feed Mode.

Table 1.

ADSP-3221

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

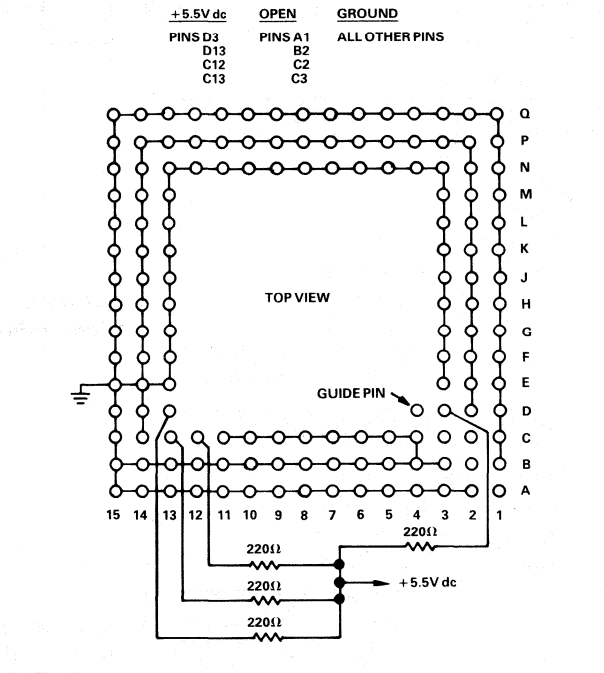
PIN	FUNCTION	PIN	FUNCTION
B2	DIN3	M12	DOUT28
B1	DIN2	M13	DOUT29
C2	DIN1	L12	DOUT30
C1	DIN0	L13	DOUT31
D2	WRAPB	K12	GND
D1	RDB0	K13	GND
E2	SELB0	J12	GND
E1	SELB1	J13	DENORM
F3	ABSB	H11	INVALOP
F2	DP	H12	OVRFLO
F1	SP	H13	UNDFLO
G2	CLK	G12	OEN
G3	RESET	G11	MSWSEL
G1	RND1	G13	SHLP
H1	RND0	F13	FAST
H2	RNDCARO	F12	ABSA
H3	V _{DD}	F11	SELA1
J1	V _{DD}	E13	SELA0
J2	V _{DD}	E12	RDA0
K1	INEXO	D13	WRAPA
K2	DOUT0	D12	DIN31
L1	DOUT1	C13	DIN30
M1	DOUT2	B13	DIN29
L2	DOUT3	C12	DIN28
N1	N/C	A13	N/C
M2	DOUT4	B12	DIN27
N2	DOUT5	A12	DIN26
M3	DOUT6	B11	DIN25
N3	DOUT7	A11	DIN24
M4	DOUT8	B10	DIN23
N4	DOUT9	A10	DIN22
M5	DOUT10	B8	DIN21
N5	DOUT11	A9	DIN20
L6	DOUT12	C8	DIN19
M6	DOUT13	B8	DIN18
N6	DOUT14	A8	DIN17
M7	DOUT15	B7	DIN16
L7	DOUT16	C7	DIN15
N7	DOUT17	A7	DIN14
N8	DOUT18	A6	DIN13
M8	DOUT19	B6	DIN12
L8	DOUT20	C6	DIN11
N9	DOUT21	A5	DIN10
M9	DOUT22	B5	DIN9
N10	DOUT23	A4	DIN8
M10	DOUT24	B4	DIN7
N11	DOUT25	A3	DIN6
N12	DOUT26	A2	DIN5
M11	DOUT27	B3	DIN4
N13	N/C	A1	N/C

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 V}{i_L}$$

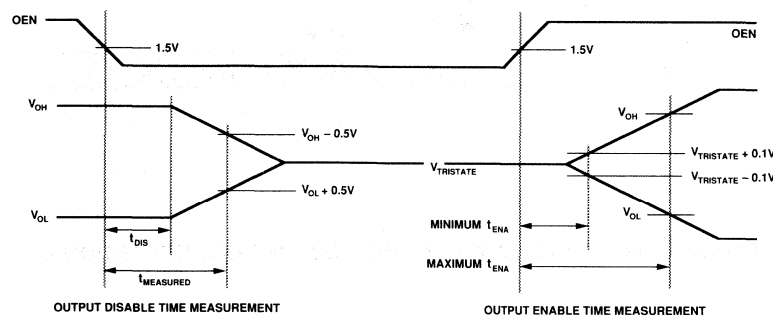
from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA} , is the earliest that outputs begin to drive. It is measured from the control signal OEN reaching 1.5 V to the point at which the fastest outputs have changed by 0.1 V from $V_{TRISTATE}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.



REFER TO THE DISCUSSION IN THE SECTION "TIMING" IN THE TEXT OF THE DATA SHEET FOR A DESCRIPTION OF THIS FIGURE.

Figure 1. Three-State Disable and Enable Timing

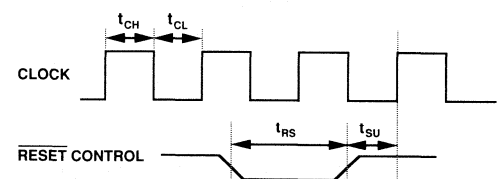
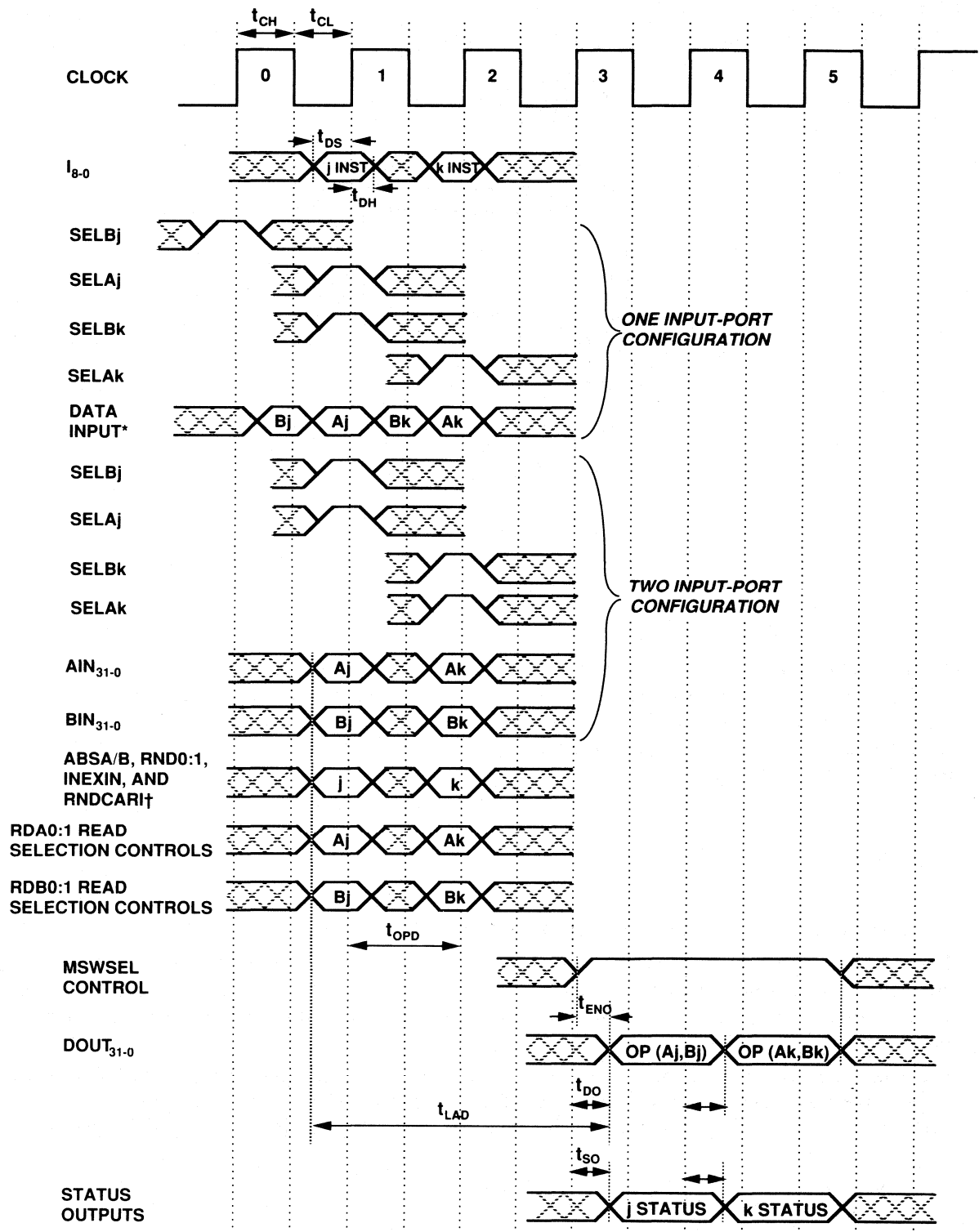
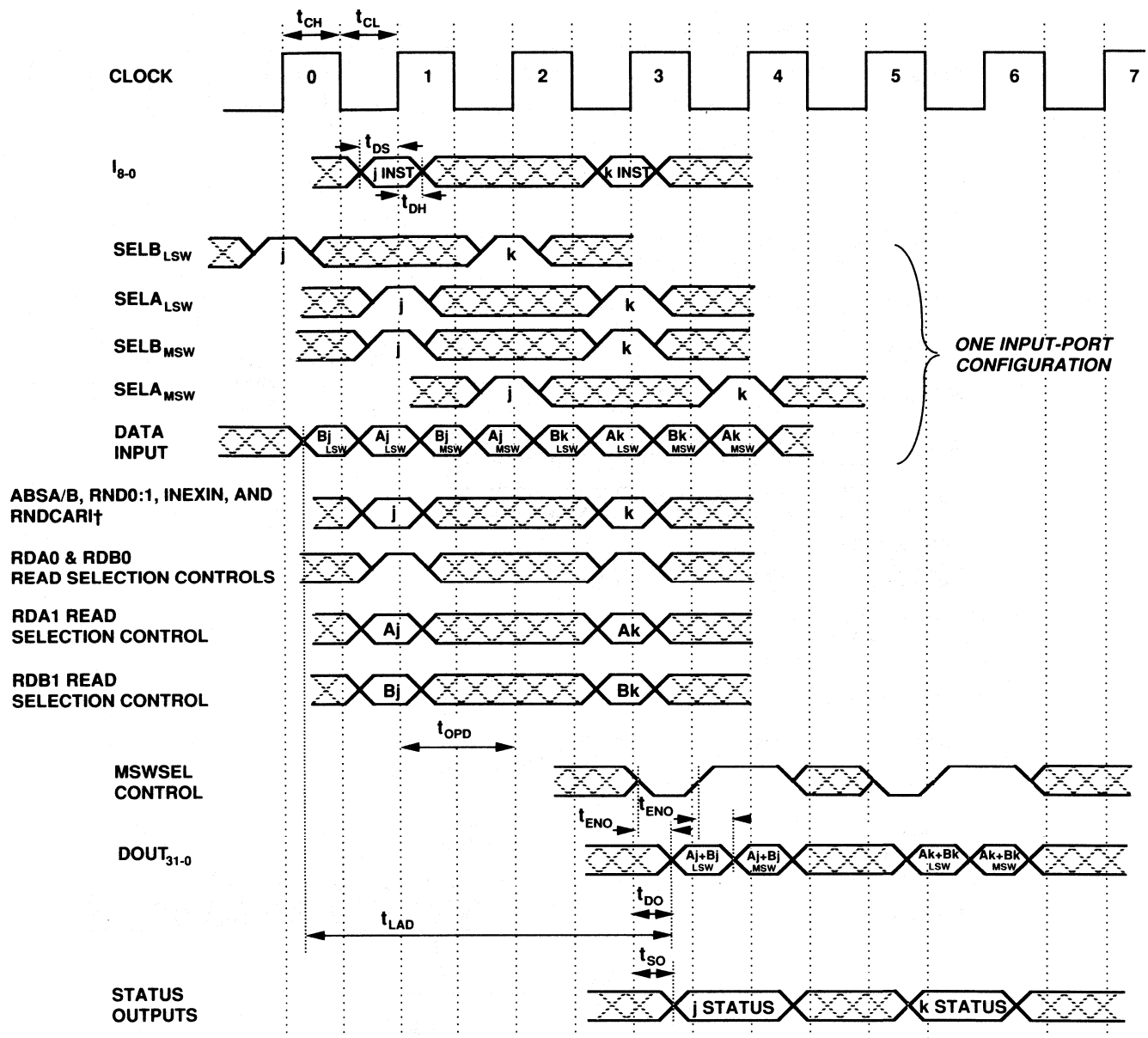


Figure 2. Reset Timing



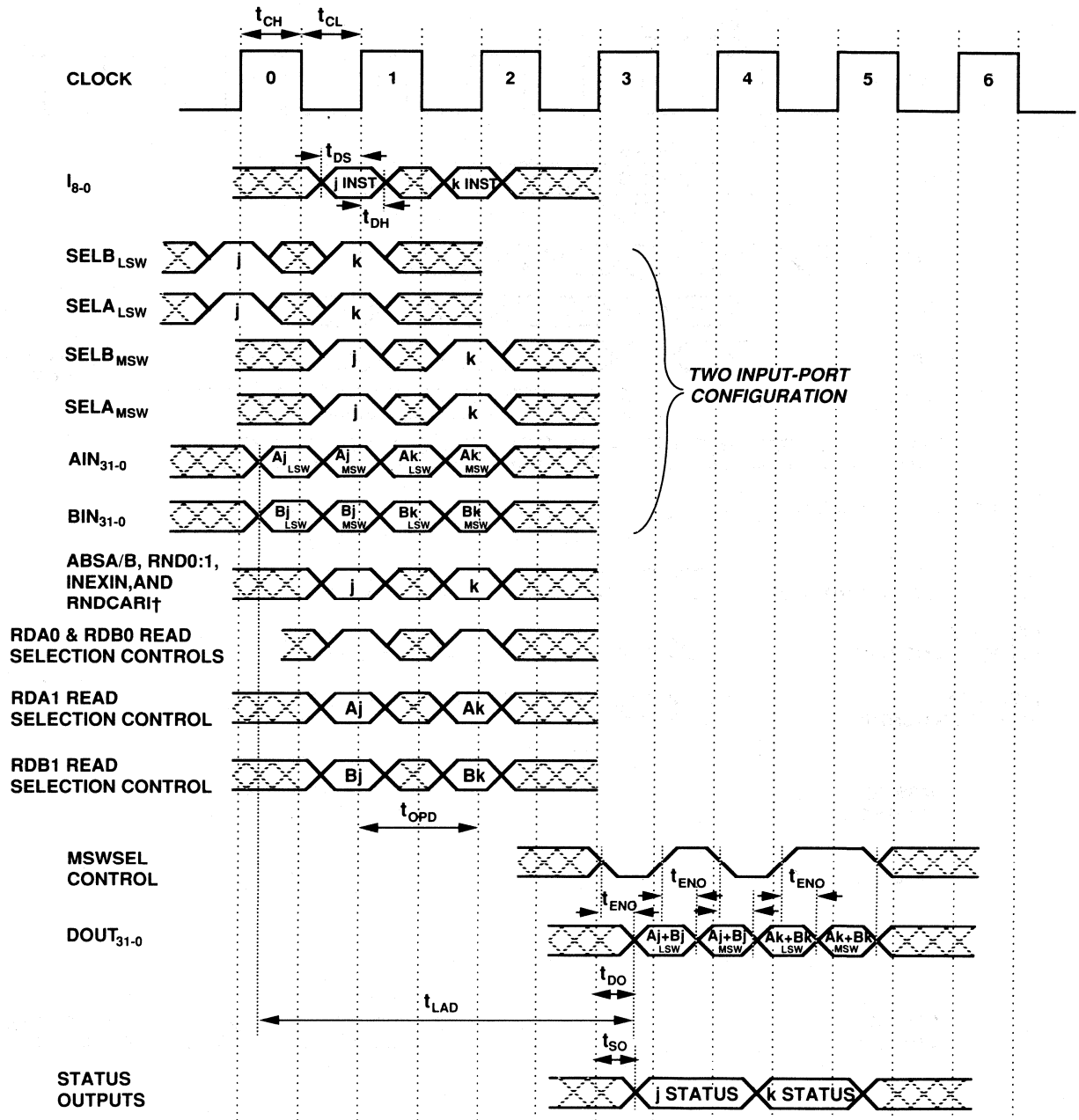
[†]RNDCAI AND INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 3. 32-Bit Single-Precision Floating-Point Logical and Fixed-Point ALU Operation



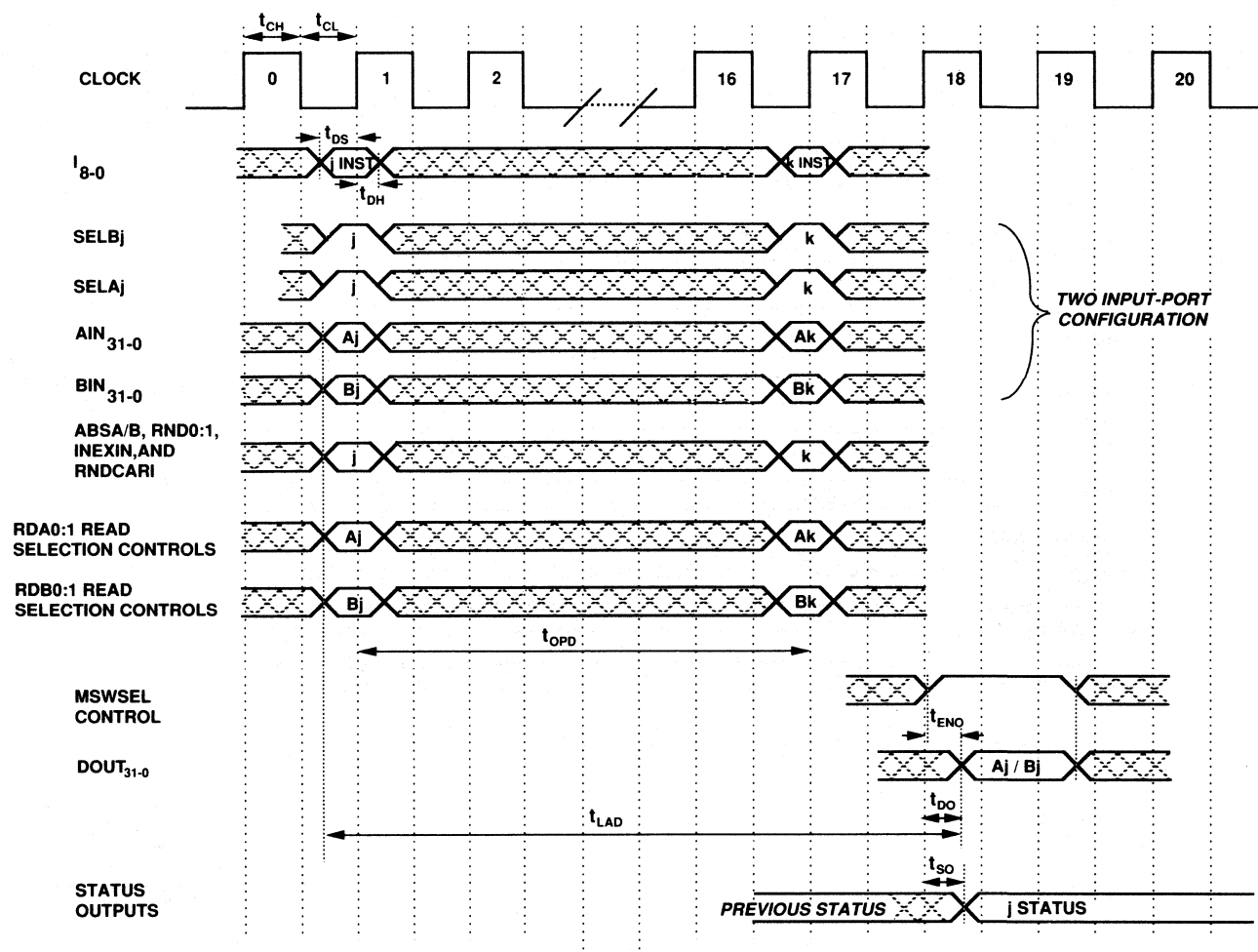
†RNDCAI AND INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 4. 64-Bit Double-Precision Floating Point ALU Operations – One Port Configuration



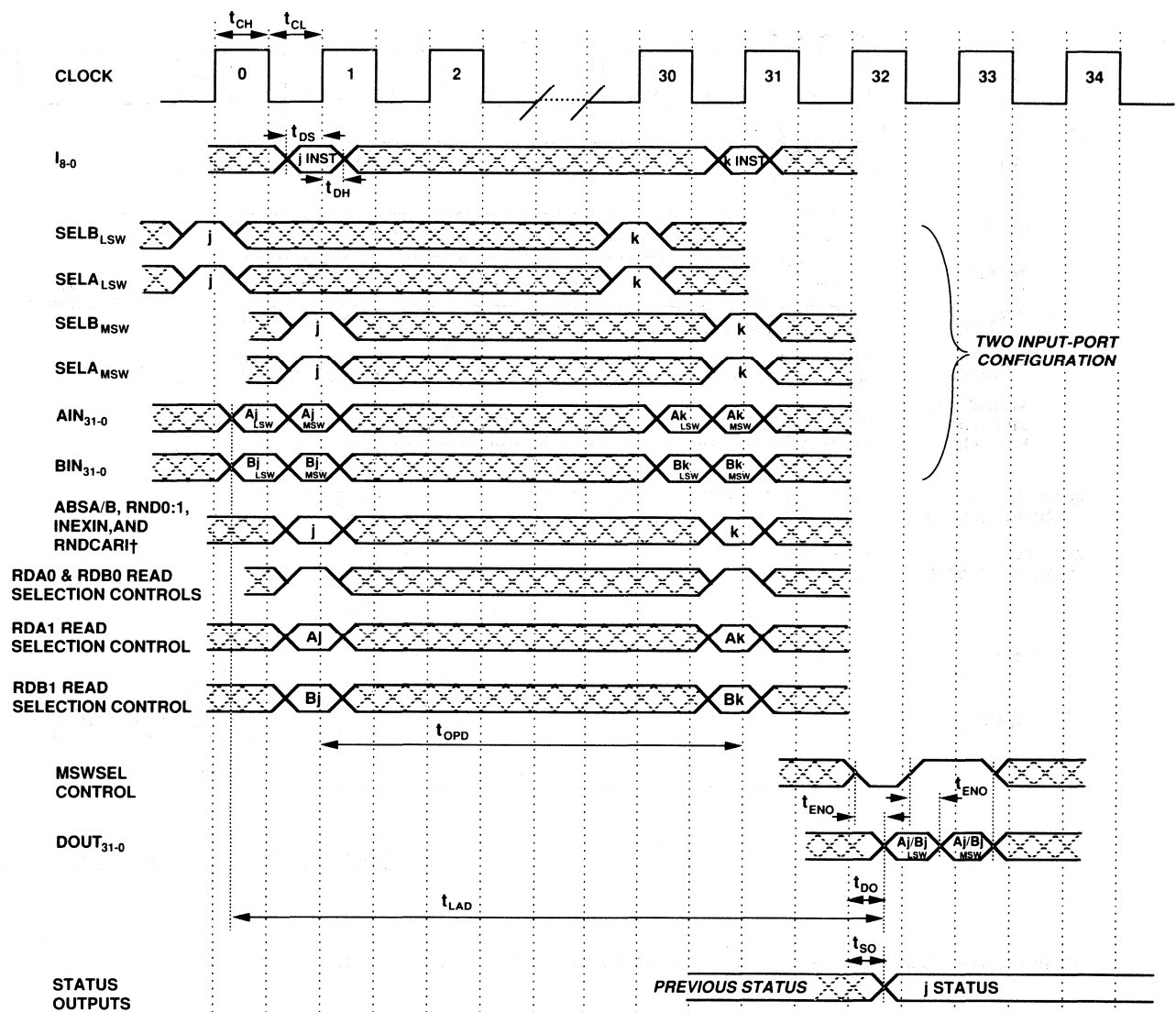
†RNDCAI and INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 5. 64-Bit Double-Precision Floating-Point ALU Operations – Two-Port Configuration



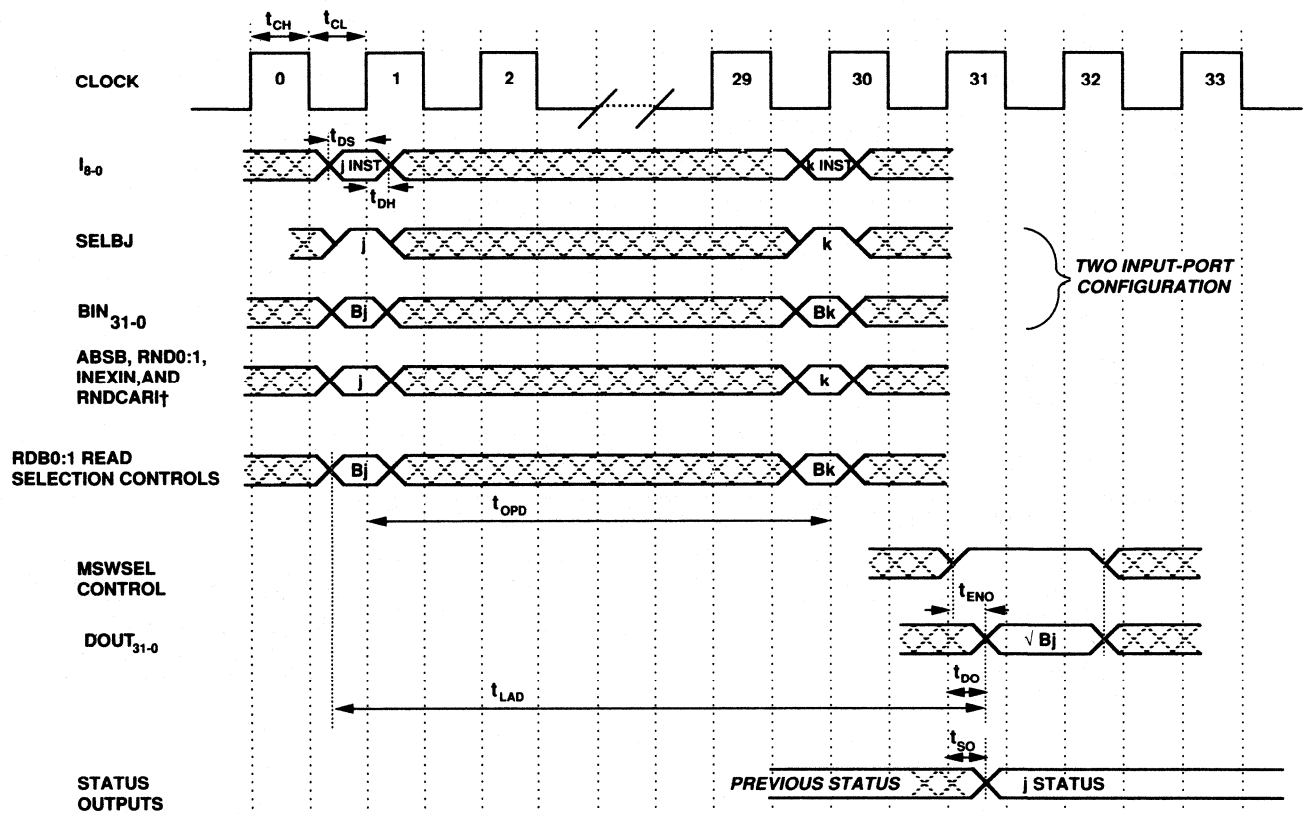
†RNDCAI AND INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 6. 32-Bit Single-Precision Floating-Point Division – Two Input-Port Configuration



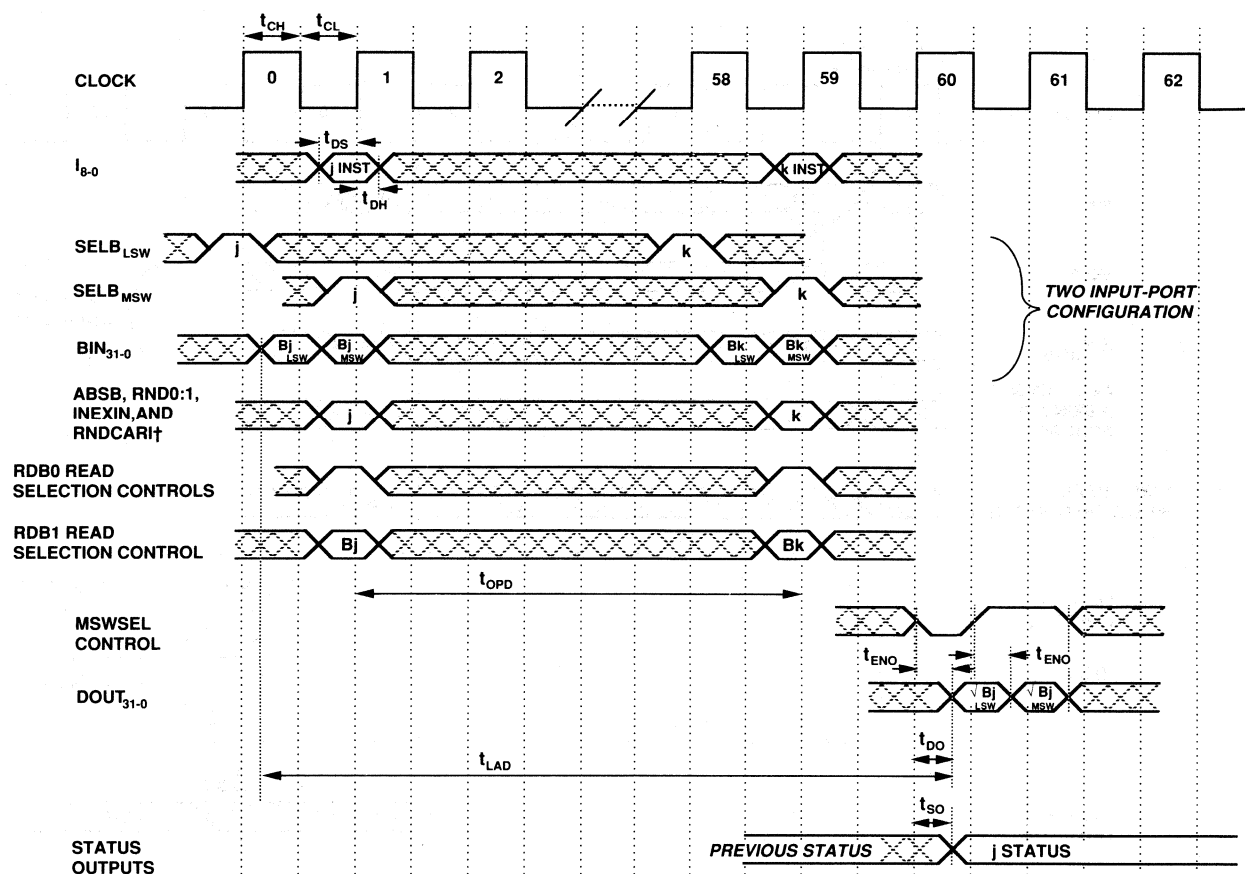
†RNSDCARI AND INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 7. 64-Bit Double-Precision Floating-Point Division – Two Input-Port Configuration



†RNDCARIT AND INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 8. 32-Bit Single-Precision Floating-Point Square Root – Two Input-Port Configuration



†RNDCAR AND INEXIN SHOULD BE LO EXCEPT FOR UNWRAP, DIVISION, AND SQUARE ROOT OPERATIONS.

Figure 9. 64-Bit Double-Precision Floating-Point Square Root – Two Input-Port Configuration

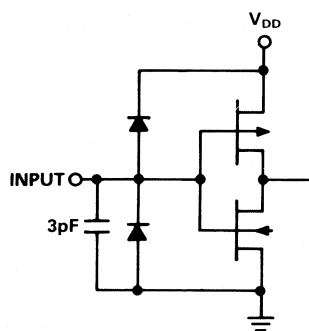


Figure 10. Equivalent Input Circuits

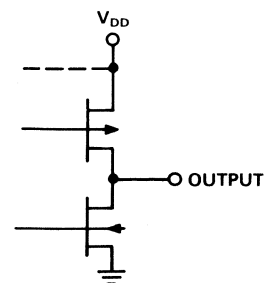


Figure 11. Equivalent Output Circuits

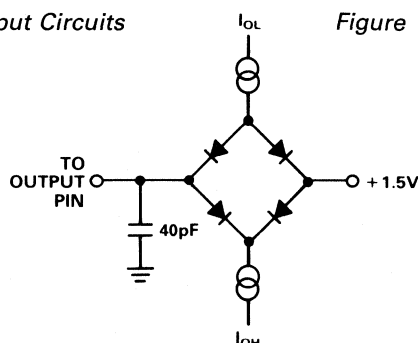


Figure 12. Normal Load for AC Measurements

5.0 ADSP-3221 Floating-Point ALU Instructions.

For all operations involving two operands, the operands may be in SP Floating point format. DP Floating point, or 32-bit FIXED point, but both operands must be of the same data type.

Note that for all arithmetic operations (SP, DP, and FIXED), the ABSA and ABSB controls can be used with the input operands, causing the absolute value of the respective operand to be used in the operation.

ADSP-3221 Fixed-Point Operation

INSTRUCTION	OPCODE									COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	
IADD	0	0	1	0	0	0	0	1	1	Integer Add (A+B)
ISUBA	0	0	1	0	0	0	1	1	1	Integer Subtract (B-A)
ISUBB	0	0	1	0	0	1	0	1	1	Integer Subtract (A-B)
IADDWC	0	0	1	0	1	0	0	1	1	Integer Add with Carry (A+B) ¹
ISUBWBA	0	0	1	0	1	0	1	1	1	Integer Subtract with Borrow (B-A) ¹
ISUBWBB	0	0	1	0	1	1	0	1	1	Integer Subtract with Borrow (A-B) ¹
INEGA	0	0	1	0	0	0	1	0	1	Perform Twos Complement Negation of the A Operand
INEGB	0	0	1	0	0	1	0	1	0	Perform Twos Complement Negation of the B Operand
IADDAS	0	0	1	1	0	0	0	1	1	Absolute Value of (A+B)
ISUBAAS	0	0	1	1	0	0	1	1	1	Absolute Value of (B-A)
ISUBBAS	0	0	1	1	0	1	0	1	1	Absolute Value of (A-B)

ADSP-3221 Logical Operations

INSTRUCTION	OPCODE									COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	
COMPL A	0	0	0	0	0	0	1	0	1	Ones Complement the A Operand
COMPL B	0	0	0	0	0	1	0	1	0	Ones Complement the B Operand
PASS A	0	0	0	0	0	0	0	0	1	Passes the A Operand (selected with RDA1, RDA0) unmodified to the output.
PASS B	0	0	0	0	0	0	0	1	0	Passes the B Operand (selected with RDB1, RDB0) unmodified to the output.
A AND B	0	0	0	0	1	0	0	1	0	Bitwise AND
A OR B	0	0	0	1	0	0	0	1	0	Bitwise OR
A XOR B	0	0	0	1	1	0	0	1	0	Bitwise Exclusive OR
NOP	0	0	0	0	0	0	0	0	0	No Operation. Preserves status flags but does not preserve the contents of the output register.
CLR	1	0	0	0	0	0	0	0	0	Clear. Sets the UNDFLO, OVERFLO, INVALOP, and INEXO flags to zero The Output Register result is not meaningful.

NOTE

¹The Carry bit in fixed point arithmetic is latched internally, for one-cycle only, to act as a Carry-In pin for the operations. Add with Carry or Subtract with Borrow. These instructions are used in performing 64-bit addition or subtraction. See note on Special Instructions in the commercial data sheet.

Table 2. ADSP-3221 Instruction Set

ADSP-3221 Single-Precision Floating-Point Operations

INSTRUCTION	OPCODE										COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
SADD	1	1	1	0	0	0	0	1	1	Floating Point SP Add (A+B)	
SSUBB	1	1	1	0	0	0	1	1	1	Floating SP Subtract (A-B)	
SSUBA	1	1	1	0	0	1	0	1	1	Floating SP Subtract (B-A)	
SCOMP	1	1	1	0	0	1	1	1	1	SP Compare. Operation is (A-B); Output Result is (A-B); Flags OVRFLO and UNDFLO generated conditional on Greater Than or Less Than conditions, respectively. If equal, output is zero and UNDFLO and OVRFLO are both LOW.	
SADDAS	0	1	1	0	0	0	0	1	1	SP Absolute Value of (A+B)	
SSUBBAS	0	1	1	0	0	0	1	1	1	SP Absolute Value of (B-A)	
SSUBAAS	0	1	1	0	0	1	0	1	1	SP Absolute Value of (B-A)	
FIX A	0	1	1	0	0	1	1	0	1	Convert 32-bit Single-Precision Floating-Point A operand→32-bit Integer	
FIX B	0	1	1	0	0	1	1	1	0	Convert 32-bit Single-Precision Floating-Point B operand→32-bit Integer	
FLOAT A	0	1	1	1	0	0	1	0	1	Convert 32-bit FIXED A operand→32-bit Single-Precision Floating-Point	
FLOAT B	0	1	1	1	0	0	1	1	0	Convert 32-bit FIXED B operand→32-bit Single-Precision Floating-Point	
DOUBLE A	0	1	1	1	0	1	1	0	1	Convert 32-bit Single-Precision A operand→64-bit Double-Precision Floating ¹	
DOUBLE B	0	1	1	1	0	1	1	1	0	Convert 32-bit Single-Precision B operand→64-bit Double-Precision Floating ¹	
SPASS A	0	1	1	1	1	0	0	0	1	Pass SP A operand. A NAN is passed unmodified but causes the INVALOP exception	
SPASS B	0	1	1	1	1	0	0	1	0	Pass SP B operand. A NAN is passed unmodified but causes the INVALOP exception	
SWRAP A	0	1	1	1	0	0	0	0	1	Converts SP denormalized A operand→Wrapped format ²	
SWRAP B	0	1	1	1	0	0	0	1	0	Converts SP denormalized B operand→Wrapped format ²	
SUNWRAP A	0	1	1	0	1	0	0	0	1	Converts Wrapped A operand→SP denormalized format ²	
SUNWRAP B	0	1	1	0	1	0	0	1	0	Converts Wrapped B operand→SP denormalized format ²	
SSIGN ³	0	1	1	1	1	1	1	0	1	Transfers sign of the B operand to the A operand. Result is Sign B, Expt A, Fraction A.	
SXSUB ³	0	1	1	1	1	1	0	0	1	Exponent Subtract. Subtracts the B exponent from the A exponent. Result is Sign A, (Expt A - Expt B), Fraction A. NANs and Infinities are operated on directly without flagging the INVALOP exception. If the Expt of the Result underflows to -127 or less, then the Output Result returned is Zero. If the Expt of the Result overflows to +128, then the Output Result returned is Infinity.	
SITRN ³	0	1	1	0	1	0	1	0	1	Integer Shift and Truncation. The A mantissa with hidden bit restored (24 bits) is treated as a right-justified unsigned integer and shifted down logically by the unbiased B exponent. ⁴ The 32-bit right-justified result appears in the MSW and is a left-zero-filled unsigned-magnitude integer. The shift value given by the unbiased B exponent is interpreted as an unsigned number; negative unbiased exponents cause very large down shifts.	

Table 2. ADSP-3221 Instruction Set (Continued)

ADSP-3221 Single-Precision Floating-Point Operations (Continued)

INSTRUCTION	OPCODE									COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	
SDIV	0	1	1	1	1	0	1	1	1	SP Fltg Pt. (A ÷ B)
SSQR	1	1	1	1	1	0	1	1	0	SP Fltg Pt. $\sqrt{B}$

NOTES

¹Conversion from Single to Double format are always exact, so INEXO will always be LOW for these conversions.

²For information on handling denormals, wrapped, and unwrapped numbers, see Application Note on "Handling IEEE Exceptions".

³See note on Special Instructions in the commercial data sheet.

⁴An unbiased exponent is the exponent after the proper exponent bias has been subtracted.

ADSP-3221 Double-Precision Floating-Point Operations

INSTRUCTION	OPCODE									COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	
DADD	1	1	0	0	0	0	0	1	1	DP Add (A+B)
DSUBB	1	1	0	0	0	0	1	1	1	DP Subtract (A−B)
DSUBA	1	1	0	0	0	1	0	1	1	DP Subtract (B−A)
DCOMP	1	1	0	0	0	1	1	1	1	DP Compare. Operation is (A−B); Output Result is (A−B); Flags OVRFLO and UNDFLO generated conditional on Greater Than or Less Than conditions, respectively. If equal, output is zero and UNFLO and OVRFLO are both LOW.
DADDAS	0	1	0	0	0	0	0	1	1	DP Absolute Value of (A+B)
DSUBBAS	0	1	0	0	0	0	1	1	1	DP Absolute Value of (A−B)
DSUBAAS	0	1	0	0	0	1	0	1	1	DP Absolute Value of (B−A)
DFIX A	0	1	0	0	1	1	1	0	1	Convert 64-bit Double-Precision A operand→32-bit Integer
DFIX B	0	1	0	0	1	1	1	1	0	Convert 64-bit Double-Precision B operand→32-bit Integer
DFLOAT A ¹	0	1	0	1	0	0	1	0	1	Convert 32-bit FIXED A operand→64-bit Double-Precision Floating-Point
DFLOAT B ¹	0	1	0	1	0	0	1	1	0	Convert 32-bit FIXED B operand→64-bit Double-Precision Floating-Point
SINGLE A	1	1	0	0	1	1	1	0	1	Convert 64-bit Double-Precision A operand→32-bit Single-Precision
SINGLE B	1	1	0	0	1	1	1	1	0	Convert 64-bit Double-Precision B operand→32-bit Single-Precision
DPASSA	0	1	0	1	1	0	0	0	1	Pass DP A operand. A NAN is passed unmodified but causes the INVALOP exception.
DPASS B	0	1	0	1	1	0	0	1	0	Pass DP B operand. A NAN is passed unmodified but causes the INVALOP exception.
DWRAP A	0	1	0	1	0	0	0	0	1	Converts DP denormalized A operand→Wrapped format ²
DWRAP B	0	1	0	1	0	0	0	1	0	Converts DP denormalized B operand→Wrapped format ²
DUNWRAP A	0	1	0	0	1	0	0	0	1	Converts Wrapped A operand→DP denormalized format ²
DUNWRAP B	0	1	0	0	1	0	0	1	0	Converts Wrapped B operand→DP denormalized format ²

Table 2. ADSP-3221 Instruction Set (Continued)

ADSP-3221 Double-Precision Floating-Point Operations (Continued)

INSTRUCTION	OPCODE										COMMENT
	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
DSIGN	0	1	0	1	1	1	1	0	1	Transfers sign of the B operand to the A operand. Result is Sign B, Expt A, Fraction A.	
DXSUB	0	1	0	1	1	1	0	0	1	Exponent subtract. Subtracts the B exponent from the A exponent. Result is Sign A, (Expt A – Expt B), Fraction A. NaNs and Infinities are operated on directly without flagging the INVALOP exception. If the Expt of the Result underflows to –1023 or less, then the Output Result returned is Zero. If the Expt of the Result overflows to +1024, then the Output Result returned is Infinity.	
DITRN	0	1	0	0	1	0	1	0	1	Integer Shift and Truncation. The A mantissa with hidden bit restored (53 bits) is treated as a right-justified unsigned integer and shifted down logically by the unbiased B exponent. ³ The 32-bit right-justified result appears in the MSW and is a left-zero-filled unsigned-magnitude integer. The shift value given by the unbiased B exponent is interpreted as an unsigned number; negative unbiased exponents cause very large down shifts.	
DDIV	0	1	0	1	1	0	1	1	1	DP Fltg Pt. (A÷B)	
DSQR	1	1	0	1	1	0	1	1	0	DP Fltg Pt. $\sqrt{B}$	

NOTES

¹Conversion from FIXED to Double format are always exact. The 32-bit FIXED source operand must be fed from one of the registers A0, A2, B0 or B2 only.

²For information on handling denormals, wrapped and unwrapped numbers, see Application Note on “Handling IEEE Exceptions.”

³An unbiased exponent is the exponent after the proper exponent bias has been subtracted.

Table 2. ADSP-3221 Instruction Set

Notations Used in the Tables Below:

RN	=	Round to the Nearest Number
RP	=	Round toward Plus Infinity
RM	=	Round toward Minus Infinity
RZ	=	Round toward Zero
NORM	=	Normalized Number
DNRM	=	Denormalized Number. A Denormalized number is treated as zero internally.
WNRM	=	Wrapped Number. A wrapped number is a number with a normalized fraction and an exponent that has been decremented through zero to take on a twos-complement negative value.
UNRM	=	Unnormalized Number. An Unnormal is an Underflowed and Wrapped Number. An UNRM can result from a multiplication of 1 or 2 Wrapped Numbers.
NORM.MAX	=	Maximum Normalized Number Representable in the Destination Format
NORM.MIN	=	Minimum Normalized Number Representable in the Destination Format
OVF	=	Overflowed Number
UNDF	=	Underflowed Number
INV	=	Invalid Operand
INF	=	Infinity
OK	=	No Exception Status Generated

In the tables below, the first mnemonic in each box describes the flag that is set, the second is the result on the DOUT pins.

B operand A operand		ZERO		DNRM		NORM		INF		NAN	
		result	status	result	status	result	status	result	status	result	status
ZERO	ZERO	ZERO ²		DNRM		NORM		INF		NAN	INVALOP
DNRM	DNRM	DNRM		NORM DNRM ZERO		INF,NORM.MAX ¹ NORM DNRM	OVRFLO	INF		NAN	INVALOP
NORM	NORM	NORM		INF,NORM.MAX ¹ NORM DNRM	OVRFLO	INF,NORM.MAX ¹ NORM DNRM ZERO	OVRFLO	INF		NAN	INVALOP
INF	INF	INF		INF		INF		INF ³ NAN ³	INVALOP	NAN	INVALOP
NAN	NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."
2. $(\pm \text{ZERO}) + (\pm \text{ZERO}) = (\pm \text{ZERO}) - (\mp \text{ZERO}) \Rightarrow \pm \text{ZERO}$
 $(\pm \text{ZERO}) + (\mp \text{ZERO}) = (\pm \text{ZERO}) - (\pm \text{ZERO}) \Rightarrow + \text{ZERO}$ (RN, RZ, RP rounding modes)
 $(\pm \text{ZERO}) + (\mp \text{ZERO}) = (\pm \text{ZERO}) - (\pm \text{ZERO}) \Rightarrow - \text{ZERO}$ (RM rounding mode)
3. $(\pm \text{INF}) + (\pm \text{INF}) = (\pm \text{INF}) - (\mp \text{INF}) \Rightarrow \pm \text{INF}$
 $(\pm \text{INF}) + (\mp \text{INF}) = (\pm \text{INF}) - (\pm \text{INF}) \Rightarrow + \text{NAN}$ (RN, RZ, RP rounding modes)
 $(\pm \text{INF}) + (\mp \text{INF}) = (\pm \text{INF}) - (\pm \text{INF}) \Rightarrow - \text{NAN}$ (RM rounding mode)
4. If DNRM result is inexact. UNDFLO will be set.

Table 3. ADSP-3221 Floating-Point Additional Subtraction (IEEE Mode)

B operand A operand		ZERO		DNRM		NORM		INF		NAN	
		result	status	result	status	result	status	result	status	result	status
ZERO	ZERO	ZERO ²		ZERO	UNDFLO	NORM		INF		NAN	INVALOP
DNRM	ZERO	ZERO	UNDFLO	NORM ZERO		INF,NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	INF		NAN	INVALOP
NORM	NORM	NORM		INF,NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	INF,NORM.MAX ¹ NORM ZERO ZERO ⁴	OVRFLO UNDFLO	INF		NAN	INVALOP
INF	INF	INF		INF		INF		INF ³ NAN ³	INVALOP	NAN	INVALOP
NAN	NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."
2. $(\pm \text{ZERO}) + (\pm \text{ZERO}) = (\pm \text{ZERO}) - (\mp \text{ZERO}) \Rightarrow \pm \text{ZERO}$
 $(\pm \text{ZERO}) + (\mp \text{ZERO}) = (\pm \text{ZERO}) - (\pm \text{ZERO}) \Rightarrow + \text{ZERO}$ (RN, RZ, RP rounding modes)
 $(\pm \text{ZERO}) + (\mp \text{ZERO}) = (\pm \text{ZERO}) - (\pm \text{ZERO}) \Rightarrow - \text{ZERO}$ (RM rounding mode)
3. $(\pm \text{INF}) + (\pm \text{INF}) = (\pm \text{INF}) - (\mp \text{INF}) \Rightarrow \pm \text{INF}$
 $(\pm \text{INF}) + (\mp \text{INF}) = (\pm \text{INF}) - (\pm \text{INF}) \Rightarrow + \text{NAN}$ (RN, RZ, RP rounding modes)
 $(\pm \text{INF}) + (\mp \text{INF}) = (\pm \text{INF}) - (\pm \text{INF}) \Rightarrow - \text{NAN}$ (RM rounding mode)
4. Exact result.
5. In FAST mode, WRAP inputs are illegal.

Table 4. ADSP-3221 Floating-Point Addition/Subtraction (FAST Mode)

Sign	HB	f22 . . . f1	f0	Unbiased Expt	Source Name	Sign	i30	i29	i28	i27	i26	i25	i24	i23	i22 . . . i7	i6	i5	i4	i3	i2	i1	i0	Rounding Modes	Status Flags
0	1	X . . . X	X	2**	128	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	all	INVALOP
0	1	0 . . . 0	0	2**	128	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	all	INVALOP
0	1	0 . . . 0	0	2**	31	U*	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	all	OVRFLO
0	1	1 . . . 1	1	2**	30	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	all	
0	1	1 . . . 1	1	2**	23	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	all	
0	1	0 . . . 0	0	2**	23	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	all	
0	1	1 . . . 1	1	2**	22	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	RN,RP	INEXO
0	1	1 . . . 1	1	2**	22	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	RZ,RM	INEXO
0	1	0 . . . 0	0	2**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	all	
0	1	1 . . . 1	1	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RN,RP	UNDFLO,INEXO
0	1	1 . . . 1	1	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RZ,RM	UNDFLO,INEXO
0	1	0 . . . 0	1	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RN,RP	UNDFLO,INEXO
0	1	0 . . . 0	1	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RZ,RM	UNDFLO,INEXO
0	1	0 . . . 0	0	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RM,RN,RZ	UNDFLO,INEXO
0	1	0 . . . 0	0	2**	-126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	2**	-126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	1	2**	-126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RP	UNDFLO,INEXO
0	0	0 . . . 0	1	2**	-126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	2**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	all		
1	0	0 . . . 0	1	2**	-126	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	0	0 . . . 0	1	2**	-126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	2**	-126	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	2**	-126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	2**	-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	1	2**	-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	RM,RN	UNDFLO,INEXO
1	1	0 . . . 0	1	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RP,RZ	UNDFLO,INEXO
1	1	1 . . . 1	1	2**	-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	RM,RN	UNDFLO,INEXO
1	1	1 . . . 1	1	2**	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RP,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	2**	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	all	
1	1	1 . . . 1	1	2**	22	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	RM,RN	INEXO
1	1	1 . . . 1	1	2**	22	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	RP,RZ	INEXO
1	1	0 . . . 0	0	2**	23	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	all	
1	1	1 . . . 1	1	2**	23	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	all	
1	1	1 . . . 1	1	2**	30	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	all	
1	1	0 . . . 0	0	2**	31	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	all	
1	1	0 . . . 0	1	2**	31	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	all	
1	1	0 . . . 0	0	2**	128	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	all	INVALOP
1	1	X . . . X	X	2**	128	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	all	INVALOP

**"U" denotes an undefined result.

Table 5. Conversion of 32-Bit Single-Precision Floating-Point to 32-Bit Twos-Complement Integer

Sign	HB	f51 . . . f22	f21	f20	f19 . . . f1	f0	Unbiased Expnt	Source Name	Sign	i30 . . . i1	i0	Rounding Modes	Status Flags
0	1	X . . . X	X	X	X . . . X	X	2**	1024	+	1 . . . 1	1	all	INVALOP
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	1024	+	1 . . . 1	1	all	INVALOP
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	31	U*	U . . . U	U	all	OVRFLO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	30	U	U . . . U	U	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	30	0	1 . . . 1	1	RZ,RM	INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	30	U	U . . . U	U	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2**	30	0	1 . . . 1	1	RZ,RM	INEXO
0	1	1 . . . 1	0	1	1 . . . 1	1	2**	30	U	U . . . U	U	RP	OVRFLO,INEXO
0	1	1 . . . 1	0	1	1 . . . 1	1	2**	30	0	1 . . . 1	1	RM,RN,RZ	INEXO
0	1	1 . . . 1	0	0	0 . . . 0	1	2**	30	U	U . . . U	U	RP	OVRFLO,INEXO
0	1	1 . . . 1	0	0	0 . . . 0	1	2**	30	0	1 . . . 1	1	RM,RN,RZ	INEXO
0	1	1 . . . 1	0	0	0 . . . 0	0	2**	30	0	1 . . . 1	1	all	
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	0	0	0 . . . 0	1	all	
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	one	0 . . . 0	1	RN,RP	UNDFLO,INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	one - 1LSB	0 . . . 0	0	RZ,RM	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	one - 1LSB	0 . . . 0	1	RN,RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	1/2 + 1LSB	0 . . . 0	0	RZ,RM	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	1/2 + 1LSB	0 . . . 0	0	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	1/2	0 . . . 0	1	RM,RN,RZ	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	+ NORM.MIN	0 . . . 0	1	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	+ NORM.MIN	0 . . . 0	0	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	+ DENORM.MIN	0 . . . 0	1	RP	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	+ DENORM.MIN	0 . . . 0	0	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	0	0	+ ZERO	0	0 . . . 0	0	all	
1	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	- DENORM.MIN	1 . . . 1	1	RM	UNDFLO,INEXO
1	0	0 . . . 0	0	0	0 . . . 0	1	2**	-1022	- DENORM.MIN	0 . . . 0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	- NORM.MIN	1 . . . 1	1	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1022	- NORM.MIN	0 . . . 0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	- 1/2	1 . . . 1	1	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	-1	- 1/2	0 . . . 0	0	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	- 1/2 - 1LSB	1 . . . 1	1	RM,RN	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	-1	- 1/2 - 1LSB	0 . . . 0	0	RP,RZ	UNDFLO,INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	- one + 1LSB	1 . . . 1	1	RM,RN	UNDFLO,INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	-1	- one + 1LSB	0 . . . 0	0	RP,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	0	- one	1 . . . 1	1	all	
1	1	1 . . . 1	0	0	0 . . . 0	0	2**	30		1 . . . 0	1	all	
1	1	1 . . . 1	0	0	0 . . . 0	1	2**	30		0 . . . 0	0	RM	INEXO
1	1	1 . . . 1	0	0	0 . . . 0	1	2**	30		0 . . . 0	1	RP,RN,RZ	INEXO
1	1	1 . . . 1	0	1	1 . . . 1	1	2**	30		1 . . . 0	0	RM	INEXO
1	1	1 . . . 1	0	1	1 . . . 1	1	2**	30		0 . . . 0	1	RP,RN,RZ	INEXO
1	1	1 . . . 1	1	0	0 . . . 0	0	2**	30		1 . . . 0	0	RM,RN	INEXO
1	1	1 . . . 1	1	0	0 . . . 0	0	2**	30		0 . . . 0	1	RP,RZ	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	30		1 . . . 0	0	RM,RN	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2**	30		0 . . . 0	1	RP,RZ	INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	31		1 . . . 0	0	all	
1	1	0 . . . 0	0	0	0 . . . 0	1	2**	31		0 . . . 0	0	RP,RN,RZ	INEXO
1	1	0 . . . 0	0	1	0 . . . 0	0	2**	31		1 . . . 0	0	RP,RZ	INEXO
1	1	0 . . . 0	0	1	0 . . . 0	0	2**	31		U . . . U	U	RM	OVRFLO,INEXO
1	1	0 . . . 0	0	1	0 . . . 0	0	2**	31		U . . . U	U	RP,RZ	INEXO
1	1	0 . . . 0	0	1	1 . . . 1	1	2**	31		U . . . U	U	RM,RN	OVRFLO,INEXO
1	1	0 . . . 0	1	0	0 . . . 0	0	2**	31		U . . . U	U	all	OVRFLO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	31		U . . . U	U	all	OVRFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	32		U . . . U	U	all	OVRFLO
1	1	0 . . . 0	0	0	0 . . . 0	0	2**	1024	- INF	1 . . . 1	1	all	INVALOP
1	1	X . . . X	X	X	X . . . X	X	2**	1024	- NAN	1 . . . 1	1	all	INVALOP

**"U" denotes an undefined result.

NOTE: Heavy line indicates rounding boundary in source.

Table 6. Conversion of 64-Bit Double-Precision Floating-Point to 32-Bit Twos-Complement Integer

Sign	HB	f51 . . . f30	f29	f28	f27 . . . f1	f0	Unbiased Expnt	Source Name	Sign	HB	f22 . . . f1	f0	Unbiased Expnt	Result Name	Rounding Modes	Status Flags
0	1	X . . . X	X	X	X . . . X	X	2** 1024	+ NAN	0	1	1 . . . 1	1	2** 128	+ NAN	all	INVALOP
0	1	0 . . . 0	0	0	0 . . . 0	0	2** 1024	+ INF	0	1	0 . . . 0	0	2** 128	+ INF	all	
0	1	1 . . . 1	1	1	1 . . . 1	1	2** 1023	+ NORM.MAX	0	1	0 . . . 0	0	2** 128	+ INF	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2** 1023	+ NORM.MAX	0	1	1 . . . 1	1	2** 127	+ NORM.MAX	RZ,RM	OVRFLO,INEXO
0	1	1 . . . 1	1	1	0 . . . 0	0	2** 127		1	1	1 . . . 0	0	2** 127	+ INF	RP,RN	OVRFLO,INEXO
0	1	1 . . . 1	1	1	0 . . . 0	0	2** 127		0	1	1 . . . 1	1	2** 127	+ NORM.MAX	RZ,RM	INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2** 127		0	1	1 . . . 1	1	2** 127	+ INF	RP	OVRFLO,INEXO
0	1	1 . . . 1	1	0	0 . . . 0	1	2** 127		0	1	1 . . . 1	1	2** 127	+ NORM.MAX	RM,RN,RZ	INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2** 127		0	1	1 . . . 1	1	2** 127	+ NORM.MAX	all	
0	1	1 . . . 1	1	0	0 . . . 0	1	2** 127		0	1	1 . . . 1	1	2** 127	+ NORM.MAX	RP	INEXO
0	1	1 . . . 1	0	0	0 . . . 0	0	2** 127		0	1	1 . . . 1	0	2** 127	+ NORM.MAX	RM,RN,RZ	INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2** -126		0	1	0 . . . 0	0	2** -126	+ NORM.MIN	all	
0	1	1 . . . 1	1	1	1 . . . 1	1	2** -127		0	0	1 . . . 1	1	2** -126	+ NORM.MIN	RP,RN	INEXO
0	1	1 . . . 1	1	1	1 . . . 1	1	2** -127		0	0	1 . . . 1	1	2** -126	+ DNRM.MAX	RZ,RM	UNDFLO,INEXO
0	1	1 . . . 1	1	0	0 . . . 0	0	2** -127		0	0	1 . . . 1	1	2** -126	+ DNRM.MAX	all	
0	1	0 . . . 0	0	0	0 . . . 0	0	2** -149		0	0	0 . . . 0	1	2** -126	+ DNRM.MIN	all	
0	1	0 . . . 0	0	0	0 . . . 0	0	2** -1022	+ NORM.MIN	0	0	0 . . . 0	1	2** -126	+ DNRM.MIN	RP	UNDFLO,INEXO
0	1	0 . . . 0	0	0	0 . . . 0	0	2** -1022	+ NORM.MIN	0	0	0 . . . 0	0	2** -126	+ ZERO	RM,RN,RZ	UNDFLO,INEXO
0	0	1 . . . 1	1	1	1 . . . 1	1	2** -1022	+ DNRM.MAX	0	0	0 . . . 0	1	2** -126	+ DNRM.MIN	RP	UNDFLO,INEXO
0	0	1 . . . 1	1	1	1 . . . 1	1	2** -1022	+ DNRM.MAX	0	0	0 . . . 0	0	2** -126	+ ZERO	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2** -1022	+ DNRM.MIN	0	0	0 . . . 0	1	2** -126	+ DNRM.MIN	RP	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	1	2** -1022	+ DNRM.MIN	0	0	0 . . . 0	0	2** -126	+ ZERO	RM,RN,RZ	UNDFLO,INEXO
0	0	0 . . . 0	0	0	0 . . . 0	0	0	+ ZERO	0	0	0 . . . 0	0	0	+ ZERO	all	
1	0	0 . . . 0	0	0	0 . . . 0	0	0	- ZERO	1	0	0 . . . 0	0	0	- ZERO	all	
1	0	0 . . . 0	0	0	0 . . . 0	1	2** -1022	- DNRM.MIN	1	0	0 . . . 0	1	2** -126	- DNRM.MIN	RM	UNDFLO,INEXO
1	0	0 . . . 0	0	0	0 . . . 0	1	2** -1022	- DNRM.MIN	1	0	0 . . . 0	0	2** -126	- ZERO	RP,RN,RZ	UNDFLO,INEXO
1	0	1 . . . 1	1	1	1 . . . 1	1	2** -1022	- DNRM.MAX	1	0	0 . . . 0	1	2** -126	- DNRM.MIN	RM	UNDFLO,INEXO
1	0	1 . . . 1	1	1	1 . . . 1	1	2** -1022	- DNRM.MAX	1	0	0 . . . 0	0	2** -126	- ZERO	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2** -1022	- DNRM.MIN	1	0	0 . . . 0	1	2** -126	- DNRM.MIN	RM	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2** -1022	- DNRM.MIN	1	0	0 . . . 0	0	2** -126	- ZERO	RP,RN,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2** -149		1	0	0 . . . 0	1	2** -126	- DNRM.MIN	all	
1	1	1 . . . 1	1	0	0 . . . 0	0	2** -127		1	0	1 . . . 1	1	2** -126	- DNRM.MAX	all	
1	1	1 . . . 1	1	1	1 . . . 1	1	2** -127		1	0	1 . . . 1	1	2** -126	- NORM.MIN	RM,RN	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2** -127		1	0	1 . . . 1	1	2** -126	- DNRM.MAX	RP,RZ	UNDFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2** -126		1	1	0 . . . 0	0	2** -126	- NORM.MIN	all	
1	1	1 . . . 1	1	0	0 . . . 0	1	2** 127		1	1	1 . . . 1	1	2** 127	- NORM.MAX	RM	
1	1	1 . . . 1	1	0	0 . . . 0	1	2** 127		1	1	1 . . . 1	0	2** 127		RP,RN,RZ	INEXO
1	1	1 . . . 1	1	0	0 . . . 0	0	2** 127		1	1	1 . . . 1	1	2** 127	- NORM.MAX	all	
1	1	1 . . . 1	1	0	0 . . . 0	1	2** 127		1	1	1 . . . 1	1	2** 127	- INF	RM	OVRFLO,INEXO
1	1	1 . . . 1	1	0	0 . . . 0	1	2** 127		1	1	1 . . . 1	1	2** 127	- NORM.MAX	RP,RN,RZ	INEXO
1	1	1 . . . 1	1	1	0 . . . 0	0	2** 127		1	1	1 . . . 1	1	2** 127	- INF	RM,RN	OVRFLO,INEXO
1	1	1 . . . 1	1	1	0 . . . 0	0	2** 127		1	1	1 . . . 1	1	2** 127	- NORM.MAX	RP,RZ	INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2** 1023	- NORM.MAX	1	1	0 . . . 0	0	2** 128	- INF	RM,RN	OVRFLO,INEXO
1	1	1 . . . 1	1	1	1 . . . 1	1	2** 1023	- NORM.MAX	1	1	1 . . . 1	1	2** 127	- NORM.MAX	RP,RZ	OVRFLO,INEXO
1	1	0 . . . 0	0	0	0 . . . 0	0	2** 1024	- INF	1	1	0 . . . 0	0	2** 128	- INF	all	
1	1	X . . . X	X	X	X . . . X	X	2** 1024	- NAN	1	1	1 . . . 1	1	2** 128	- NAN	all	INVALOP

NOTE: Heavy line indicates rounding boundary in source.

Table 7. Conversion of 64-Bit Double-Precision Floating-Point to 32-Bit Single-Precision Floating Point (IEEE Mode)

		B operand											
		ZERO		DNRM		WRAP		NORM		INF		NAN	
A operand		result	status	result	status	result	status	result	status	result	status	result	status
ZERO		NAN	INVALOP	ZERO		ZERO		ZERO		ZERO		NAN	INVALOP
DNRM		INF ¹	OVRFLO& INVALOP	NAN	UNDFLO& INVALOP	NAN	UNDFLO INVALOP	NAN	UNDFLO INVALOP	ZERO		NAN	INVALOP
WRAP		INF ¹	OVRFLO& INVALOP	NAN	UNDFLO& INVALOP	NORM		NORM WRAP UNRM	UNDFLO UNDFLO	ZERO		NAN	INVALOP
NORM		INF ¹	OVRFLO& INVALOP	NAN	UNDFLO& INVALOP	INF,NORM.MAX ¹ NORM	OVRFLO	INF,NORM.MAX ¹ NORM WRAP UNRM	OVRFLO UNDFLO UNDFLO	ZERO		NAN	INVALOP
INF		INF		INF		INF		INF		NAN	INVALOP	NAN	INVALOP
NAN		NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode.
In FAST mode, WRAP inputs are illegal.

Table 8. ADSP-3221 Floating-Point Division ($A \div B$) (IEEE Mode)

		B operand									
		ZERO		DNRM		NORM		INF		NAN	
A operand		result	status	result	status	result	status	result	status	result	status
ZERO		NAN	INVALOP	NAN	INVALOP	ZERO		ZERO		NAN	INVALOP
DNRM		NAN	INVALOP	NAN	INVALOP	ZERO		ZERO		NAN	INVALOP
NORM		INF ¹	OVRFLO& INVALOP	INF ¹	OVRFLO& INVALOP	INF,NORM.MAX ¹ NORM ZERO	OVRFLO UNDFLO	ZERO		NAN	INVALOP
INF		INF		INF		INF		NAN	INVALOP	NAN	INVALOP
NAN		NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode.

Table 9. ADSP-3221 Floating-Point Division ($A \div B$) (FAST Mode)

		B operand											
		B<ZERO		±ZERO		+DNRM		+WRAP		+NORM		+INF	
Mode		result	status	result	status	result	status	result	status	result	status	result	status
IEEE		-NAN	INVALOP	±ZERO		+NAN	UNDFLO& INVALOP	NORM		NORM		+INF	
FAST		-NAN	INVALOP	±ZERO		+ZERO		NORM		NORM		+INF	

Table 10. ADSP-3221 Floating-Point Square Root ($\sqrt{B}$)

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS triple 8-bit video RAM-DAC. This consists of three 8-bit digital-to-analog converters, a 256×24 RAM color look-up table and a 3×24 overlay register.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification are as follows:

Device	Part Number
-1	ADV453S(X)40/883B
-2	ADV453S(X)66/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-40	40-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

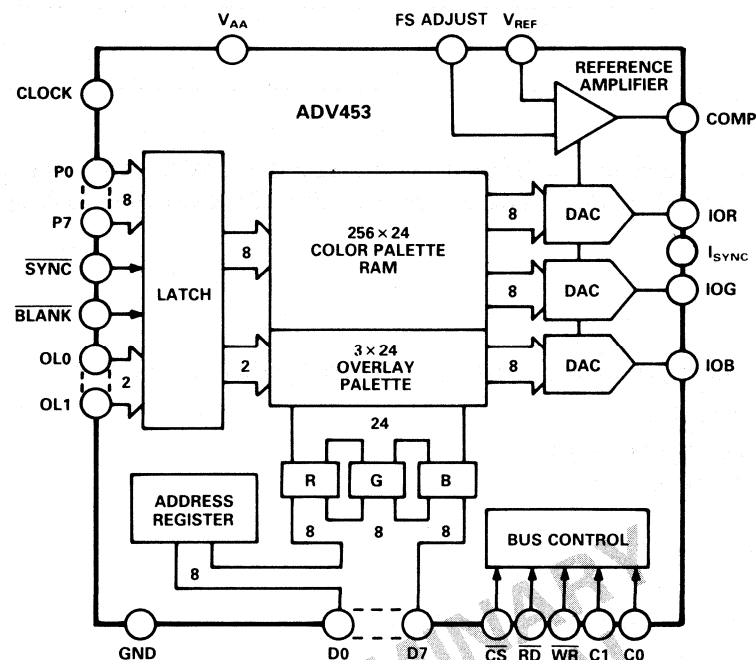
Supply Voltage	 -0.3 V, +7 V
V_{AA} to GND	 +7 V
Logic Voltage to DGND	 -0.3 V to $V_{DD} + 0.3$ V
CLK Input Voltage to DGND	 GND -0.3 V, $V_{DD} + 0.3$ V
Power Dissipation	
Up to $+75^\circ\text{C}$	 1.5 W
Derates above $+75^\circ\text{C}$	 50 mW/ $^\circ\text{C}$
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$
Storage Temperature Range	 -60°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	 $+300^\circ\text{C}$

1.5 Thermal Characteristics.

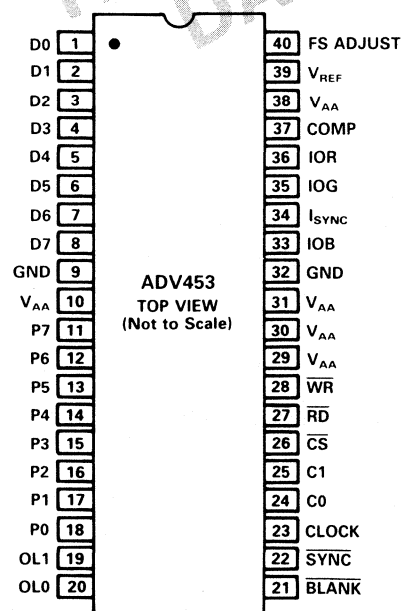
Thermal Resistance see MIL-M-38510 Appendix C.

ADV453

3.2.1 Functional Block Diagram and Terminal Assignments.

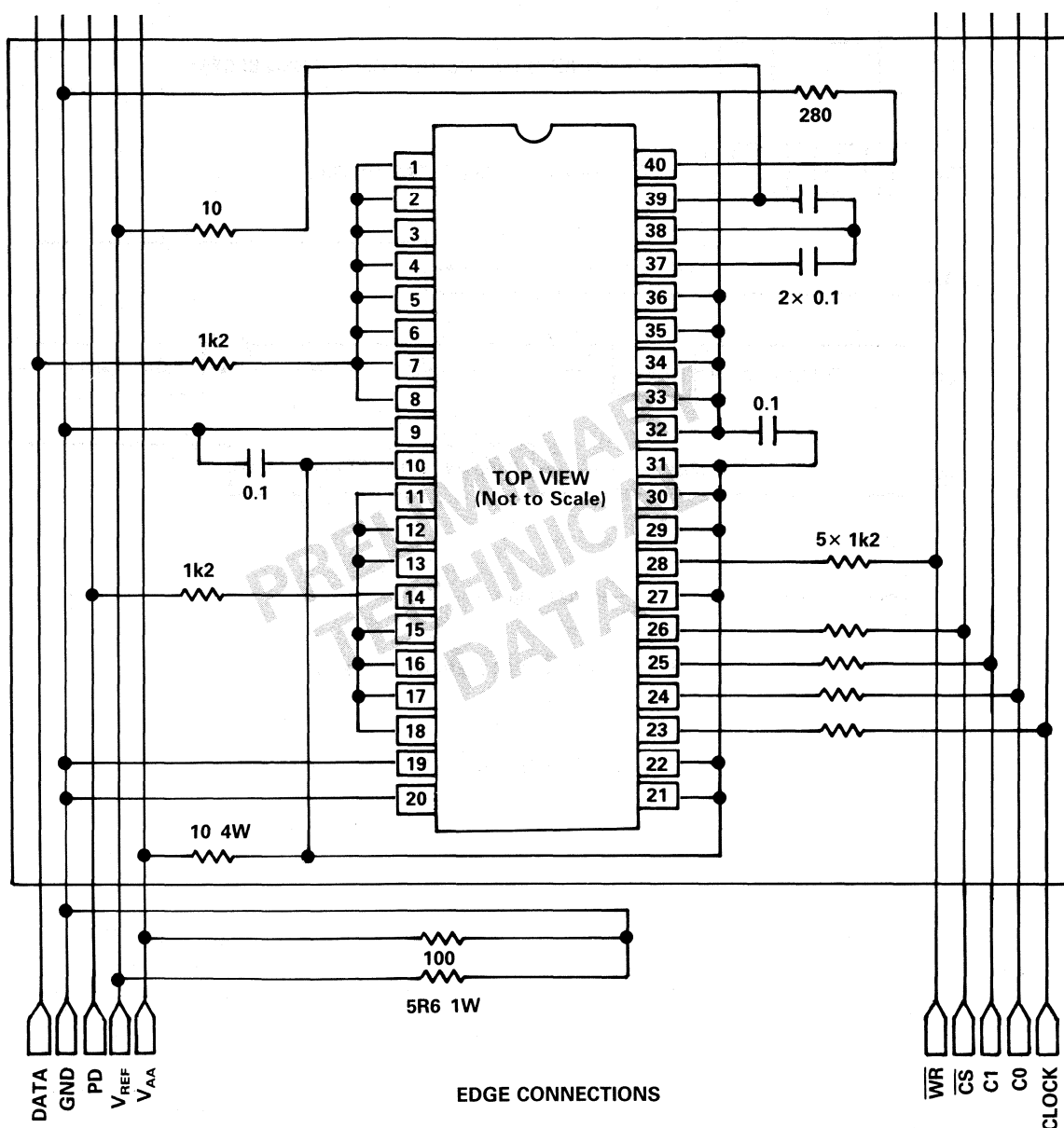


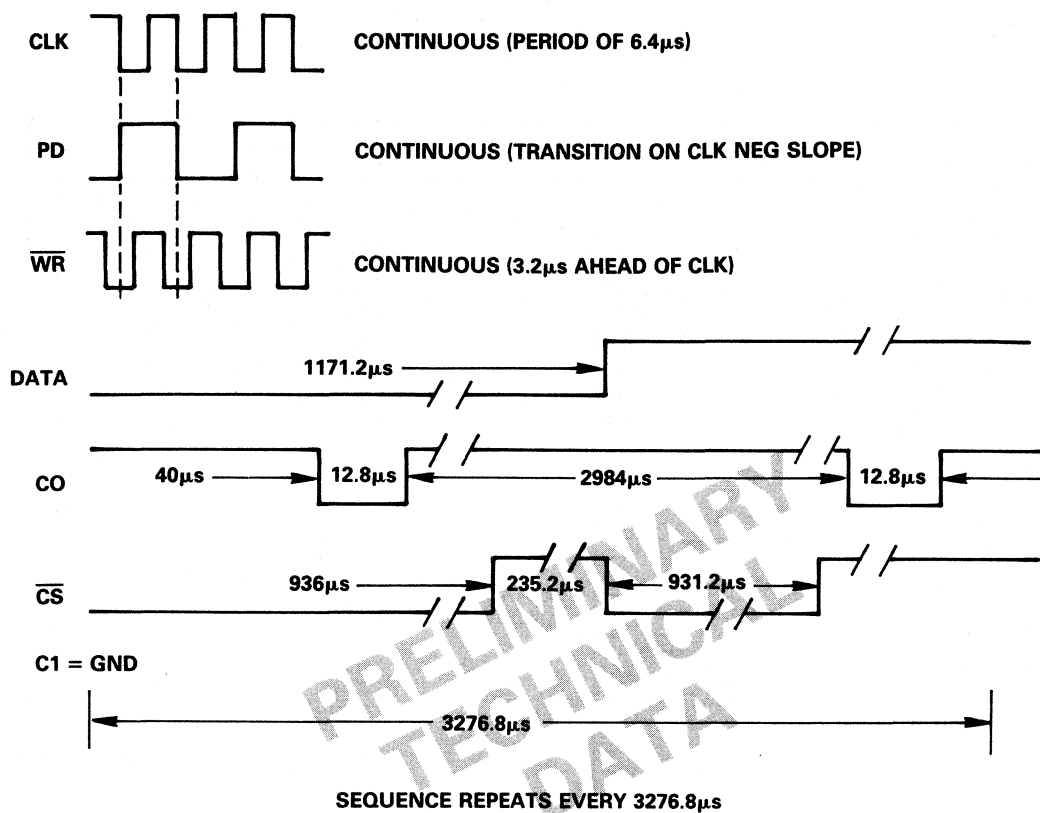
Pin Assignments



4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a voltage-to-frequency converter with a full scale range of 500kHz.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	ADVFC32SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: H-10A

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to GND	+18V
V_{EE} to GND	-18V
Input Voltage Range Pin 1 & 2	+ V_{CC}
Diff. Input Voltage Range Pin 1 & 2	- V_{EE}
Output Pullup Supply	+30V
Comparator Input Voltage	- V_{EE} to + V_{CC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 70^\circ\text{C/W}$
 $\theta_{JA} = 150^\circ\text{C/W}$

ADVFC32 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Linearity	L _E	– 1	0.01				f _{FS} = 10kHz	± % of FSR max
			0.1	0.1			f _{FS} = 100kHz 10mV < V _{IN} < 10V	± % of FSR max
			0.2				f _{FS} = 500kHz 10mV < V _{IN} < 10V	± % of FSR max
Input Offset Voltage ²	V _{OS}	– 1	4	4			V _{IN} = 20mV f _{FS} = 100kHz	± mV max
Input Offset Drift	TC _{VOS}	– 1	30		30		f _{FS} = 10kHz 25°C to 125°C	± µV/°C max
					30		– 55°C to 25°C	
			30		30		f _{FS} = 200kHz 25°C to 125°C	± µV/°C max
					30		– 55°C to 25°C	
Gain Error ²	A _E	– 1	10	10			f _{FS} = 100kHz V _{IN} = 10V	± % max
Gain Drift	TC _{AE}	– 1					V _{IN} = 10V	ppm/°C max
					+ 150		f _{FS} = 10kHz	
					– 150		25°C to 125°C	
					+ 150		f _{FS} = 10kHz	
					– 150		– 55°C to 25°C	
					+ 150		f _{FS} = 200kHz	
					– 150		25°C to + 125°C	
Power Supply Rejection	PSRR	– 1	0.015	0.015			f _{FS} = 100kHz	% of FS/% max
							V _{IN} = 200mV Noninverting Input	
							V _{IN} = 50mV Inverting input	
Input Bias Current	I _{BS}	– 1	250	250				± nA max
			100	100				
Low Level Output Voltage	V _{OL}	– 1	0.4	0.4			V _{IN} = – 0.1V I _{SINK} = 8mA	V max
Leakage Current	I _{OH}	– 1	1	1			V _{OUT} = 15V Logic 1	µA max
Quiescent Current	I _S	– 1	8	8				mA max
Settling Time	t _{SL}	– 1	See Note 3				Full Scale Step Input	max

NOTES

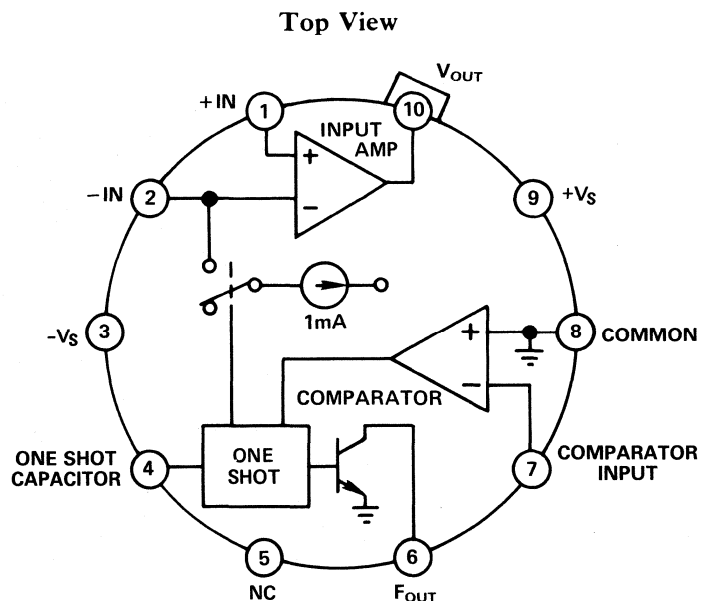
¹V_S = ± 15V, T_A = +25°C, unless otherwise specified.

²Adjustable to zero.

³1 pulse of new frequency plus 1µs.

Table 1.

3.2.1 Functional Block Diagram and Pin Assignments.

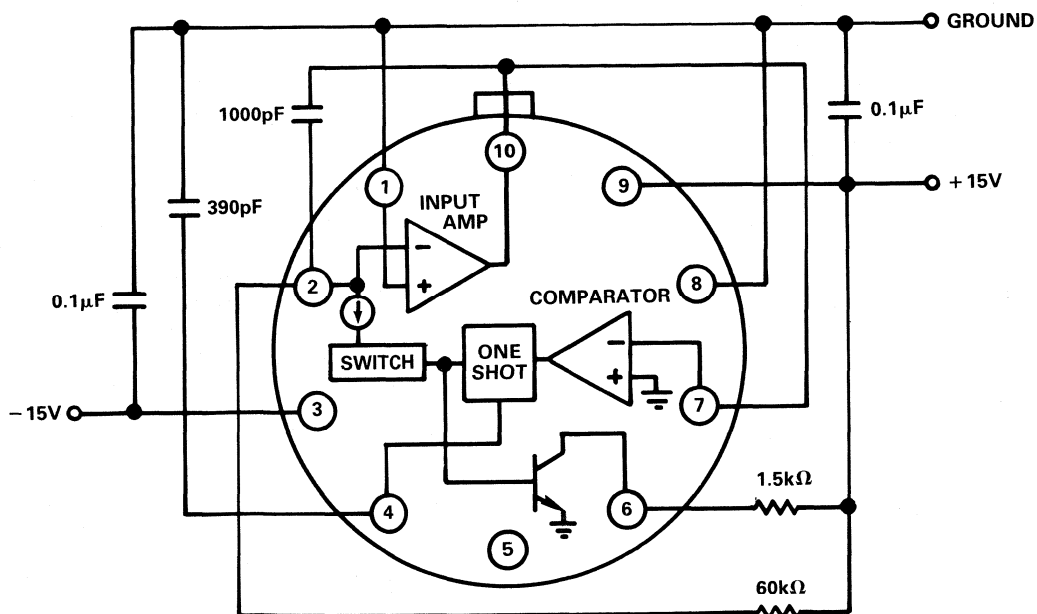


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a resolver-to-digital converter with up to 16 bits resolution and accuracies of 8 and 4 arc mins.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD2S80S(X)/883B
-2	AD2S80T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-40A	40-Lead Side Brazed Ceramic DIP
E	E-44A	44-Terminal Leadless Ceramic Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_S$ to GND ^{1, 2}	+14.0 V dc
$-V_S$ to GND ^{1, 2}	-14.0 V dc
$+V_L$ to GND ²	$+V_S$
Digital Input Voltage to GND ²	-0.4 V to $+V_L$
Demod I/P	+14.0 V to $-V_S$
Integrator I/P	+14.0 V to $-V_S$
VCO Input	+14.0 V to $-V_S$
V_{REF} to GND ^{3, 4}	+14.0 V dc to $-V_S$
Analog Input Voltage (SIN, COS) to GND ^{3, 4}	+14.0 V dc to $-V_S$
Power Dissipation	860 mW
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C

NOTES

¹The device should be powered up as follows: $-V_S$ should be applied before or simultaneously with the $+V_S$.

V_L can be applied at any time with respect to $+V_S$ and $-V_S$.

²GND refers to ANALOG GND; ANALOG GND must be externally connected to DIGITAL GND.

³SIGNAL GND is internally connected to ANALOG GND.

⁴SIN, COS REF input voltage may be present without $+V_S$, $-V_S$, $+V_L$.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 11^\circ\text{C/W}$ for D-40A
 $\theta_{JC} = 10^\circ\text{C/W}$ for E-44A

2S80 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Angular Accuracy ²		-1	±8	±8	±8	±8	+V _S = ±10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc SC1 = SC2 = High 16 Bit Resolution	arc min
							+V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc SC1 = SC2 = High 16 Bit Resolution	
Angular Accuracy ²		-2	±4	±4	±4	±4	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc SC1 = SC2 = High 16 Bit Resolution	arc min
							+V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc SC1 = SC2 = High 16 Bit Resolution	
Resolution	RES	-1, 2	16				10, 12, 14, 16 User Selectable	1 Bit in 16 1 in 65536
Differential Nonlinearity ²	DNL	-1, 2	±4	±4	±4	±4	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc SC1 = SC2 = High 16 Bit Resolution	LSB
							+V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc SC1 = SC2 = High 16 Bit Resolution	
Signal and Reference Frequency		-1, 2	50 to 20,000					Hz
Total Effective Angular Offset		-1, 2	±800	±800	±800	±800	Output Data Nulled by Application of Offset Current to Integrator Input	nA max
Integrator Output Range		-1, 2	±8	±8	±8	±8	+V _S = +12.0 V dc, V _L = 5.0 V dc -V _S = -12.0 V dc 1 mA Load	V
Integrator Output Range		-1, 2	±7	±7	±7	±7	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc 1 mA Load	V
Integrator Input Offset Voltage	V _{IO}	-1, 2	5					mV max
Integrator Dead Zone Current		-1, 2	110					nA/LSB max
Integrator Input Bias Current	I _{IB}	-1, 2	150					nA max
Integrator Input Impedance	Z _{IN}	-1, 2	1					MΩ min
Demod O/P Scaling		-1, 2	90	90	90	90		nA/ Bit min
			110	110	110	110		nA/Bit max
PSD O/P Offset Voltage		-1, 2	12					mV max
PSD Input Bias Current	I _{IB}	-1, 2	150					nA max
PSD Input Impedance	Z _{IN}	-1, 2	1					MΩ min
VCO Maximum Rate		-1, 2	1.1	1	1	1		MHz max
VCO Rate Tempco		-1, 2	-0.05					%/°C

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
VCO Gain Scaling		-1, 2	6660	6660	6660	6660	Measured with VCO Input Current of ±10 μA	Hz/μA min
			8140	8140	Sub 2 8140	8140		Hz/μA max
					Sub 3 8465			
VCO Input Bias Current	I _{IB}	-1, 2	300					nA max
VCO Input Bias Tempco		-1, 2	-0.55					nA/°C
VCO Linearity ⁴		-1, 2	±3	±3	±3	±3	VCO Measured at 10 Points over the Frequency Range 0-1 MHz	% max
VCO Total Effective Offset	I _{IO}	-1, 2	340	300	Sub 2 300	300	Measured with 68 kΩ Input Resistance	nA max
					Sub 3 340			
Tracking Rate Range		-1, 2	1074 268 67 16.7				Comment: 10 Bit RES 12 Bit RES 14 Bit RES 16 Bit RES	rps max (Revolutions per Second)
Reference Input Voltage		-1, 2	1					V Peak min
			11					V Peak max
Reference Input Impedance		-1, 2		1				MΩ min
Reference Input Bias Current		-1, 2	150					nA max
Signal Input Voltage (SIN, COS)		-1, 2	2 ±10%					V rms
Signal Input Impedance		-1, 2	1					MΩ min
Signal Input Bias Current		-1, 2	150					nA max
Signal Input Phase Shift (wrt Reference)		-1, 2	±10					Degrees max
Digital Inputs High Voltage	V _{IH}	-1, 2	2.0	2.0	2.0	2.0	DB1-DB16 $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT +V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc	V min
Digital Inputs Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8	0.8	DB1-DB16 $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT +V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc	V max
Digital Inputs High Current	I _{IH}	-1, 2	±100	±100	±100	±100	DB1-DB16 $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT V _L = 5.5 V, V _{IH} = 5.5 V +V _S = 13.2 V dc, -V _S = -13.2 V dc	μA max
Digital Inputs Low Current	I _{IL}	-1, 2	±100	±100	±100	±100	DB1-DB16 $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT V _L = 5.5 V, V _{IL} = 0.0 V +V _S = 13.2 V dc, -V _S = -13.2 V dc	μA max
Digital Inputs Low Voltage ³	V _{IL}	-1, 2	1.0	1.0	1.0	1.0	SC1, SC2 DATA LOAD, +V _S = +12.0 V dc, -V _S = -12.0 V V _L = 5.0 V, $\overline{\text{ENABLE}}$ = High	V max
Digital Inputs Low Current ³	I _{IL}	-1, 2	400	400	400	400	SC1, SC2 DATA LOAD, +V _S = +12.0 V dc, -V _S = -12.0 V V _L = 5.0 V, $\overline{\text{ENABLE}}$ = High	μA max

Table 1. (Continued on next page)

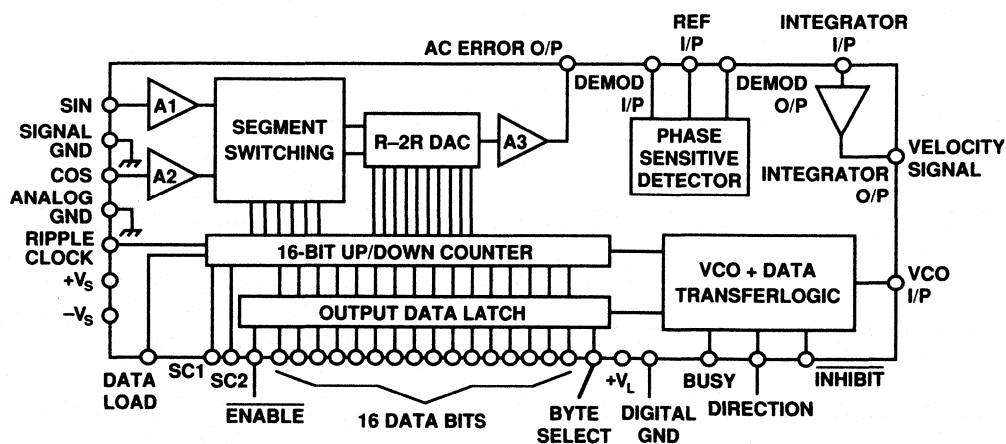
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Digital Outputs High Voltage	V_{OH}	-1, 2	2.4	2.4	2.4	2.4	DB1-DB16, RIPPLE CLOCK DIRECTION $+V_S = +12.0\text{ V}$, $V_L = 4.5\text{ V}$ $-V_S = -12.0\text{ V}$, $I_{OH} = 100\text{ }\mu\text{A}$	V min
Digital Outputs Low Voltage	V_{OL}	-1, 2	0.4	0.4	0.4	0.4	DB1-DB16, RIPPLE CLOCK DIRECTION $+V_S = +12.0\text{ V dc}$, $V_L = 5.5\text{ V dc}$ $-V_S = -12.0\text{ V}$, $I_{OL} = 1.2\text{ mA}$	V max
High Level Three State Leakage Current	I_{OZH}	-1, 2	± 100	± 100	± 100	± 100	DB1-DB16 Only $+V_S = +12.0\text{ V dc}$, $V_L = 5.5\text{ V dc}$ $-V_S = -12.0\text{ V dc}$, $V_{OL} = 5.0\text{ V dc}$	$\mu\text{A max}$
Low Level Three State Leakage Current	I_{EZH}	-1, 2	± 100	± 100	± 100	± 100	DB1-DB16 Only $+V_S = +12.0\text{ V dc}$, $V_L = 5.5\text{ V dc}$ $-V_S = -12.0\text{ V dc}$, $V_{OL} = 0.0\text{ V dc}$	$\mu\text{A max}$
Busy Pulse Width ²	t_{BUSY}	-1, 2	200	200	200	200		ns min
			600	600	600	600		ns max
Power Supply Current from $+V_S$	$+I_S$	-1, 2	30	30	30	30	$+V_S = +13.2\text{ V dc}$	mA max
Power Supply Current from $-V_S$	$-I_S$	-1, 2	-30	-30	-30	-30	$-V_S = -13.2\text{ V dc}$	mA max
Power Supply Current from $+V_L$	$+I_L$	-1, 2	1.5	1.5	1.5	1.5	$+V_S = +5.5\text{ V dc}$	mA max

NOTES

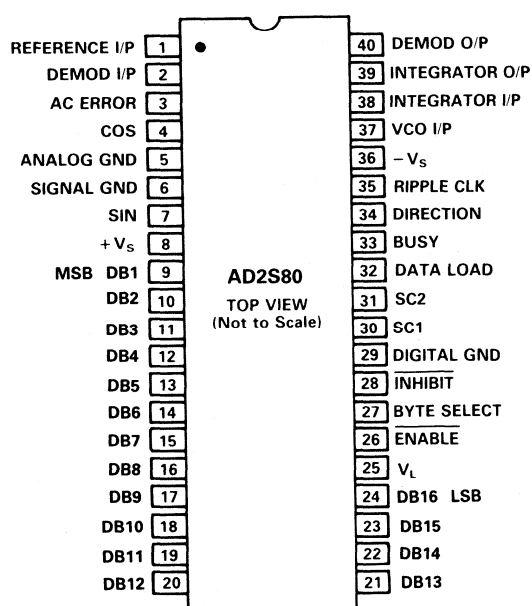
¹ $+V_S = +12.0\text{ V dc}$, $-V_S = -12.0\text{ V dc}$, $V_L = +5.0\text{ V dc}$.² V_{SIN} , $V_{COS} = 2 V_{RMS}$ Maximum at 5 kHz. $V_{REF} = 2 V_{RMS}$ at 5 kHz.³Digital inputs SC1, SC2, DATA LOAD are internally pulled up to $+V_S$.⁴VCO linearity is expressed as % (percentage) of reading.

Table 1.

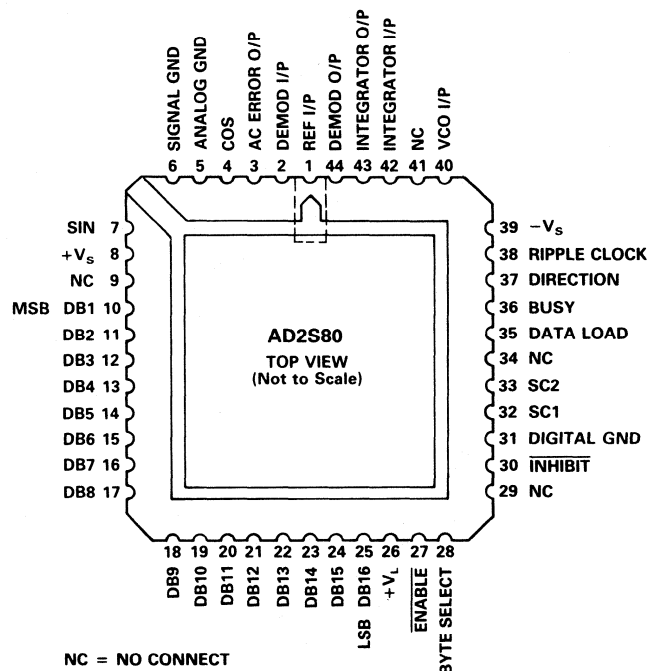
3.2.1 Functional Block Diagram and Terminal Assignments.



D Package (DIP)



E Package (LCC)

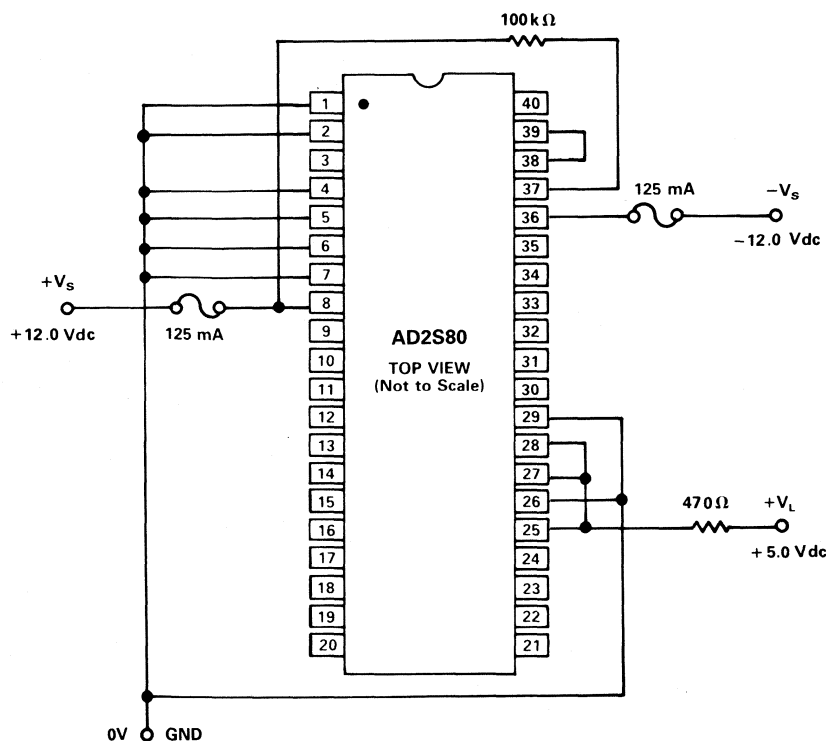


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Hybrid Circuits

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General Specification Hybrid Circuits

ADI-H-1000

1.0 SCOPE

1.1 Scope.

This specification covers the general requirements for hybrid microcircuits. Specific hybrid microcircuit requirements are in the device specification.

1.2 Part Number.

The complete part number is per paragraph 1.2 of the device specification.

1.2.1 Device Type.

The device type and electrical grade selections are per the device specification.

1.2.2 Device Class.

The device conforms to product assurance level Class B per paragraph 3.4 of MIL-H-38534.

1.2.3 Case Outline.

The case outline is per paragraph 1.2.3 of the device specification.

1.3 Absolute Maximum Ratings.

Absolute maximum ratings are per paragraph 1.3 of the device specification.

1.3.1 Recommended Operating Conditions.

1.4 Electrostatic Discharge (ESD) Damage.

ESD damage may occur to devices subjected to high energy electrostatic fields.

1.5 Thermal Characteristics.

Maximum temperature rise from junction to case and from junction to ambient are per paragraph 1.5 of the device specification.

2.0 APPLICABLE DOCUMENTS

2.1 Issues of Documents.

The following documents of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 – Microcircuits, General Specification for

MIL-M-38534 – Hybrid Microcircuits, General Specifications for

STANDARD

MILITARY

MIL-STD-1772 – Certification Requirement for Hybrid Microcircuit facilities and lines.

MIL-STD-883 – Test Methods and Procedures for Microelectronics.

2.2 Order of Precedence.

In the event of a conflict between the text of this specification, the device specification and the references cited herein, the order of precedence shall be as follows:

Device Specification
General Specification
MIL-H-38534 and/or MIL-M-38510

REV. C

3.0 REQUIREMENTS

3.1 Item Requirements.

The individual item requirements are per the device specification.

3.2 Design and Construction.

The design and construction is in accordance with paragraph 3.5 of MIL-H-38534.

3.2.1 Circuit Diagram and Terminal Connections.

The circuit functional block diagram and terminal connections are per the device specification.

3.2.2 Schematic Circuit.

The schematic circuit is on file at the factory in the device documentation package.

3.2.3 Case Outline.

The case outline is per paragraph 1.2.3 of the device specification.

3.3 Lead Material and Finish.

Lead material and finish are per MIL-M-38534 per paragraph 3.5.8.

3.4 Electrical Performance Characteristics.

The electrical performance characteristics are per Table 1 of the device specification.

3.5 Electrical Test Requirements.

The electrical test requirements as a minimum are per Table 1 below, and per the device specifications.

MIL-STD-883 TEST REQUIREMENTS Method 5008	Subgroups
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, or 7
Group A Test Requirements	1, 2, 3, 4, or 7
Group C End Point Electrical Test	1

*PDA applies to subgroup 1 (see paragraph 4.2.1.b) of this specification.

Table 1. Electrical Test Requirements

Electrical testing in the following subgroups is performed per the device specification unless otherwise noted.

Subgroup 1	Electrical Tests per the device specification @ +25°C
Subgroup 2	Electrical Tests per the device specification @ +125°C
Subgroup 3	Electrical Tests per the device specification @ -55°C
Subgroup 4	Dynamic and/or Selection Tests @ +25°C
Subgroup 7	Functional Tests at +25°C

3.6 Marking.

Each microcircuit is permanently and legibly marked per: MIL-STD-883 paragraph 1.2.1.C and paragraph 1.2 of the device specification.

3.6.1 Date Code.

The date code is per paragraph 3.6.3 of MIL-H-38534.

3.6.2 Country of Origin Cross Reference.

The following numeric codes may be substituted for the actual country of origin marking.

Country	Code
USA	50

3.7 Certificate of Conformance.

A Certificate of Conformance will be provided with each shipment of microcircuits per paragraph 1.2.1 of MIL-STD-883.

4.0 QUALITY ASSURANCE PROVISIONS**4.1 Sampling and Inspection.**

Sampling and inspection procedures are per Appendix B of MIL-M-38510 or MIL-H-38534 and Method 5008 of MIL-STD-883.

4.2 Screening.

Screening is per Method 5008 of MIL-STD-883 for Class B devices and is conducted on all devices prior to quality conformance inspections. The following additional criteria are applicable:

4.2.1 Burn-In.

Burn-In is per Method 1015 of MIL-STD-883, Condition B unless otherwise specified.

- a. The burn-in circuit is per paragraph 4.2.1 of the device specification.
- b. Percent Defective Allowable (PDA) is 10% for failures from final electrical test, subgroup 1.

4.3 Quality Conformance Inspection.

Quality conformance inspection is per paragraph 4.6 of MIL-H-38534 and as specified herein. End point electrical parameters are per the device specification (the applicable subgroup is per Table 1 of this specification).

4.4 Data Recording.

Data recording is per paragraph 4.7 of MIL-H-38534.

4.5 Change Notification.

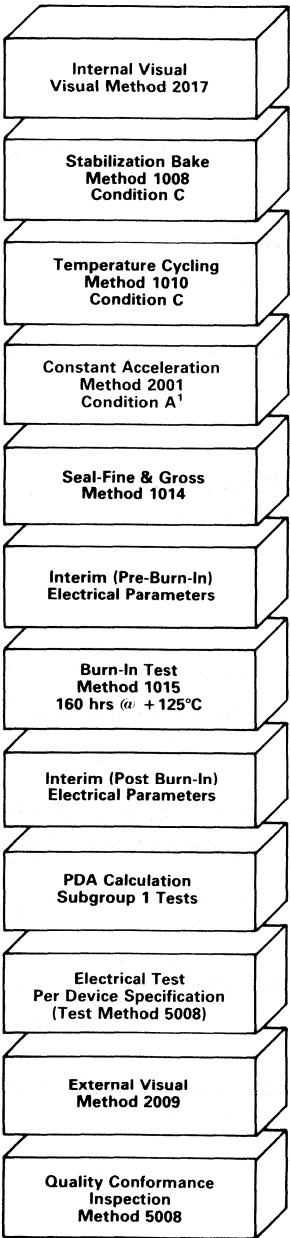
The device specification and this specification will be maintained under revision control. To determine the current revision status, contact the factory.

5.0 PACKAGING

5.1 Packaging Requirements.

The packaging requirements are per paragraph 5 of MIL-H-38534. Microcircuits which have been determined to require electrostatic discharge protection (category A) by test Method 3015 of MIL-STD-883, will be packaged in conductive material with an external conductive field shielding barrier.

HYBRID PROCESS FLOW
MIL-STD-883 METHOD 5008
CLASS B DEVICE



NOTE
¹Condition A, Y1 plane.

6.0 OTHER

1.1 Scope.

This specification covers the detail requirements for a high speed sample-and-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD346SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-14A

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_{CC}$ to GND (Pin 11)		+18V
$-V_{CC}$ to GND (Pin 14)		–18V
Digital Input (Pin 1)		0 to +7V
Analog Input (Pin 13)		$\pm 15\text{V}$
Junction Temperature		+175°C
Storage Temperature Range		–65°C to +150°C
Lead Temperature (Soldering 10sec)		+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 20^\circ\text{C/W}$
 $\theta_{JA} = 60^\circ\text{C/W}$

AD346 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Analog Input Voltage Range	V _{IN}	–1	10			10		± V min
Overvoltage, No Damage	V _{OV}	–1	15					± V max
Digital Input Logic “1” Current	I _{IH}	–1	20					μA max
Digital Input Logic “0” Current	I _{IL}	–1	360					– μA max
Digital Input Track Mode Logic “1”	V _{IH}	–1	2.0 5.5					V min V max
Digital Input Hold Mode Logic “0”	V _{IL}	–1	0 0.8					V min V max
Analog Output Voltage ²	V _O	–1	10.0			10.0		± V min
Offset Voltage ³	V _{OS}	–1	3	3				± mV max
Offset Voltage Temperature Coefficient	V _{OSTC}	–1	20		20			± mV max
Gain Error	A _E	–1	0.02	0.02			% of –1V/V	± % max
Gain Error Over Temperature	TCA _E		0.05		0.05		% of –1V/V	± % max
Offset Step (Pedestal)	O _S	–1	4	4				± mV max
Pedestal Over Temperature	TCO _S	–1	20		20			± mV max
Droop Rate	T _{DR}	–1	0.5	0.5				mV/ms max
Droop Rate over Temperature	T _{DRTC}	–1	650		650			mV/ms max
Acquisition Time to ±0.01% 10V Step	t _{A1}	–1	2.0					μs max
Acquisition Time to ±0.01% 20V Step	t _{A2}	–1	2.5			2.5		μs max
Settling Time Sample Mode	t _{S1}	–1	2.0					μs max
Sample to Hold	t _{S2}	–1	1.0					μs max
Feedthrough (Hold Mode)	FT	–1	0.02			0.02	@ C _L ≤ 200pF	% FSR max
Nominal Voltages for Rated Performance	V _S	–1	15				(± 3%)	± V typ
Power Supply Rejection Ratio	PSRR	–1	300					μV/V max
Supply Currents	+ I _{SS}	–1	18	18			V _{SS} = ± 15V	mA max
	– I _{SS}	–1	10	10			V _{SS} = ± 15V	– mA max
Supply Currents Over Temperature	+ I _{SSTC}	–1	20		20		V _{SS} = ± 15V	mA max
	– I _{SSTC}	–1	10		10		V _{SS} = ± 15V	– mA max

NOTES

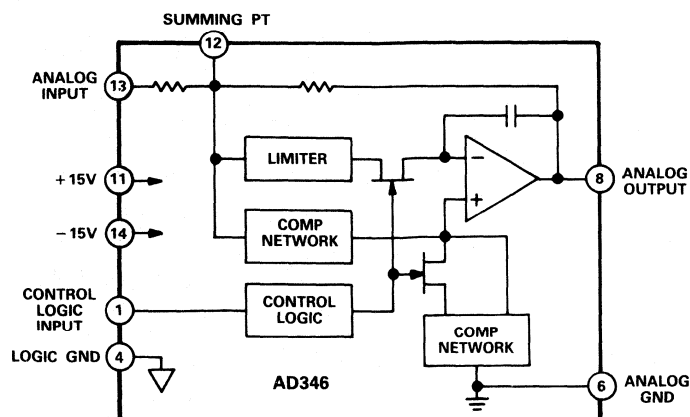
¹T_A = +25°C and ± V_S = ± 15V unless otherwise specified.

²Max Output Swing is 4V less than + V_S.

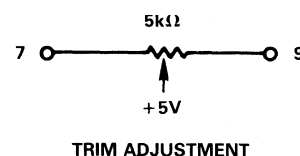
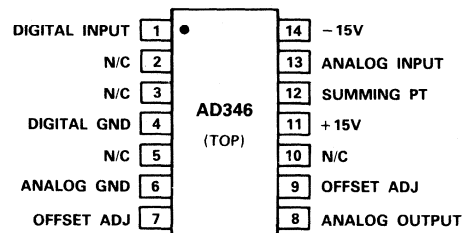
³Voltage Offset is externally adjustable to zero.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



DH-14A Package

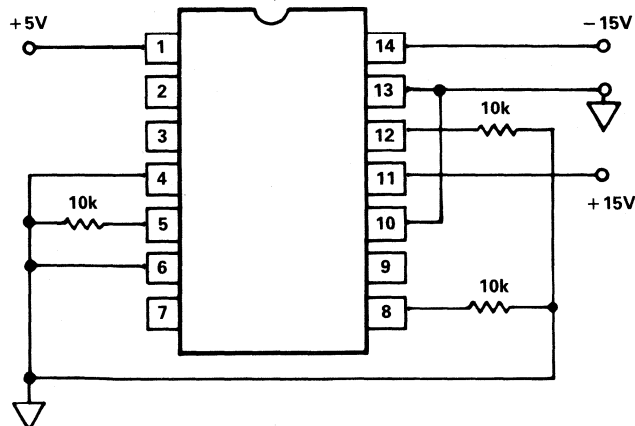


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the device requirements for a high speed, low drift FET input operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD380SH/883B
-2	AD381SH/883B
-3	AD382SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline:

Device	Package
-1	H-12A
-2	H-08B
-3	H-12A

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage	+18V
Negative Supply Voltage	-18V
Input Signal	$\pm V_S$
Differential Input Signal	$\pm 2 \times V_S$
Output Short Circuit Current to Ground (Device -1, 3)	80mA Continuous
Output Short Circuit Current to Ground (Device -2)	20mA Continuous
Junction Temperature	+175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= 70°C/W for H-12A
θ_{JA}	= 100°C/W for H-12A
θ_{JC}	= 40°C/W for H-08B
θ_{JA}	= 150°C/W for H-08B

AD380/AD381/AD382 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Open Loop Gain	A _{OL}	– 1	40,000			40,000	No Load	V/V min
		– 1	25,000			25,000	Note 2	V/V min
		– 2	100,000			100,000	Note 3	V/V min
		– 3	35,000			35,000	Note 2	V/V min
		– 3	150,000			150,000	Note 4	V/V min
Gain Bandwidth Product	GBP	– 1	200			200	f = 60kHz, C _C = 1pF	MHz min
			20			20	f = 60kHz, C _C = 10pF	
Slew Rate	SR	– 1	200			200	C _C = 1pF, 20V Swing	V/μs
		– 2, 3	20			20		
Output Voltage Swing	OVS	– 1	12			10	R _L = 200Ω	± V min
		– 2					R _L = 1kΩ	
		– 3					R _L = 200Ω	
Input Offset Voltage	V _{OS}	– 1	2.0	2.0				mV max
		– 2, 3	1.0	1.0				
Input Offset Voltage vs. Temperature	V _{OSTC}	– 1	50		50			± μV/°C max
		– 2, 3	10		10			
Output Short Circuit Current	I _{SC}	– 1	90			90	Short Circuit Current to Ground, Continuous	mA min
			220			220		mA max
		– 2	20			20		mA min
			220			220		mA max
		– 3	80			80		mA min
			220			220		mA max
Input Bias Current	I _{BIAS}	– 1	100			100	Either Input	pA max
		– 2	100			100		
		– 3	100			100		
Input Offset Current	I _{OS}	– 1, 2, 3	5					pA typ
Common-Mode Range	V _{DIF}	– 1, 2, 3	10					± V max
Common-Mode Rejection Ratio	CMRR	– 1	60			60	V _{INPUT} = ± 10V	dB min
		– 2, 3	80			80		
Operating Power Supply	V _{SS}	– 1	6					± V min
			20					± V max
		– 2, 3	5					± V min
			18					± V max
Quiescent Current	I _{SS}	– 1	17			17		± mA max
		– 2, 3	6			6		

NOTES

¹T_A = +25°C, V_S = ±15V, unless otherwise specified.

²V_{OUT} = +10V to 0V 200Ω load, V_{OUT} = 0V to –10V 200Ω load.

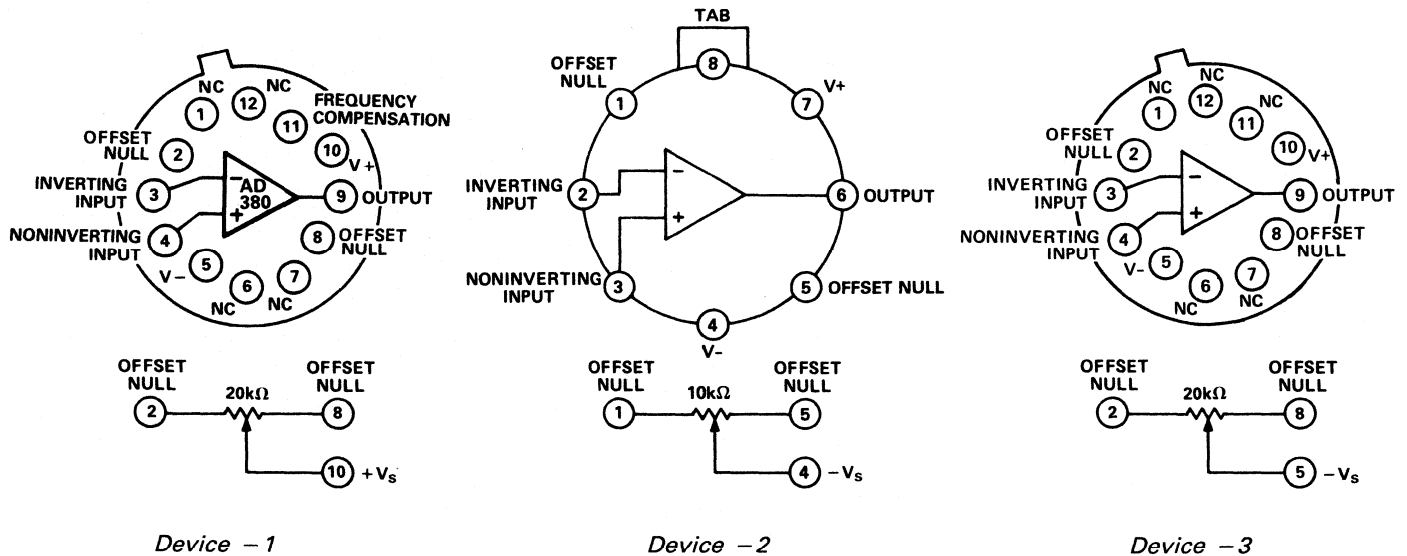
³V_{OUT} = +10V to 0V 2k load, V_{OUT} = 0V to –10V 2k load.

⁴V_{OUT} = +10V to 0V 10kΩ load, V_{OUT} = 0V to –10V 10kΩ load.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

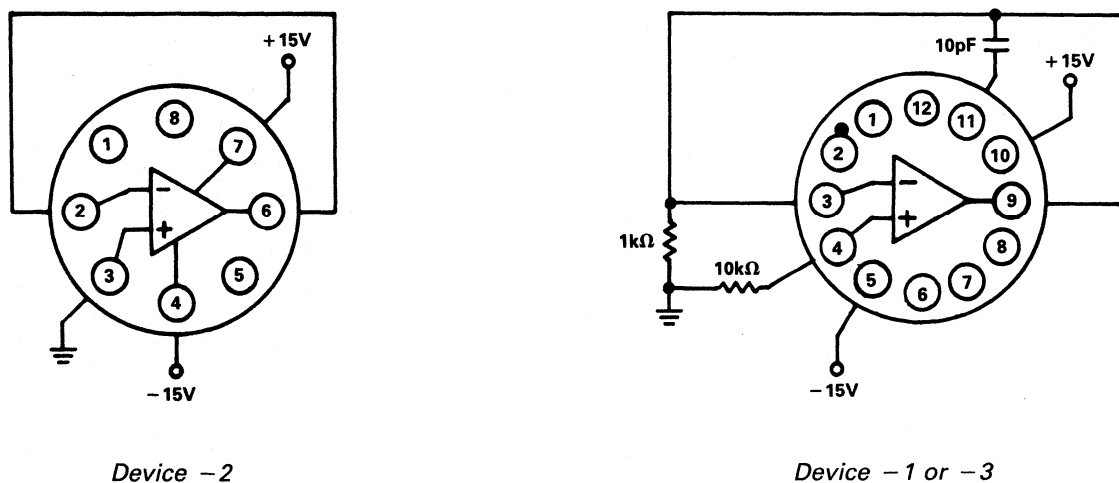


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a hybrid, 14-bit accurate track-and-hold amplifier including a differential amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD386TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-24B.

1.3 Absolute Maximum Ratings.

Positive Supply Voltage to Ground	+18 V
Negative Supply Voltage to Ground	-18 V
Analog Input to Ground	$-V_S$ to $+V_S$
T/H Input to Ground	-0.5 V to +16 V
Analog Output Short Circuit Duration	Indefinite
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA}	= 24°C/W
θ_{JC}	= 50°C/W

AD386 – SPECIFICATIONS

Test	Symbol	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
DIFFERENTIAL AMPLIFIER							
Input Voltage Range	V_{INA}	10					$\pm V$ min
Common Mode Voltage	V_{CMA}	10					$\pm V$ min
Input Resistance Signal	R_{INSA}	5					k Ω max
GND Sense	R_{INGA}	10					
Offset Voltage	V_{OSA}		2			Note 2	mV max
Offset Voltage Drift	V_{OSDA}			30			$\mu V/^{\circ}C$ max
Common Mode Rejection Ratio	$CMRR_A$		80			$V_{CM} = \pm 10$	dB min
Power Supply Rejection Ratio	$PSRR_A$		76	76		Note 3	dB min
Gain	G_A	-1					V/V min
Gain Error	G_{EA}		0.02				% max
Gain Error Drift	G_{EDA}			5			ppm/ $^{\circ}C$ max
Gain Linearity	G_{LA}		0.003				% max
Gain Linearity Drift	G_{LDA}			0.05			ppm/ $^{\circ}C$ max
Noise	N_A	45				ENBW = 1.8 M	μV rms max
Small Signal Bandwidth	BW_A	6					MHz min
Slew Rate	SR_A	65					V/ μs min
Settling Time 10 V Step to 1/2 LSB14	T_{SET1A}	1.5	1.5			Note 4	μs max
20 V Step to 1/2 LSB14	T_{SET2A}						
Output Voltage	V_{OUTA}			10		$R_I > 3.5 k$	$\pm V$ min
Output Current	I_{OUTA}	15				Short Circuit	mA min
Positive Power Supply	$+V_{SA}$	+5					Volts min
		+18					Volts max
Negative Power Supply	$-V_{SA}$	-5					Volts min
		-18					Volts max
Positive Supply Current	$+I_{SA}$			+5		$V_S = \text{Nom}$	mA max
Negative Supply Current	$-I_{SA}$			-5		$V_S = \text{Nom}$	mA max
TRACK AND HOLD							
Input Voltage Range	V_{INT}	10					$\pm V$ min
Input Resistance	R_{INT}	5					k Ω min
Offset Voltage	V_{OST}		2				mV max
Offset Voltage Drift	V_{OSDT}			30			$\mu V/^{\circ}C$ max
Power Supply Rejection Ratio	$PSRR_T$		76	76		Note 3	dB min
Gain	G_T	-1					V/V min
Gain Error	G_{ET}		0.02				% max
Gain Error Drift	G_{EDT}			5			ppm/ $^{\circ}C$ max
Gain Linearity	G_{LT}		0.003				% max
Gain Linearity Drift	G_{LDT}			0.05			ppm/ $^{\circ}C$ max
Small Signal Bandwidth	BW_T	2					MHz min
Slew Rate	SR_T	15					V/ μs min
Pedestal + Offset	PO		1.5	7.5			mV max
Pedestal Linearity	P_L	0.003					% max

Table 1. (Continued on next page)

REV. A

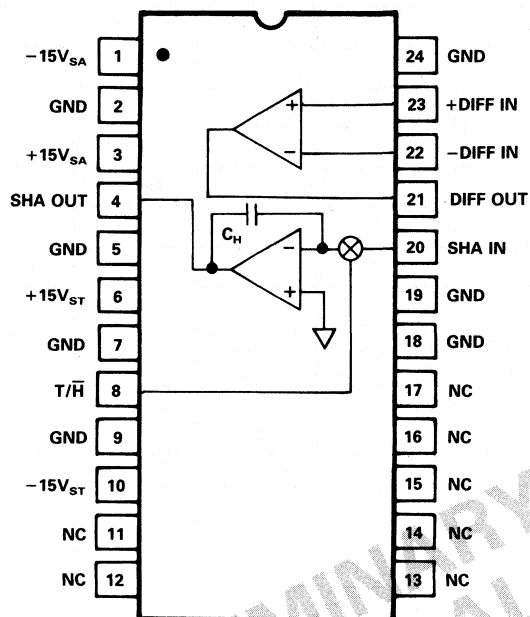
Test	Symbol	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Aperture Delay	T _{APD}	12					ns max
Aperture Jitter	T _{APJ}	40					ps max
Transient Settling, to 14 Bits	T _{TSET}	500				Note 4	ns max
Droop Rate	D _{RP}		100				mV/s max
Droop Rate Over Temp	D _{RPD}			18			V/s max
Feedthrough	F _{TH}	-94	-94				dB max
Noise	N	50				ENBW = 1.7 M	μV rms max
Acquisition Time 10 V Step to 1/2 LSB14	T _{ACQT1}	3.6	3.6			Note 4	μs max
20 V Step to 1/2 LSB14	T _{ACQT2}	4.5	4.5				
Input Voltage Logic High	V _{IH}		2.4	2.4			V min
Logic Low	V _{IL}		0.8	0.8			V max
Input Current V _{IH} = 2.4	I _{IH}		10	10			±μA max
V _{IL} = 0.8	I _{IL}		10	10			
Output Voltage	V _{OUTT}			10		RI > 3.5 k	±V min
Output Current	I _{OUTT}	15				Short Circuit	mA min
Positive Power Supply	+V _{ST}	+8					Volts min
		+18					Volts max
Negative Power Supply	-V _{ST}	-8					Volts min
		-18					Volts max
Positive Supply Current	+I _{ST}		+12	+12		V _S = Nom	mA max
Negative Supply Current	-I _{ST}		-6	-6		V _S = Nom	mA max
SYSTEM							
Gain Linearity	G _{LS}	0.003				Note 5	% max
Acquisition Time 20 V Step to 1/2 LSB14	T _{ACQS}	4.8				Note 5	μs max

NOTES

¹All specifications with +V_S = 15 V, -V_S = -15 V unless otherwise noted.²After 5 minute warmup.³Test Conditions: +V_S = +15, -V_S = -16 to -14 and +V_S = +14 to +16, -V_S = -15 V.⁴R_{LOAD} = 5 kΩ, C_{LOAD} = 10 pF, settling measured to 1/2 LSB @ output.⁵Calculated by adding the respective individual measurements for the Differential Amplifier and the Track-and-Hold.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

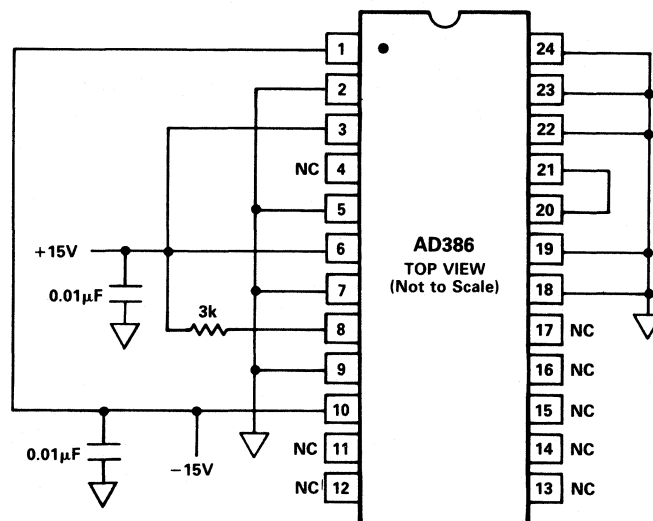


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life/Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the device requirements for a hybrid quad 12-bit voltage output D/A converter with double buffered latches.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD390SD/883B
- 2	AD390TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_S$ to DGND	0 to +18V
$-V_S$ to DGND	0 to -18V
Digital Inputs (Pins 1-12, 23-28) to DGND	-1.0V to +7V
Ref In to DGND	$\pm V_S$
AGND to DGND	$\pm 0.6\text{V}$
Analog Outputs (Pins 16, 18-21)	Infinite
Short to AGND or DGND, Momentary Shorts to $\pm V_S$	
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 8^\circ\text{C/W}$
 $\theta_{JA} = 25^\circ\text{C/W}$

AD390 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C (–55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Data Input Voltage High End Point Electrical	V _{IH}	–1, 2 –1, 2	2.0 (2.0) 5.5 (5.5)	2.0		2.0	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 23–28.	V min V max V min
Data Input Voltage Low End Point Electrical	V _{IL}	–1, 2 –1, 2	0.0 (0.0) 0.8 (0.8)	0.8		0.8	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 23–28.	V min V max V max
Input Current High End Point Electrical	I _{IH}	–1, 2 –1, 2	1200 (1200)	1200			Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 23–28, Except for Pin 24 Which is 3X.	μA max
Input Current Low End Point Electrical	I _{IL}	–1, 2 –1, 2	400 (400)	400				μA max
Output Voltage Range	V _{OUT}	–1, 2	10 (10) 10 (10)			10 10		+ V max – V min
Output Current Range	I _{OR}	–1, 2	5 (5)				@ ±10V Output	mA min
Gain Error End Point Electrical	A _E	–1 –2 –1, 2	0.1 0.05	0.1 0.2		0.05	With External + 10,000 Ref	± % FSR max ²
Gain Error Temperature Coefficient	TC _{AE}	–1 –2	(40) (20)				With Internal Reference	± ppm/°C max
		–1 –2	(10) (5)		10 5		With External Reference	± ppm/°C max
Offset Error End Point Electrical	V _{OS}	–1 –2 –1, 2	0.05 0.025	0.05 0.1		0.025		± % FSR max
Bipolar Zero Temperature Coefficient	TCB _{PZ}	–1 –2	(10) (5)		10 5		V _{BPFS} = ±10V	± ppm/°C max
Differential Linearity ³ Error End Point Electrical	DLE	–1 –2 –1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Linearity Error ⁴ End Point Electrical	LE	–1 –2 –1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Linearity Error Temperature Coefficient	TC _{LE}	–1 –2	(3/4) (1/2)		3/4 1/2			± LSB max
Positive Summation Error End Point Electrical	E _{PE}	–1 –2 –1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Negative Summation Error End Point Electrical	E _{NE}	–1 –2 –1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Reference Output	REF _{OUT}	–1, 2	9.997 10.003	9.997 10.003			R _L = 6.8kΩ	V min V max
Power Supply Voltages ³	V _S	–1, 2 –1, 2	13.5 16.5					± V min ± V max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C (−55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Power Supply Currents	I_{EE} I_{CC}	−1, 2	100 35	100 35	120 35		No Load	− mA max + mA max
Power Supply Gain Sensitivity Delta Gain/ Delta V_S (+ V_S and − V_S)	PSRR	−1, 2	0.0067			0.0067	Input Bits = 1111 1111 1111	± % FS/%
Timing Specifications Chip Select Pulse Width	t_{AW}	−1 −2	100				See Figure 2	ns min
Address Select Low Time	t_{WP}	−1 −2	100				See Figure 2	ns min
Data Valid Before $\overline{A0}$ Rising Edge	t_{OW}	−1 −2	50				See Figure 2	ns min
Data Valid After $\overline{A0}$ Rising Edge	t_{DH}	−1 −2	10				See Figure 2	ns min
Chip Select Valid Before $\overline{A1}$ Low	t_{AS}	−1 −2	0				See Figure 2	ns min
Output Voltage Settling Time	t_{SETT}	−1 −2	8				See Figure 2	μs max

NOTES

¹ $T_A = +25^\circ\text{C}$ and $\pm V_S = \pm 15\text{V}$ unless otherwise specified.

AD390 can be used with supplies as low as $\pm 11.4\text{V}$ (see AD390 commercial data sheet).

²FSR means Full-Scale Range and is equal to 20V for a $\pm 10\text{V}$ bipolar range.

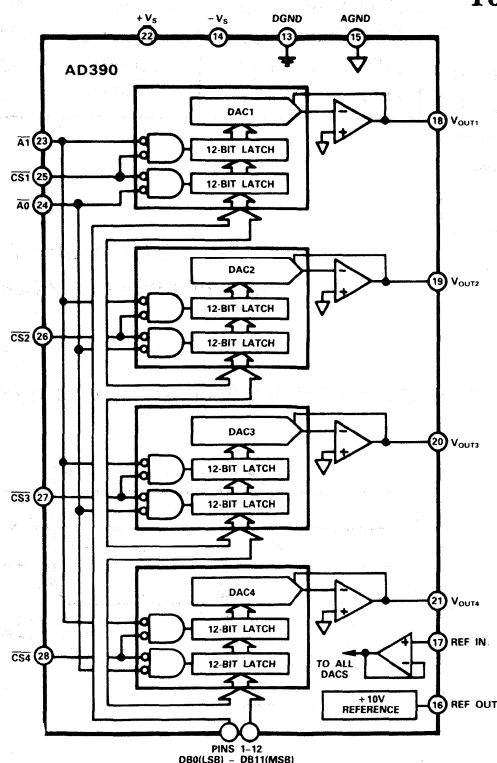
³Monotonicity is tested for over the full military temperature.

⁴Integral Nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.

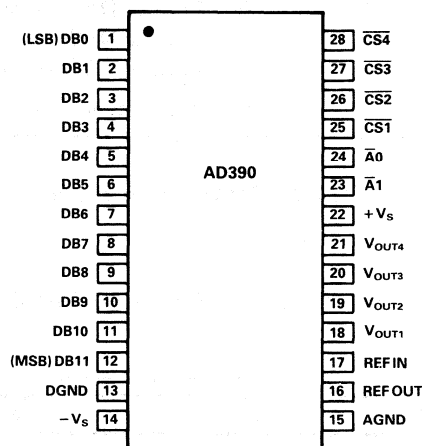
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



DH-28 Package



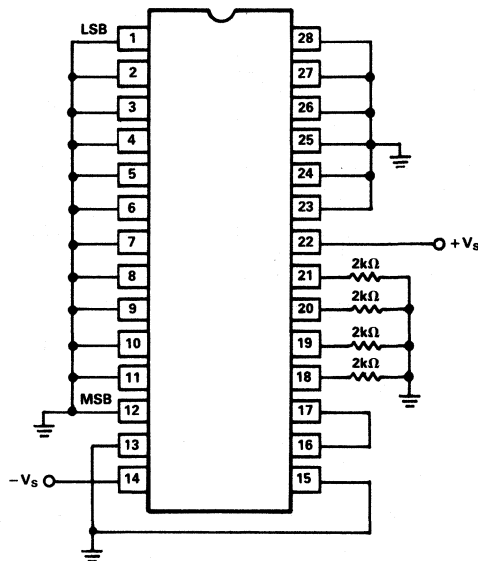
AD390

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (1).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



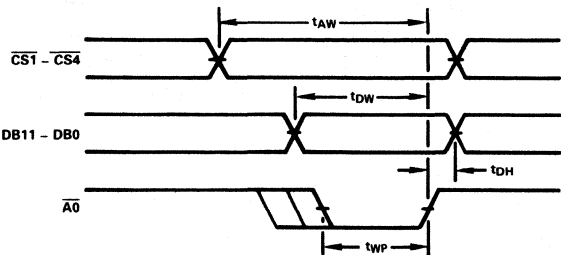
CS1	CS2	CS3	CS4	A1	A0	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC 1
1	0	1	1	1	0	Enable 1st rank of DAC 2
1	1	0	1	1	0	Enable 1st rank of DAC 3
1	1	1	0	1	0	Enable 1st rank of DAC 4
0	1	1	1	0	1	Load DAC 1 second rank from first rank
1	0	1	1	0	1	Load DAC 2 second rank from first rank
1	1	0	1	0	1	Load DAC 3 second rank from first rank
1	1	1	0	0	1	Load DAC 4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table 2. AD390 Truth Table

Digital Input Code	Analog Output Voltage	
0000 0000 0000	- 10.000V	- Full Scale
0100 0000 0000	- 5.000V	- 1/2 Scale
1000 0000 0000	0.000V	Zero
1000 0000 0001	+ 4.88mV	+ 1LSB
1100 0000 0000	+ 5.000V	+ 1/2 Scale
1111 1111 1111	+ 9.9951V	+ Full Scale - 1LSB

Table 3. AD390 Analog Output vs. Digital Input ($\pm V$ Scale)

Write Cycle #1 (Load First Rank from Data Bus; $\overline{A1} = 1$)



Write Cycle #2 (Load Second Rank from First Rank; $\overline{A0} = 1$)

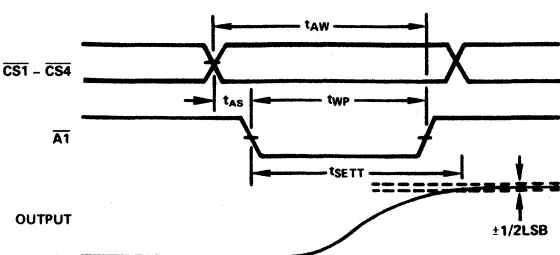


Figure 1. Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a hybrid quad 12-bit voltage output CMOS D/A converter with individual DAC reference inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD394SD/883B
- 2	AD394TD/883B
- 3	AD395SD/883B
- 4	AD395TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_S$ to DGND		-0.3V to +17V
$-V_S$ to DGND		+0.3V to -17V
Digital Inputs (Pins 1-16) to DGND		-0.3V to +7V
V_{REFIN} to DGND		$\pm 25\text{V}$
AGND to DGND		-0.3V to $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)		Indefinite
	Short to AGND or DGND Momentary Short to $\pm V_S$	
Operating Temperature Range (Ambient)		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10secs)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 8^\circ\text{C/W typ}$
 $\theta_{JA} = 25^\circ\text{C/W typ}$

AD394/AD395 — SPECIFICATIONS

Test	Symbol	Device	Design Limit (@ 25°C/(−55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Data Input Voltage High End Point Electrical	V _{IH}	−1, 2, 3, 4 −1, 2, 3, 4	2.4/(2.4) 5.5/(5.5)	2.4		2.4	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 13–16.	+ V min + V max + V min
Data Input Voltage Low End Point Electrical	V _{IL}	−1, 2, 3, 4 −1, 2, 3, 4	0.0/(0.0) 0.8/(0.8)	0.8		0.8	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 13–16.	+ V min + V max + V min
Input Current High	I _{IH}	−1, 2, 3, 4	40/(40)			40	V _{IN} = 0V or +5V	± μA max
Input Current Low End Point Electrical	I _{IL} I _{IH} , I _{IL}	−1, 2, 3, 4 −1, 2, 3, 4	40/(40)	40		40	V _{IN} = 0V or +5V	± μA max
Output Voltage Range ²	V _{OUT}	−1, 2, 3, 4	11/(11) 11/(11)			10 10	AD394 Output Voltage Equals −REFIN to +REFIN AD395 Output Equals 0V to −(V _{REFIN}) R _L = 2kΩ	− V min + V max
Output Current Range	I _{OR}	−1, 2, 3, 4	5/(5)					± mA min
Gain Error End Point Electrical	A _E	−1, 3 −2, 4 −1, 2, 3, 4	0.1 0.05	0.1 0.2		0.05	External + 10.000V REF Bit Code = 1111 1111 1111	± %FSR ³ max
Gain Error Temperature Coefficient	TC _{AE}	−1, 3 −2, 4	/(10) /(5)		10 5		External + 10.000V REF Bit Code = 1111 1111 1111	± ppm/°C max
Offset Error End Point Electrical	V _{OS}	−1, 3 −2, 4 −1, 2, 3, 4	0.05 0.025	0.05 0.1		0.025	External + 10.000V REF Bit Code = 0000 0000 0000	± %FSR max
Offset Temperature Coefficient	TC _{BPZ}	−1, 3 −2, 4	/(10) /(5)		10 5		External + 10.000V REF Bit Code = 0000 0000 0000	± ppm/°C max
Differential Linearity Error ⁴ End Point Electrical	DLE	−1, 3 −2, 4 −1, 2, 3, 4	3/4 1/2	3/4 1.5	1 1	1/2		± LSB max
Linearity Error ⁵ End Point Electrical	TC _{LE}	−1, 3 −2, 4 −1, 2, 3, 4	3/4 1/2	3/4 1/2 1	3/4 1/2			± LSB max
Power Supply Voltages ²	V _S	−1, 2, 3, 4 −1, 2, 3, 4	13.5/(13.5) 16.5/(16.5)	15 15	15 15			− V min V max
Power Supply Currents	I _{CC} I _{EE}	−1, 2, 3, 4	28/(35) 22/(22)			28 22	Data Input Bits = 1111 1111 1111 R _L = ∞ Data Input Bits = 1111 1111 1111 R _L = ∞	− mA max + mA max
Power Supply Gain Sensitivity Δ Gain/ ΔV _S (+ V _S and − V _S)	PSRR	−1, 2, 3, 4	0.006			0.006	Input Bits = 1111 1111 1111 V _S = ±15V ±10%	± %FS/%
Timing Specifications Chip Select	t _{CS}	−1, 2, 3, 4	170				See Figure 1	ns min
Data Access Time	t _{DA}	−1, 2, 3, 4	0				See Figure 1	ns min
Data Setup Time	t _{DS}	−1, 2, 3, 4	150				See Figure 1	ns min
Data Hold Time	t _{DH}	−1, 2, 3, 4	5				See Figure 1	ns min

NOTES

¹T_A = +25°C and ±V_S = ±15V, V_{REFIN} = +10V for AD394, V_{REFIN} = −10V for AD395.

²Both the AD394 and AD395 can be used with supplies as low as ±11.4V. See page 6, Figure 10 of product data sheet.

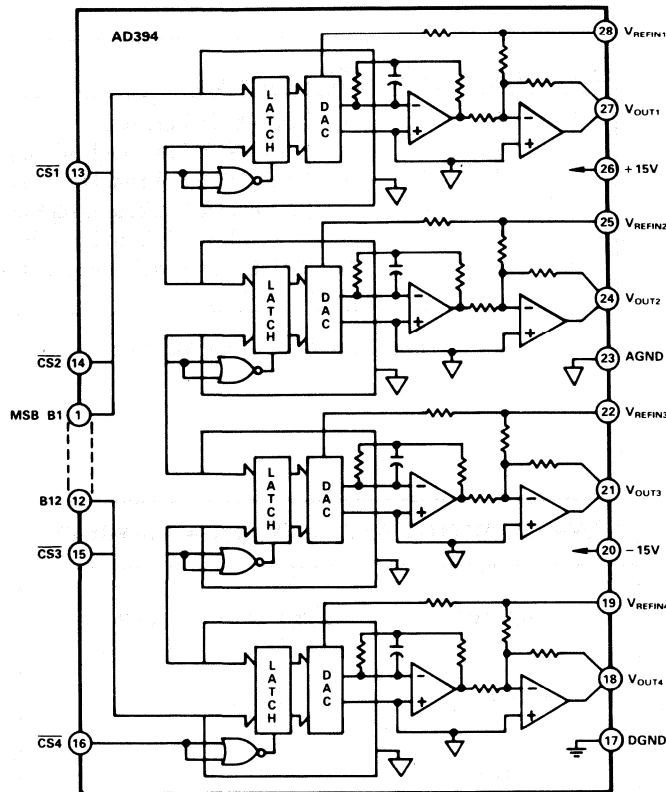
³FSR means Full-Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.

⁴Monotonicity is tested for over the full military temperature.

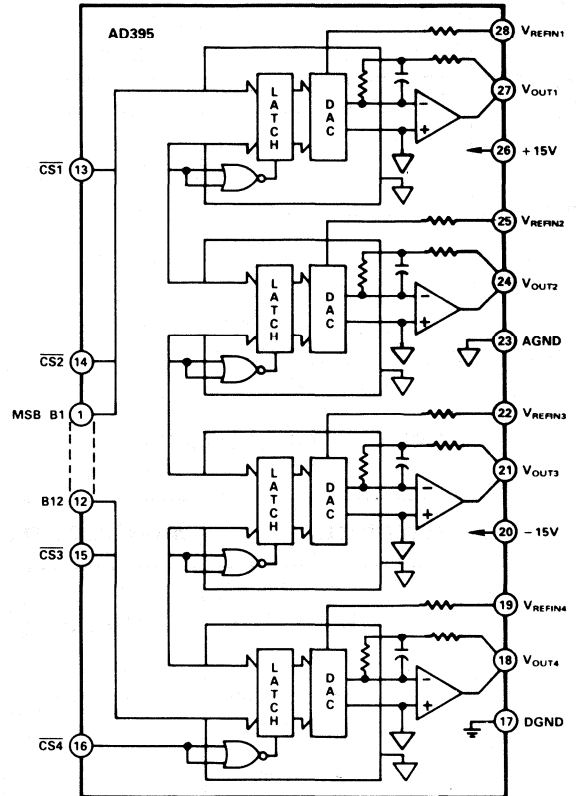
⁵Integral nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



AD394 (Bipolar) Functional Block Diagram



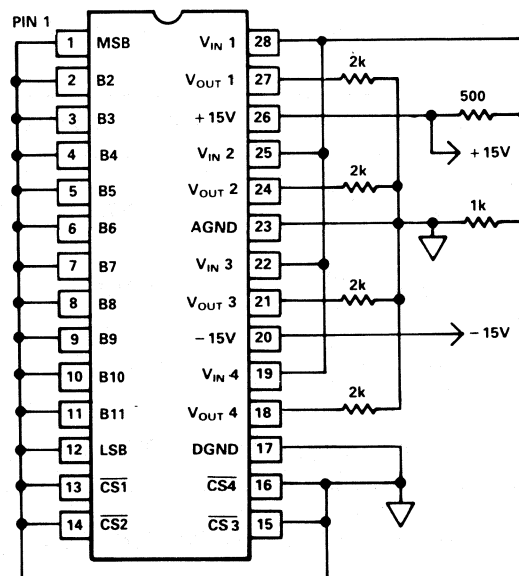
AD395 (Unipolar) Functional Block Diagram

3.2.4 Microcircuit Technology Group.

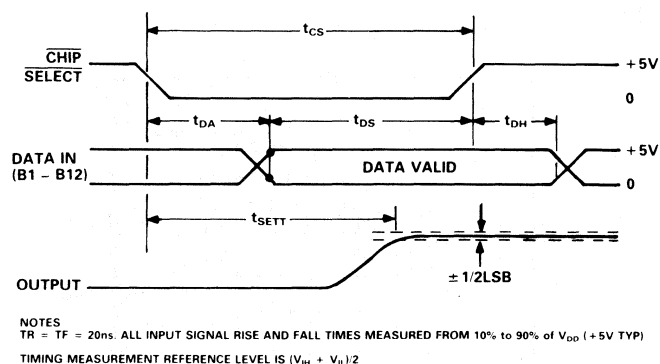
This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD394/AD395



WRITE MODE
 CS LOW, DAC RESPONDS TO
 DATA BUS (db0-db11) INPUTS

HOLD MODE
 CS HIGH, DATA BUS (db0-db11) IS
 LOCKED OUT; DAC HOLDS LAST DATA
 PRESENT WHEN CS ASSUMED
 HIGH STATE.

MODE SELECTION

CS1	CS2	CS3	CS4	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table 2. DAC Select Matrix

Figure 1. Timing Diagram

DATA INPUT	ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE $V_{REFIN} = +10\text{ VOLTS}$
1111 1111 1111	$+1 \cdot (V_{REFIN}) \left\{ \frac{2047}{2048} \right\}$	+9.9951V + FULL SCALE - 1LSB
1100 0000 0000	$+1 \cdot (V_{REFIN}) \left\{ \frac{1024}{2048} \right\}$	+5.000V + 1/2 SCALE
1000 0000 0001	$+1 \cdot (V_{REFIN}) \left\{ \frac{1}{2048} \right\}$	+4.88mV + 1LSB
1000 0000 0000	$+1 \cdot (V_{REFIN}) \left\{ \frac{0}{2048} \right\}$	+0.000V ZERO
0111 1111 1111	$-1 \cdot (V_{REFIN}) \left\{ \frac{1}{2048} \right\}$	-4.88mV - 1LSB
0100 0000 0000	$-1 \cdot (V_{REFIN}) \left\{ \frac{1024}{2048} \right\}$	-5.000V - 1/2 SCALE
0000 0000 0000	$-1 \cdot (V_{REFIN}) \left\{ \frac{2048}{2048} \right\}$	-10.000V - FULL SCALE

Table 3. AD394 Bipolar Code Table

DATA INPUT	ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE $V_{REFIN} = +10\text{ VOLTS}$
1111 1111 1111	$-1 \cdot (V_{REFIN}) \left\{ \frac{4095}{4096} \right\}$	-9.9976V - FULL SCALE - 1LSB
1000 0000 0000	$-1 \cdot (V_{REFIN}) \left\{ \frac{2048}{4096} \right\}$	-5.000V - 1/2 SCALE
0000 0000 0001	$-1 \cdot (V_{REFIN}) \left\{ \frac{1}{4096} \right\}$	-2.44mV - 1LSB
0000 0000 0000	$-1 \cdot (V_{REFIN}) \left\{ \frac{0}{4096} \right\}$	0.000V ZERO

Table 4. AD395 Unipolar Code Table

1.1 Scope.

This specification covers the detail requirements for a hybrid quad 14-bit voltage output CMOS D/A converter with individual DAC reference inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD396SD/883B
– 2	AD396TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_S$ to DGND	– 0.3V to +17V
$-V_S$ to DGND	+ 0.3V to – 17V
Digital Inputs (Pins 1–16) to DGND	– 0.3V to +7V
V_{REFIN} to DGND	$\pm 25\text{V}$
AGND to DGND	– 0.3V, $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)	Indefinite
	Short to AGND or DGND Momentary Short to $\pm V_S$
Operating Temperature Range (Ambient)	– 55°C to +125°C
Storage Temperature	– 65°C to +150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 8^\circ\text{C/W}$ typ
 $\theta_{JA} = 25^\circ\text{C/W}$ typ

AD396 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Data Input Voltage High	V _{IH}	– 1, 2	2.4 5.5			2.4	Test Limits Apply to Pins 1–8. Design Limits Apply to Pins 9–16.	+ V min
End Point Electrical		– 1, 2		2.4				+ V max
Data Input Voltage Low	V _{IL}	– 1, 2	0.0 0.8			0.8		+ V min
End Point Electrical		– 1, 2		0.8				+ V max
Input Current High	I _{IH}	– 1, 2	40			40	V _{IN} = 0 or +5V	± µA max
Input Current Low	I _{IL}	– 1, 2	40			40	V _{IN} = 0 or +5V	± µA max
End Point Electrical				40				
Output Voltage Range	V _{OUT}	– 1, 2	11 11			10 10	Output Voltage Equals – REFIN to + REFIN	– V min
								– V max
Output Current Range	I _{OR}	– 1, 2	5					± mA min
Gain Error	A _E	– 1 – 2	0.1 0.05	0.1		0.05	External + 10.000V REF Code = 1111 1111 1111 11	± FSR max
End Point Electrical		– 1, 2		0.2				
Gain Error Temp Co.	dA _E /dT	– 1 – 2	10 5		10	5	External + 10.000V REF Code = 1111 1111 1111 11	± ppm/°C max
Offset Error	V _{OS}	– 1 – 2	0.05 0.025	0.05		0.025	External + 10.000V REF Code = 0000 0000 0000 00	± FSR max
End Point Electrical		– 1, 2		0.1				
Offset Temp Co.	dV _{OS} /dT	– 1 – 2	10 5		10	5	External + 10.000V REF Code = 0000 0000 0000 00	± ppm/°C max
Differential Linearity Error ²	DLE	– 1, 2	1	1	1			± LSB max
End Point Electrical				1.5				
Linearity Error	LE	– 1 – 2	2 1	2 1	4 2			± LSB max
End Point Electrical		– 1, 2		2				
Power Supply Voltages ³	V _S	– 1, 2	13.5 16.5	15 15	15 15			– V min
								+ V max
Power Supply Currents	I _{CC}	– 1, 2	28			28	Code = 1111 1111 1111 11 R1 = Infinity	– mA max
	I _{EE}	– 1, 2	22			22	Code = 0000 0000 0000 00 R1 = Infinity	+ mA max
Power Supply Gain Sensitivity	PSRR	– 1, 2	0.006			0.006	Code = 1111 1111 1111 11 V _S = ± 15V, ± 10%	± %FS/%
Timing Specifications								
Write Pulse Width	t ₇	– 1, 2	240				See Figure 1	ns min
Data Setup Time	t ₃	– 1, 2	140				See Figure 1	ns min
Data Hold Time	t ₄	– 1, 2	30				See Figure 1	ns min

NOTES

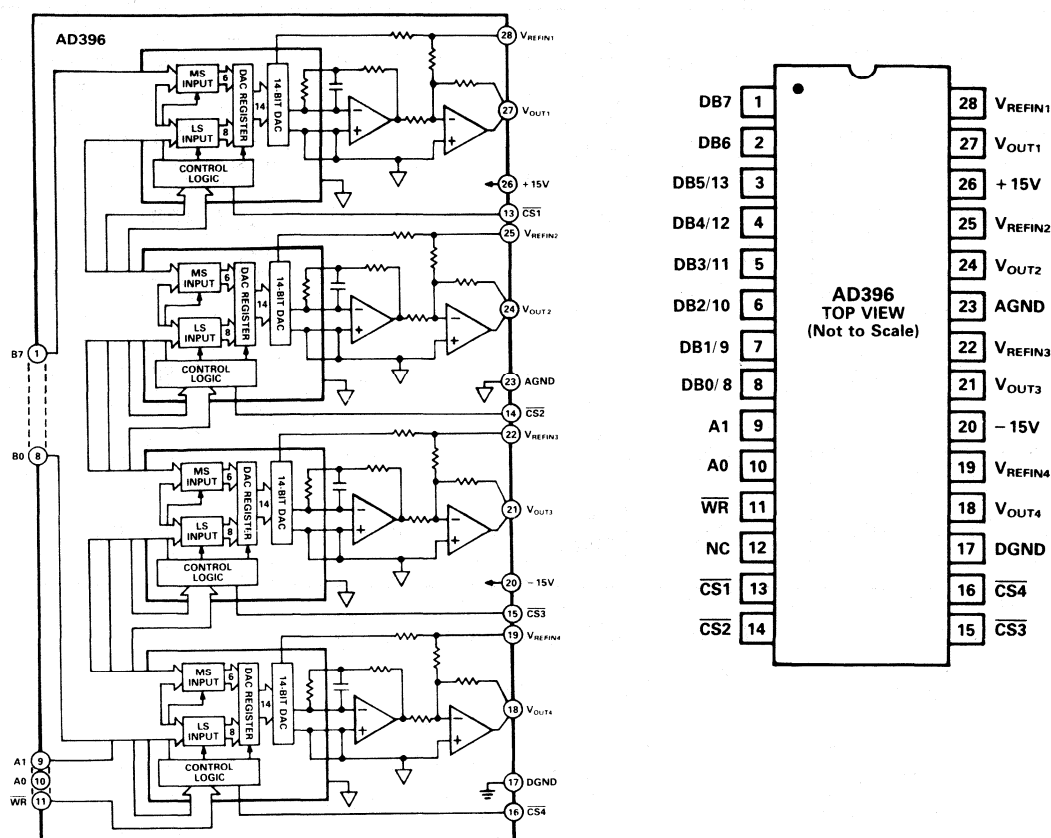
¹V_{CC} = ± 15V, V_{DD} = + 5V, T_A = + 25°C unless otherwise noted.

²Monotonicity is tested over – 55°C to + 125°C.

³The AD396 can be used with supplies as low as ± 11.4V. See AD396 product data sheet.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

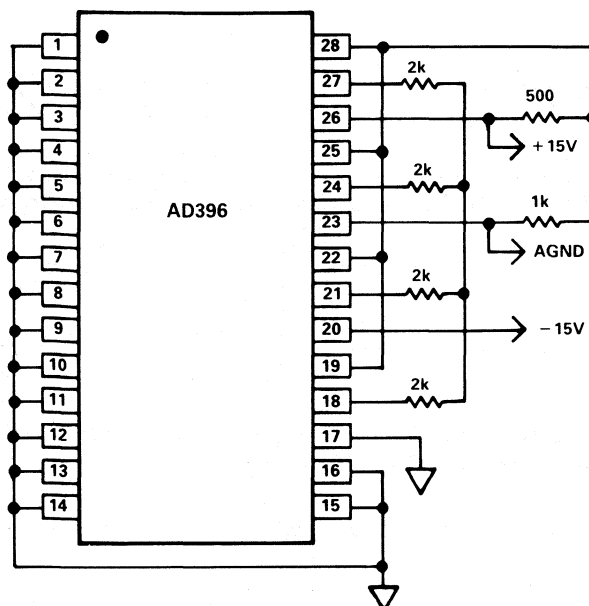


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE $V_{REFIN} = +10 \text{ VOLTS}$	
1111	1111	1111 11	$+1 \cdot (V_{REFIN}) \left\{ \frac{8191}{8192} \right\}$	+ 9.9988V	+ FULL SCALE - 1LSB
1100	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{ \frac{4096}{8192} \right\}$	+ 5.000V	+ 1/2 SCALE
1000	0000	0000 01	$+1 \cdot (V_{REFIN}) \left\{ \frac{1}{8192} \right\}$	+ 1.22mV	+ 1LSB
1000	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{ \frac{0}{8192} \right\}$	+ 0.000V	ZERO
0111	1111	1111 11	$-1 \cdot (V_{REFIN}) \left\{ \frac{1}{8192} \right\}$	- 1.22mV	- 1LSB
0100	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{ \frac{4096}{8192} \right\}$	- 5.000V	- 1/2 SCALE
0000	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{ \frac{8192}{8192} \right\}$	- 10.000V	- FULL SCALE

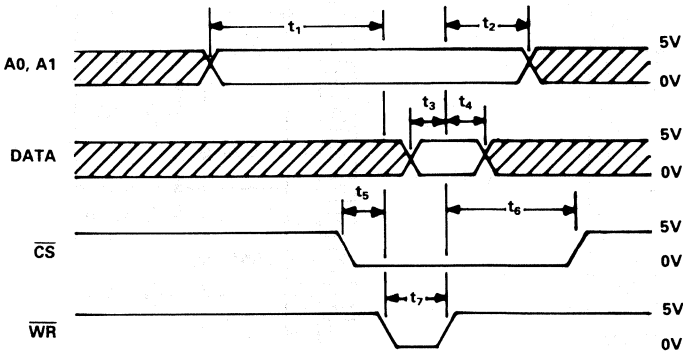
Table 2. AD396 Bipolar Code Table

$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X ¹	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus ²
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

Table 3. Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Register
1	0	1	1	Load DAC 2 From Data Register
1	1	0	1	Load DAC 3 From Data Register
1	1	1	0	Load DAC 4 From Data Register
0	0	0	0	All DACs Simultaneously Loaded

Table 4. DAC Select Matrix



- NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF + 5V. $t_r = t_f = 20\text{ns}$.
 2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD396 Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a hybrid, differential input, precision, uncommitted gain, instrumentation amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD522SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-14B

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage (Pin 8)		+ 20V
Negative Supply Voltage (Pin 5)		– 20V
Input Signal (Pins 1, 3, 13)		$\pm V_S$
Differential Input Signal (Pin 1 to 3)		$\pm (2 \times V_S)$
Short Circuit to Ground (Pin 7)		Continuous
Lead Temperature (Soldering 10sec)		+ 300°C
Storage Temperature Range		– 65°C to + 150°C
Junction Temperature		+ 175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 7^\circ\text{C}/\text{W}$
 $\theta_{JA} = 40^\circ\text{C}/\text{W}$

AD522 – SPECIFICATIONS

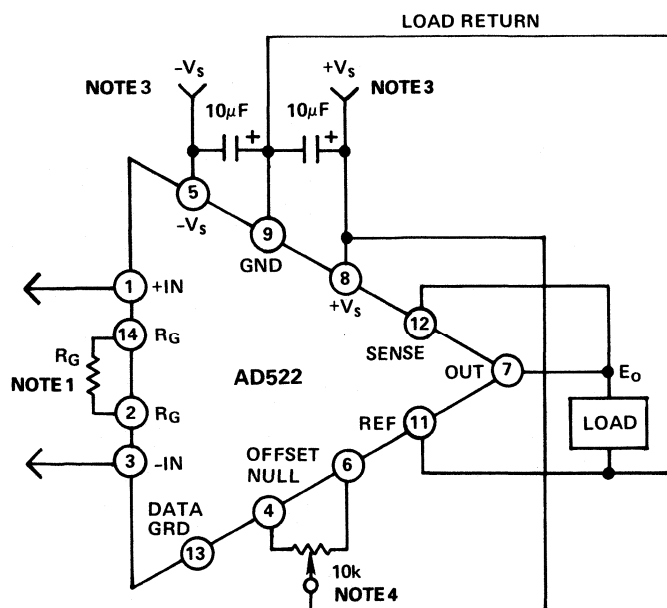
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
+ Supply Currents	I _{CC}	– 1	8			8		+ mA max
–	I _{EE}	– 1	8			8		– mA max
Input Offset Voltage (RTI)	V _{OS}	– 1	200	200			G = 1	± μV max
		– 1	200	200			G = 1001	± μV max
Input Offset Voltage Drift Over Temperature (RTI)	TCV _{OS}	– 1	100		100		G = 1 (RTI)	± μV/°C max
			6		6		G = 1001 (RTI)	
Data Guard Impedance	Z _{DG}		3				0.5mA Current Source	kΩ min
Input Bias Current	I _B	– 1	25			25		± nA max
Input Offset Current	I _{OS}	– 1	20			20		± nA max
Common-Mode Rejection	CMRR	– 1	80			80	G = 1, ± 10V dc Both Inputs	dB min
		– 1	100			100	G = 101, ± 10V dc Both Inputs	dB min
		– 1	110			110	G = 1001, ± 10V dc Both Inputs	dB min
Gain Equation Error	A _{EE}	– 1	5			5	G = 1, V _{IN} = +10V, – 10V	mV max
		– 1	0.2			0.2	G = 101, V _{IN} = +99mV, – 99mV	± % max
Gain Nonlinearity	A _{NL}	– 1	0.001				G = 1	± % max
			0.005				G = 101	
Gain vs. Temperature	TC _{AE}	– 1	2				G = 1	ppm/°C max
			50				G = 1001	
Small Signal Response – 3dB	BW	– 1	200				G = 1	kHz min
			2.0				G = 101	
Full Power Bandwidth	FP _{BW}	– 1	1.0					kHz min
Slew Rate	t _{SR}	– 1	0.1					V/μs min
Input Currents vs Temperature	TCL _B	– 1	300					pA/°C max
	TCL _{OS}	– 1	300					
Input Impedance	Z _{OFS}	– 1	10					MΩ min
	Z _{CM}	– 1	10					MΩ min
Common-Mode Voltage Range	VCM	– 1	10					± V max
Voltage Noise, RTI (0.1 to 100Hz p-p)	EN	– 1	0.5				G = 1	mV pk-pk
		– 1	1.5				G = 1001	

NOTE

¹T_A = +25°C and ±V_S = ±15V, V_{DD} = +5V unless otherwise specified.

Table 1.

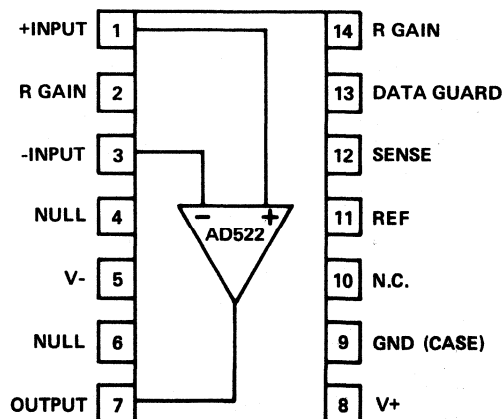
3.2.1 Functional Block Diagram and Terminal Assignments.



$$E_o = \left(1 + \frac{200k}{R_G}\right) \left[(E_1 - E_2) - \left(\frac{E_1 + E_2}{2} \times \frac{1}{CMR}\right) \right]$$

DH-14B Package

Top View



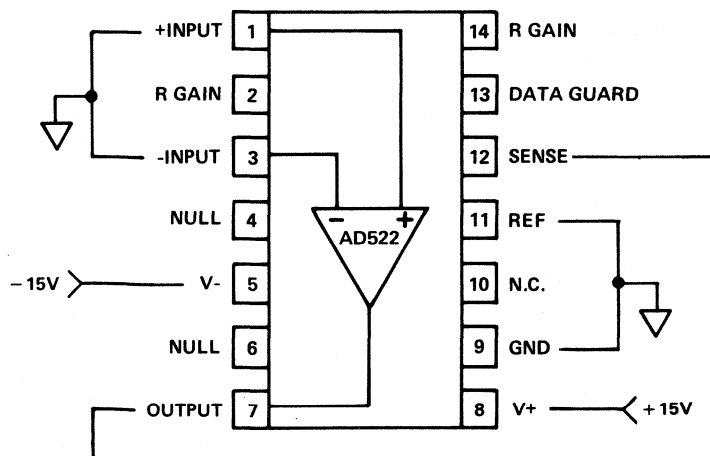
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

Top View



and the other side of the river, the water is very shallow.

and the other side of the river,

and the other side of the river,

and the other side of the river,

and the other side of the river,

and the other side of the river,

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1.1 Scope.

This specification covers the detail requirements for a hybrid 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD572SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32C.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V dc}$
Logic Supply Voltage	$+ 7\text{V dc}$
Analog Inputs (Pins 24, 25)	$\pm 25\text{V dc}$
Digital Inputs	$+ 5.5\text{V dc}$
Junction Temperature	$+ 175^\circ\text{C}$
Storage Temperature Range	$- 65^\circ\text{C to } + 150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+ 300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 7^\circ\text{C/W}$
$\theta_{JA} = 35^\circ\text{C/W}$

AD572 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Analog Input Voltage Ranges	V _{IN}	– 1	± 2.5, ± 5, ± 10 0 to 5 0 to 10					V
Output High Drive	V _{OH}	– 1	2.4			2.4	@ 80µA	V min
Output Low Drive	V _{OL}	– 1	0.4			0.4	@ 3.2mA	V max
Input Impedance			2.5			2.5	10V Span	kΩ min
Buffer Amp Bias Current	I _B	– 1	150			150		± nA max
Buffer Amp Offset Error	I _{OSE}	– 1	15			15		± mV max
Buffer Amp Common-Mode Rejection	CMRR	– 1	60			60		dB min
Buffer Amp Settling Time	t _{SL}	– 1	2				T _A = +25°C To ± 0.01% of FSR for 20V Step	µs
Reference Voltage Error	V _{REF}	– 1	20	20			10V Nominal	± mV max
Reference Voltage Drift	TCV _{REF}	– 1	20		20		± 5V Input Range	± ppm/°C max
Full Scale Calibration Error	A _E	– 1	0.25	0.25			0 to 10V Input Range Unipolar and Bipolar Mode	± % FSR max
Unipolar Offset Error	V _{OS}	– 1	0.2	0.2			0 to 10V Input Range	± % FSR max
Unipolar Offset Drift	TCV _{OS}	– 1	5		5		0 to 10V Input Range	± ppm/°C max
Bipolar Zero Error	B _{PZE}	– 1	0.4	0.4			± 10V Input Range	± % FSR max
Bipolar Gain Drift	TC _{AE}	– 1	25		25		+ 5V Input Range	± ppm/°C max
Bipolar Offset Error	B _{OSE}	– 1	0.2	0.2			± 10V Input Range	± % FSR max
Bipolar Offset Drift	TCB _{POS}	– 1	7		7		± 5V Input Range	± ppm/°C max
Linearity Error	L _E	– 1	1/2			1/2	Major Carries & Summations	± LSB max
Differential Linearity ²	DLE	– 1	1		1	1	Major Carries & Summations	± LSB max
+ 5V Power Supply Sensitivity	PSRR ₁	– 1	0.01			0.01	± V _{DD} = +4.75V to +5.25V	± % FSR/% max
± 15V Power Supply Sensitivity	PSRR ₂	– 1	0.005			0.005	± V _{CC} = ± 13.5V to ± 16.5V	± % FSR/% max
Conversion Speed	t _{CONV}	– 1	25			25	To 12 Bits	µs max
Serial/Parallel Code Match Error		– 1	0			0	Random Code	± Bits
+ 5V Supply Drain	I _{DD}	– 1	140			140	All Bits On	mA max
+ 15V Supply Drain	I _{CC}	– 1	40			40	All Bits On	mA max
– 15V Supply Drain	I _{EE}	– 1	35			35	All Bits On	– mA min
Total Power Dissipation	P _D	– 1	1.2				All Bits On	W max
Power Supply Range	+ V _{DD} ± V _{CC}	– 1 – 1	± 5% ± 5%				For Rated Accuracy	

NOTES

¹T_A = +25°C and ± V_S = ± 15V, V_{DD} = +5V unless otherwise specified.

²Guaranteed no missing codes. ± 5V input range.

Table 1.

5.0 Digital Output Data.

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement binary, depending on whether Bit 1 (Pin 12) or its logical inverse Bit 1 (Pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 4. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 4. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

The digital output codes corresponding to analog input voltages are shown in Table 3.

5.0.1 Short Cycle Input.

A Short Cycle Input pin 14 permits the timing cycle shown in Table 2. to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, Pin 14 is connected to +5V (Pin 16). When 10-bit resolution is desired, Pin 14 is connected to Bit 11 output Pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision $t_{10} + 100\text{ns}$ in timing diagram of Table 2. Short cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table 2.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	$t_{12} + 100\text{ns}$
2	10	0.10	21	$t_{10} + 100\text{ns}$
4	8	0.39	17	$t_8 + 100\text{ns}$

Table 2.

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1	1
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1	0
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0	0
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0	0

Table 3.

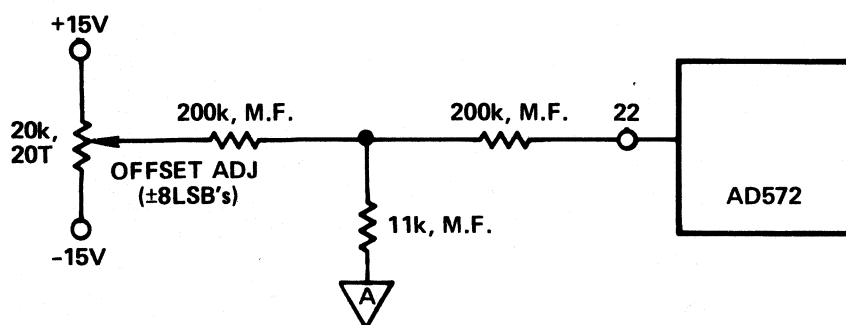


Figure 2. Low Tempco Offset Adjust Circuit

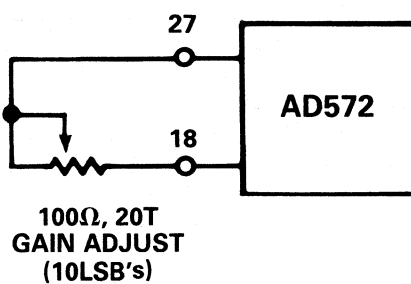


Figure 3. Gain Adjust Circuit

Range	Buffer Follower	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5V	Used Not Used	30, and 29 to 24 24	25 to 22	—
0 to +10V	Used Not Used	30, and 29 to 24 24	—	
-2.5 to +2.5V	Used Not Used	30, and 29 to 24 24	25 to 22	↑ 22 ↓
-5 to +5V	Used Not Used	30, and 29 to 24 24	—	
-10 to +10V	Used Not Used	30, and 29 to 25 25	—	

Table 4.

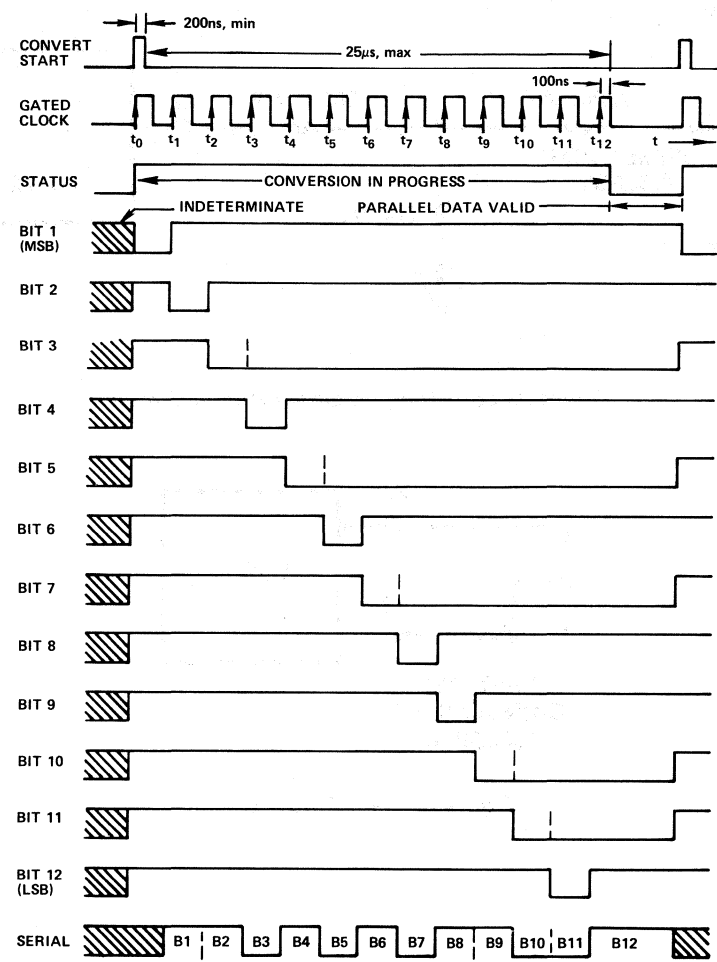


Figure 4. Timing Diagram (Binary Code 110101011001)



AD578

1.1 Scope.

This specification covers the detail requirements for a hybrid, very fast, 12-bit successive approximation analog-to-digital converter including internal clock reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD578SD/883B
-2	AD578TD/883B
-3	AD578ZSD/883B
-4	AD578ZTD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32B.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	± 18V
Logic Supply Voltage	+ 7V
Analog Inputs (Pins 27 & 28)	± 25V
Digital Inputs	+ 5.5V
Junction Temperature	+ 175°C
Storage Temperature	- 65°C to + 150°C
Lead Temperature (Soldering 10secs)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 8°C/W
 θ_{JA} = 38°C/W

AD578 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Analog Input Voltage Ranges	V _{IN}	– 1, 2, 3, 4	± 5, ± 10 0 to + 10 0 to + 20					V
Input Impedance 0 to + 10V, ± 5V ± 10V, 0 to + 20V	R _{IN}	– 1, 2, 3, 4	5 10					kΩ typ
Gain Error	V _{GE}	– 1, 2, 3, 4	0.25	0.25			10V Unipolar 20V Bipolar	± %/FSR max
Gain Drift	V _{GD}	– 1, 3 – 2, 4	50		50 30		10V Unipolar 20V Bipolar 10V Unipolar 20V Bipolar	± ppm/°C max
Unipolar Offset Error	V _{OSE}	– 1, 2, 3, 4	0.25	0.25			10V Unipolar	± %/FSR max
Unipolar Offset Drift	V _{OSD}	– 1, 3 – 2, 4	15		15 10		10V Unipolar	± ppm/°C max
Bipolar Offset Error	V _{OSE}	– 1, 2, 3, 4	0.25	0.25			20V Bipolar	± %/FSR max
Bipolar Offset Drift	V _{OSD}	– 1, 3 – 2, 4	25		25 20		20V Bipolar	± ppm/°C max
Linearity Error	RA	– 1, 2, 3, 4	1/2	1/2	3/4		10V Unipolar 20V Bipolar	± LSB max
Differential Linearity Error ²	DNL	– 1, 2, 3, 4	1	1	1		10V Unipolar 20V Bipolar	± LSB max
Reference Voltage Error	V _{REF}	– 1, 2, 3, 4	100	100				± mV max
Reference Voltage Drift	V _{REFD}	– 1, 2, 3, 4	20		20			± ppm/°C max
+ 5V Power Supply Sensitivity	PSRR	– 1, 2, 3, 4	0.005	0.005			+ 5V/± 5%	± %/% ΔV _S max
± 15V Power Supply Sensitivity	PSRR	– 1, 2	0.005	0.005			± 15V/± 10%	± %/% ΔV _S max
± 12V Power Supply Sensitivity	PSRR	– 3, 4	0.007	0.007			± 12V/± 5%	± %/% ΔV _S max
Digital Output High Drive	V _{OH}	– 1, 2, 3, 4	2.4	2.4			@ – 80μA	V min
Digital Output Low Drive	V _{OL}	– 1, 2, 3, 4	0.4	0.4			@ 3.2mA	V max
Conversion Speed	t _C	– 1, 3 – 2, 4	6 4.5			6 4.5		μs max
+ 5V Supply Drain	+ I _{DD}	– 1, 2, 3, 4	150	150			All Bits On	mA max
+ 15V Supply Drain	+ I _{CC}	– 1, 2, 3, 4	8	8			All Bits On	mA max
– 15V Supply Drain	– I _{CC}	– 1, 2, 3, 4	35	35			All Bits On	mA max
Power Supply Range	+ V _{DD} + V _{CC} + V _{CC}	– 1, 2, 3, 4 – 1, 2 – 3, 4	+ 5 ± 15 ± 12				± 5% ± 10% ± 5%	V

NOTES

¹V_{CC} = ± 15V, (± 12V for Z Model), V_{DD} = + 5V, T_A = + 25°C unless otherwise noted.

²Guaranteed No Missing Codes – 55°C to + 125°C.

Table 1.



This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD578

5.0 Gain and Offset Adjustment.

The gain and offset adjustment circuits are shown in Figure 1 for unipolar or Figure 2 for bipolar operation. If the offset and gain specifications are sufficient, the 100Ω trimmers may be replaced by a 50Ω ± 1% fixed resistor.

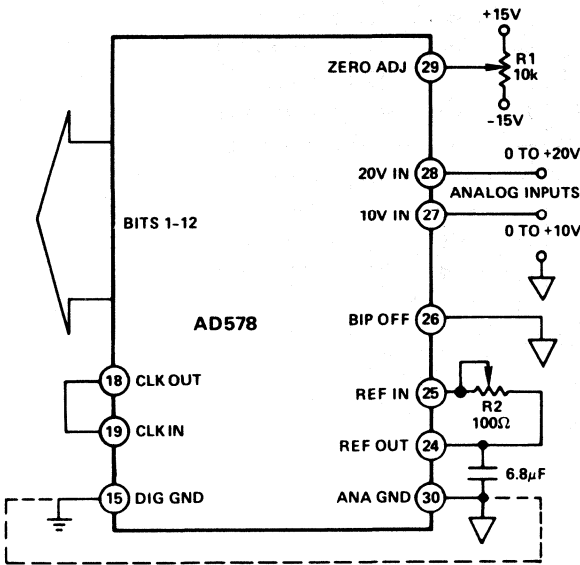


Figure 1. Unipolar Input Connections

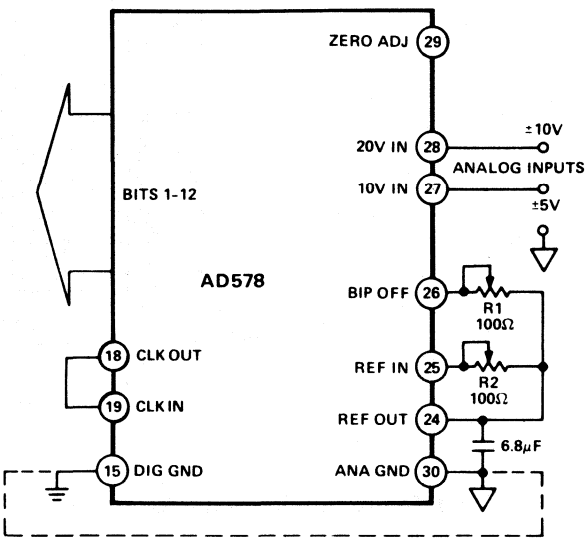


Figure 2. Bipolar Input Connections

5.1 Digital Output Data.

The digital output codes corresponding to analog input voltages are shown in Table 2.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	0 to +20V Range	– 5V to +5V Range	– 10V to +10V Range	B1 (MSB)	B12 (LSB)
+ 9.9976	+ 19.9951	+ 4.9976	+ 9.9951	1	1
+ 9.9952	+ 19.9902	+ 4.9952	+ 9.9902	1	1
⋮	⋮	⋮	⋮	⋮	⋮
+ 5.0024	+ 10.0049	+ 0.0024	+ 0.0049	1	0
+ 5.0000	+ 10.0000	+ 0.0000	+ 0.0000	1	0
⋮	⋮	⋮	⋮	⋮	⋮
+ 0.0024	+ 0.0049	– 4.9976	– 9.9951	0	0
+ 0.0000	+ 0.0000	– 5.0000	– 10.0000	0	0

Table 2. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

5.2 Clock Rate Control Alternate Connections.

The internal clock is preset to a nominal conversion time of $5.6\mu\text{s}$. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

The curves in Figure 3 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grade's conversion speed specification has been exceeded.

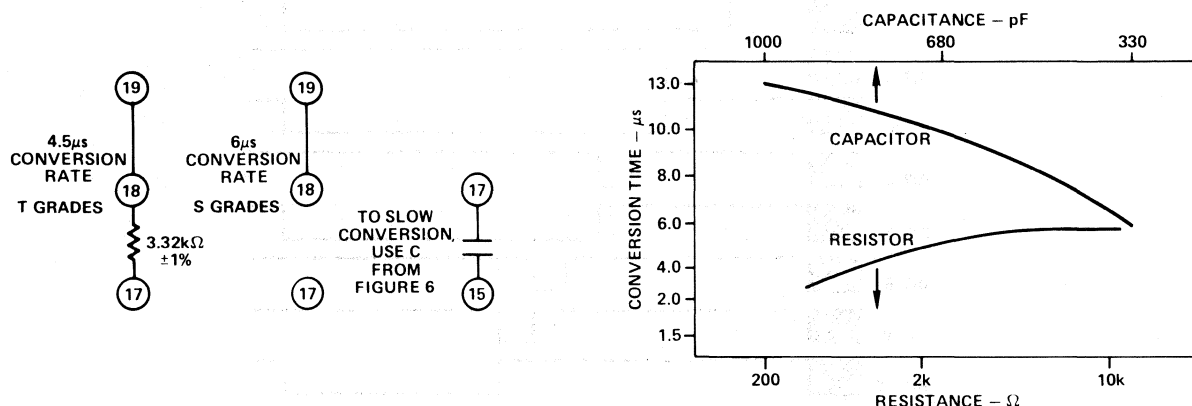


Figure 3. Conversion Time vs. R or C Values

5.2.1 External Clock.

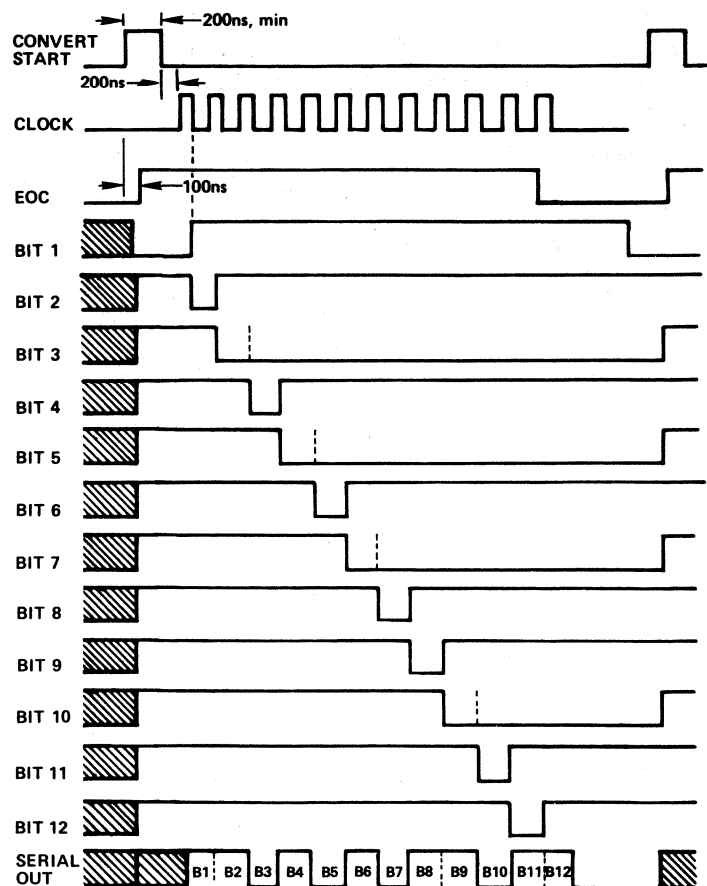
An external clock may be connected directly to the clock input, pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

5.2.2 Short Cycle Input.

A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 4 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table 3.

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	4.5	3.75	3

Table 3. Short Cycle Connections



CLOCK
 INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
 EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
 CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH
 MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
 1 THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO,
 AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 4. AD578 4.5μs Timing Diagram



Very Fast, Complete 10-Bit A/D Converter

AD579

1.1 Scope.

This specification covers the detail requirements for a hybrid, very fast, 10-bit successive approximation analog-to-digital converter including internal clock, reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD579TD/883B
-2	AD579ZTD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Logic Supply Voltage	$+7\text{ V}$
Analog Inputs (Pins 27 & 28)	$\pm 25\text{ V}$
Digital Inputs	$+5.5\text{ V}$
Junction Temperature Range	$+175^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 8^\circ\text{C/W}$
θ_{JA}	$= 38^\circ\text{C/W}$

AD579 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Analog Input Voltage Ranges	V _{IN}	–1, 2	±5, ±10 0 to 5 0 to 10					V
Gain Error End Point Electrical	V _{GE}	–1, 2	0.25	0.25 0.30				±% FSR max
Unipolar Offset Error	V _{OSE}	–1, 2	0.25	0.25			Adjustable to Zero	±% FSR max
Bipolar Offset Error End Point Electrical	V _{OSE}	–1, 2	0.25	0.25 0.30				±% FSR max
Linearity Error	L _E	–1, 2	1/2	1/2	3/4	1/2	±5 V & 0 to 10 V Range Major Carries & Summations	±LSB max
Differential Linearity ²	D _{LE}	–1, 2	1	1	1		±5 V & 0 to 10 V Range Major Carries & Summations	±LSB max
Reference Voltage Error	V _{REF}	–1, 2	100	100				+mV max
Unipolar Offset Drive	V _{OSD}	–1, 2	15		15		0 to 10 V Range	±ppm/°C max
Bipolar Offset Drift	V _{OSD}	–1, 2	20		20		±5 V Range	±ppm/°C max
Bipolar Gain Drift	V _{GD}	–1, 2	40		40		±5 V Range	±ppm/°C max
+5 V Power Supply Sensitivity	PSRR	–1	0.005				V _{DD} = +4.75 V to +5.25 V	±%/° max
±15 V Power Supply Sensitivity	PSRR	–1	0.005				V _{CC} = ±13.5 V to ±16.5 V	±%/° max
±12 V Power Supply Sensitivity	PSRR	–2	0.007				V _{CC} = ±11.4 V to ±12.60 V	±%/° max
Digital Output High Drive	V _{OH}	–1, 2	2.4	2.4			@ –80 μA	V min
Digital Output Low Drive	V _{OL}	–1, 2	0.4	0.4			@ 3.2 mA	V max
Conversion Speed ³	t _C	–1, 2	1.8		2.0	1.8		μs max
+5 V Supply Drain	+I _{DD}	–1, 2	150					mA max
+15 V Supply Drain	+I _{CC}	–1, 2	8					mA max
–15 V Supply Drain	–I _{CC}	–1, 2	35					mA max

NOTES

¹T_A = +25°C, V_{CC} = ±15 V, V_{DD} = +5 V unless otherwise noted, and 6.8 μF capacitor from Pin 24 to Pin 30.

²Guaranteed no missing codes –55°C to +125°C.

³With 422 Ω resistor between Pins 17 and 18.

Table 1.

5.0 Gain and Offset Adjustment.

The gain and offset adjustment circuits are shown in Figure 1 for unipolar or Figure 2 for bipolar operation. If the offset and gain specifications are sufficient, the 100 Ω trimmers may be replaced by a 50 Ω ±1% fixed resistor.

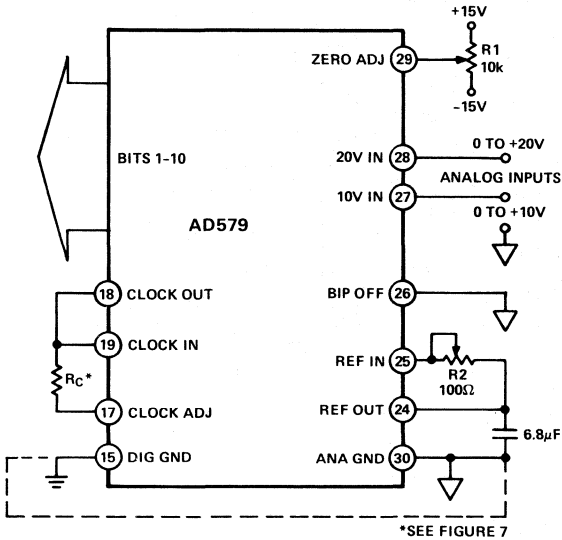


Figure 1. Unipolar Input Connections

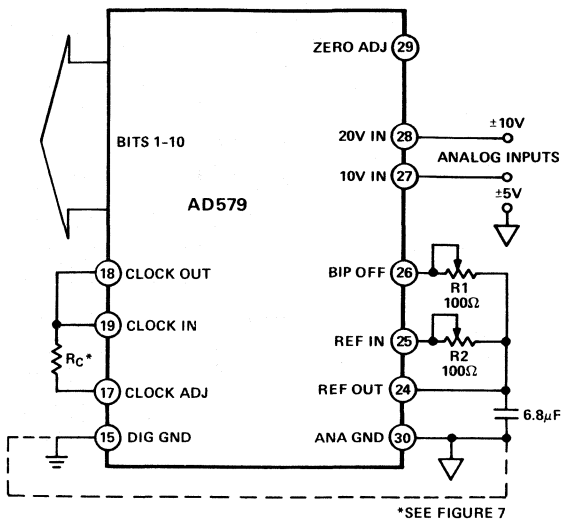


Figure 2. Bipolar Input Connections

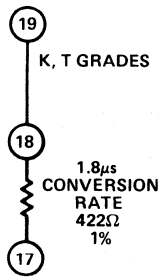


Figure 3. Clock Rate Control Connection

5.1 Digital Output Data.

The digital output codes corresponding to analog input voltages are shown in Table 2.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10 V Range	0 to +20 V Range	–5 V to +5 V Range	–10 V to +10 V Range	B1 (MSB)	B10 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1	
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 0	
.	.	.	.	.	
.	.	.	.	.	
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 1	
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0	
.	.	.	.	.	
.	.	.	.	.	
+0.0097	+0.0195	–4.9902	–9.9804	0 0 0 0 0 0 0 0 0 1	
+0.0000	+0.0000	–5.0000	–10.0000	0 0 0 0 0 0 0 0 0 0	

Table 2. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

5.1 Clock Rate Control Alternate Connections.

The internal clock is preset to a nominal conversion time of 4.8 μ s. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between Pin 17 and Pin 18 and short Pin 18 to Pin 19. The clock rate control circuit is shown in Figure 3.

5.2.1 External Clock.

An external clock may be connected directly to the clock input, Pin 19. When operating in this mode the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle.

5.2.2 Short Cycle Input.

Short Cycle Input – A Short Cycle Input, Pin 14, permits the timing cycle shown in Figure 4 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 10-bit resolution. Short cycle pin connections and associated maximum 10- and 8-bit conversion times are summarized in Table 3.

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	5
Conversion Speed (μ s)	1.8	1.5

Table 3. Short Cycle Connections

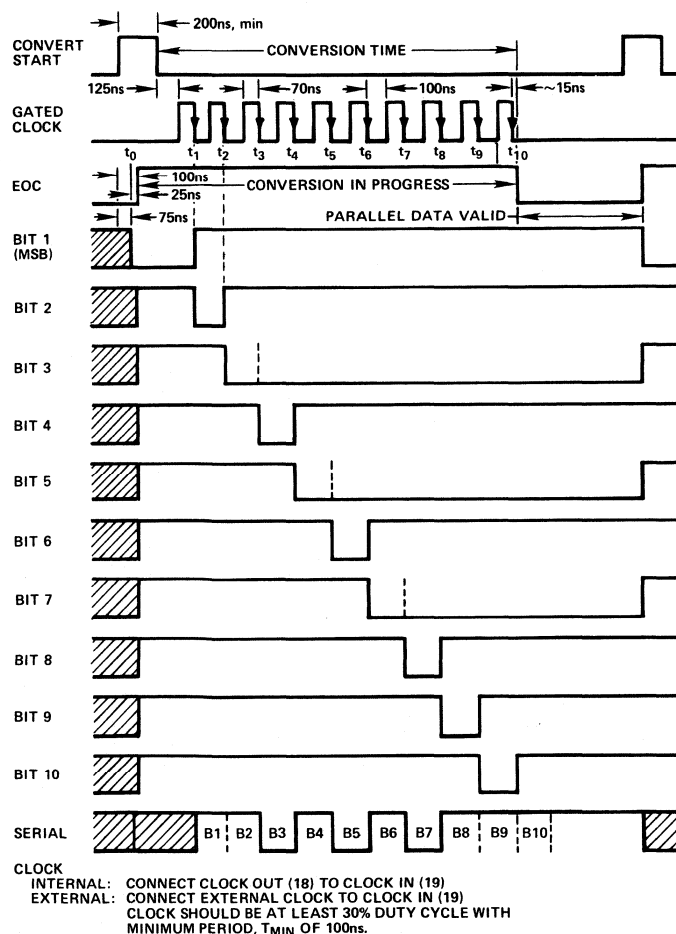


Figure 4. Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a two hybrid, 18-bit floating-point analog-to-digital converter including sample-and-hold, PGA, reference, timing and interface circuitry.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD1330TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32E and DH-48.

1.3 Absolute Maximum Ratings.

Positive Analog Supply Voltage to Analog Ground	+17 V
Negative Analog Supply Voltage to Analog Ground	–17 V
Digital Supply Voltage to Digital Ground	+7 V
Analog Ground to Digital Ground	–0.05 V to +0.05 V
Analog Input to Analog Ground	– V_S to + V_S
Digital Input to Digital Ground	–0.3 V to V_{DD} +0.3 V
Analog Output Short Circuit Duration	Indefinite
Digital Output Short Circuit Duration	1 Output for 1 sec
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

AD1330 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
INPUT CHARACTERISTICS								
Differential Input Range	V_{IND}	-1	5					$\pm V$ min
Common Mode Range	V_{CM}	-1	10					$\pm V$ min
Input Resistance								
Signal	R_{INS}	-1		4				k Ω min
Ground	R_{ING}	-1		10				k Ω min
Offset	V_{OS}	-1		10			Note 2	mV max
Offset Drift	V_{OSD}	-1			± 100		Note 3	$\mu V/^{\circ}C$ max
CMRR	CMRR	-1		-70	-70		$V_{CM} = \pm 5$	dB min
PSRR	PSRR-	-1		60	60		Note 4	dB min
TRANSFER CHARACTERISTICS								
Gain Error	G_E	-1		0.3			Note 5	% max
Gain Error Drift	G_{ED}	-1			± 50			ppm/ $^{\circ}C$ max
Gain Match, Adj Ranges	G_{MT}	-1		0.08	0.12			% max
Gain Switching Accuracy	G_{SW}	-1		10	15		Note 6	% max
Integral Nonlinearity	ILE	-1		± 2	± 2		Note 7, 8	LSB max
Differential Nonlinearity	DLE	-1		± 2	± 2		Note 7, 8	LSB max
DYNAMIC SPECIFICATIONS								
Signal-to-Noise Ratio							Note 9	
Fixed Gain								
AIS Gain = $\times 64$	SNR1	-1		56				dB min
AIS Gain = $\times 32$	SNR2	-1		60				dB min
AIS Gain = $\times 16$	SNR3	-1		64				dB min
AIS Gain = $\times 1$ to $\times 8$	SNR4	-1		68				dB min
Auto Gain								
Gains 1-64 to 8-64	SNR5	-1		66				dB min
Gains 16-64	SNR6	-1		62				dB min
Gains 32-64	SNR7	-1		58				dB min
Total Harmonic Distortion							Note 10	
Fixed Gain	THD_F	-1		-72				dB max
Auto Gain	THD_A	-1		-67				dB max
Peak Distortion	IMD	-1		-72			Note 9	dB max
Input Referred Noise	N_{IN}	-1	88				Note 11	μV rms max
REFERENCE								
Reference Voltage	V_{REF}	-1		4.95				V min
				5.05				V max
Reference Drift	V_{REFD}	-1			± 25			ppm/ $^{\circ}C$ max
Output Resistance	R_{OUT}	-1	4.0					k Ω min
			6.0					k Ω max
DIGITAL INPUTS AND OUTPUTS								
Input Volt, Logic Low	V_{IL}	-1		0.8	0.8			V max
Input Volt, Logic High	V_{IH}	-1		2.0	2.25			V min
Input Current	I_I	-1		± 100	± 100			μA max
Output Volt, Logic Low	V_{OL1}	-1		0.4			$I_{OL} = 4$ mA	V max
	V_{OL2}	-1			0.4		$I_{OL} = 3.2$ mA	V max
Output Volt, Logic High	V_{OH1}	-1		2.4			$I_{OH} = -4$ mA	V min
	V_{OH2}	-1			2.4		$I_{OH} = -3.2$ mA	V min
High Imp. Leakage Current	I_{OZ}	-1		± 10	± 10			μA max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
POWER SUPPLY								
+ Analog Supply	+V _S	-1	+14.25 +15.75					V min V max
- Analog Supply	-V _S	-1	-14.25 -15.75					V min V max
Digital Supply	V _{DD}	-1		+4.5 +5.5	+4.5 +5.5			V min V max
+ Analog Supply Current	I _{S+}	-1		70				mA max
- Analog Supply Current	I _{S-}	-1		80				mA max
Logic Supply Current	I _{DD}	-1		70				mA max
Power Consumption								
AIS + CCS	P _{D1}	-1		2.6			V _S = ±15 V	W max
AIS	P _{D2}	-1		1.4			V _S = ±15 V	W max
CCS	P _{D3}	-1		1.2			V _S = ±15 V	W max
Clock Frequency	F _{CLK}	-1		2.5	2.5			MHz max
Sample Rate	F _S	-1		100	100			kHz max
CLK Duty Cycle	T _{DTY}	-1	45 55					% min % max
READ CYCLE								
Read Cycle Time	t _{WC}	-1	25	35	35		Co = 30 pF Co = 100 pF	ns min ns max
Data Access Time	t _A	-1	15 25	30	30		Co = 30 pF Co = 100 pF Co = 150 pF	ns max ns max ns max
Out Low Impedance Time	t _{LZ}	-1	2					ns min
Out High Impedance Time	t _{HZ}	-1	15	25	25		Co = 30 pF Co = 100 pF	ns max ns max
Output Hold Time	t _{OH}	-1	2					ns min
A0 Valid to $\overline{\text{RD}}$ Low	t _{AORD}	-1	3					ns min
$\overline{\text{RD}}$ High to A0 Invalid	t _{RDAO}	-1	3					ns min
A0/1 Valid to $\overline{\text{CS}}$ Low	t _{AOCS}	-1	3					ns min
$\overline{\text{CS}}$ High to A0/1 Invalid	t _{CSAO}	-1	3					ns min
IRQ Low to D0-D15 Valid	t _{DVAL}	-1	0					ns max
WRITE CYCLE								
Write Cycle Time	t _{WC}	-1		15	15			ns min
Write Pulse Width	t _{WP}	-1	5					ns min
Data Setup Time	t _{SU}	-1	3					ns min
Input Hold Time	t _{IH}	-1	3					ns min
A0/1 Valid to $\overline{\text{WR}}$ Low	t _{AOWR}	-1	3					ns min
$\overline{\text{WR}}$ High to A0 Invalid	t _{WRAO}	-1	3					ns min
A0/1 Valid to $\overline{\text{CS}}$ Low	t _{AOCS}	-1	3					ns min
$\overline{\text{CS}}$ High to A0 Invalid	t _{CSAO}	-1	3					ns min

NOTES

¹All specifications with +V_S = +15 V, -V_S = -15 V, V_{DD} = +5 V unless otherwise noted.

²Sum of differential amplifier offset, SHA1 offset, and SHA1 pedestal; specified after 5 minute warmup. These offsets add directly to the input signal.

³Offset as defined in Note 1.

⁴Measured at PGA output with differential amplifier input grounded and fixed AIS gain of ×64.

⁵Gain is trimmed with the AIS set to a fixed gain of ×1 to produce a change of 4094 LSBs in the ADC Word for a 9.9951 volt change in input (10 volt span).

⁶Gain-switching thresholds are set to ±80% of full scale to prevent overranging the internal A/D converter under combinations of component tolerance and operating temperature. Gain Switching Accuracy is the error in the switching threshold as a percentage of the ideal threshold.

⁷Measured with fixed AIS gain of ×1; does not include effects of gain ratio matching.

⁸Specification is worst case total of AIS + CCS.

⁹SNR of fundamental less harmonics 2-5. Fixed-gain testing uses the largest possible input for each gain without clipping. Autogain testing measures SNR with input -2 dB with respect to each successive gain-switching threshold.

¹⁰THD of harmonics 2-5 with the fundamental. When testing fixed gains the input is -0.3 dB with respect to full scale for that gain. Autogain testing measures THD with input -2 dB with respect to each successive gain-switching threshold.

¹¹In autogain mode, the amplitude of the largest single harmonic component, regardless of harmonic number, relative to the fundamental.

¹²Derived from the FFT noise floor when the AIS gain is ×64 and the input is grounded.

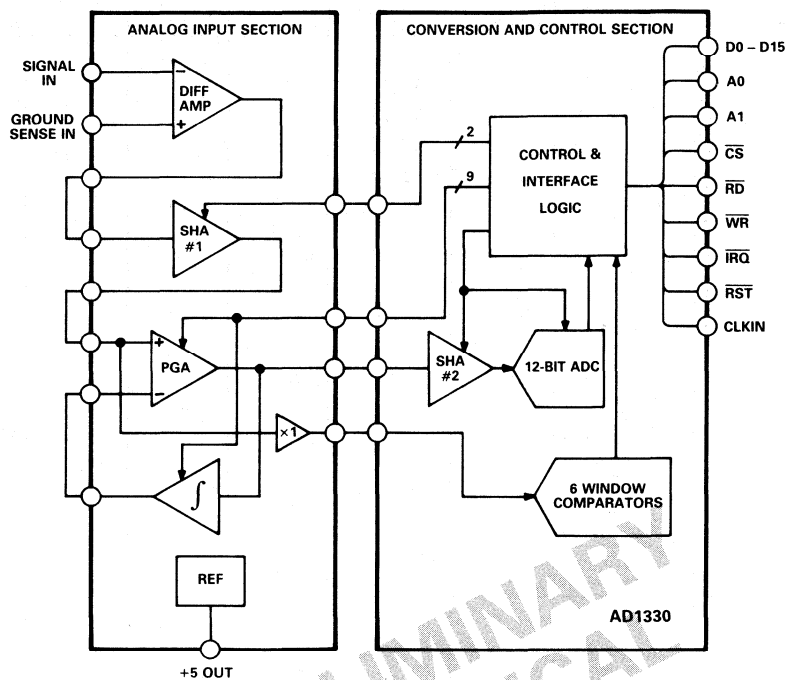
Table 1.

REV. A

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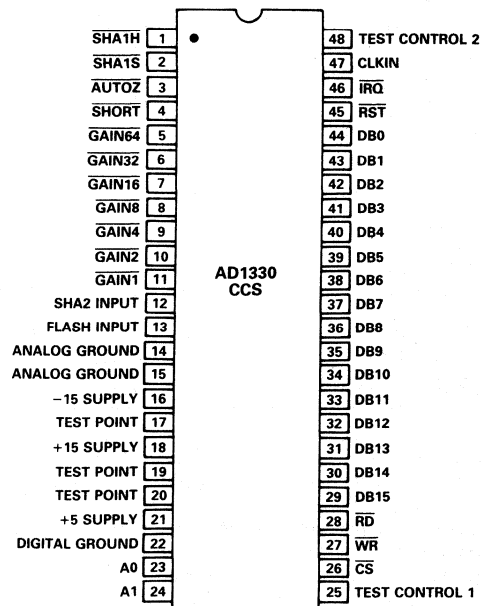
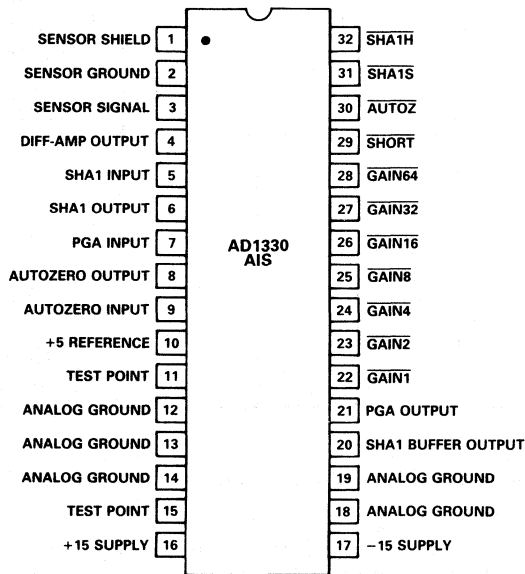
AD1330

3.2.1 Functional Block Diagram and Terminal Assignments.



AIS Pinout

CCS Pinout



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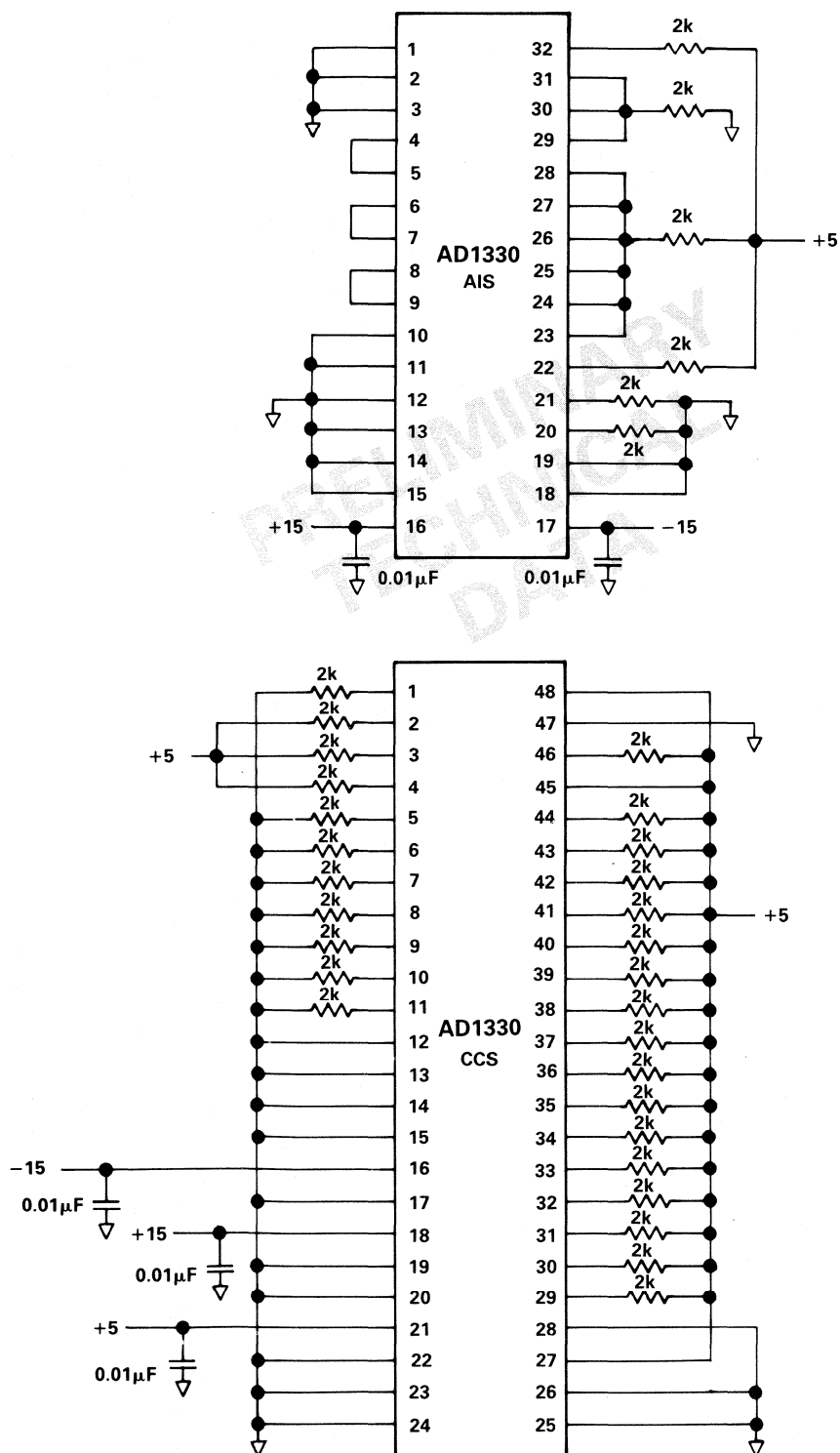
REV. A

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life/Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).





Complete 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1332

1.1 Scope.

This specification covers the detail requirements for a hybrid, 12-bit analog-to-digital converter including internal filter, reference, timing circuitry and FIFO memory.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD1332TD/883B

1.2.3 Case Outline.

See Appendix 1 of the General Specification ADI-H-1000; package: DH-40A

1.3 Absolute Maximum Ratings.

Positive Analog Supply Voltage to Power/Signal Ground	+17 V
Negative Analog Supply Voltage to Power/Signal Ground	-17 V
Digital Supply Voltage to Digital Ground	+7 V
Power/Signal Ground to Digital Ground	-0.3 V to +0.3 V
Analog Input to Power/Signal Ground	$-V_S$ to $+V_S$
Digital Input to Power Ground	-0.3 V to +7 V
Digital Input to Digital Ground	-0.3 V to $V_{DD}+0.3$ V
Analog Output Short Circuit Duration	Indefinite
Digital Output Short Circuit Duration	1 Output for 1 sec
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = TBD °C/W
 θ_{JA} = TBD °C/W

AD1332 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
FILTER								
Input Impedance	F_{ZIN}	-1	8				$R_L > 4 \text{ k}\Omega$	k Ω min
Input Voltage Range	F_{VIN}	-1	± 10					V min
Output Voltage Range	F_{VOUT}	-1	± 10					V min
Offset Voltage	F_{VOS}	-1		± 5	± 20			mV max
Gain dc	F_{G1}	-1		± 0.05				dB max
0.8 fc	F_{G2}	-1		± 1				dB max
fc	F_{G3}	-1	-3					dB typ
4 fc	F_{G4}	-1		-45				dB max
10 fc	F_{G5}	-1	-76					dB typ
Settling Time	F_{SET}	-1	125				Note 2	μs max
SAMPLE-AND-HOLD								
Acquisition Time to 0.1%	SH_{TACQ}	-1	2.8					μs max
Droop Rate	SH_{DRP}	-1	1					mV/ms max
Droop Rate, Over Temperature	SH_{TCDRP}	-1	Doubles					/10°C typ
SAMPLE-AND-HOLD & A/D CONVERTER								
Input Impedance	AD_{ZIN}	-1	4					k Ω min
Input Voltage Range	AD_{VIN}	-1	± 5					V
Sampling Rate	AD_{FS}	-1		125	125			kHz max
CLK IN Frequency	AD_{FIN}	-1		2.5	2.5			MHz max
CLK Duty Cycle	AD_{DC}	-1	45 55					% min % max
Integral Nonlinearity	AD_{ILE}	-1		± 1	± 1		Notes 3, 4 $f_{in} = f_1$	LSB max
Resolution, NMC	AD_{NME}	-1		12	12			Bits min
- Full Scale Error	AD_{FSE-}	-1		± 2	± 13		Notes 3, 4 $f_{in} = f_1$	LSB max
+ Full Scale Error	AD_{FSE+}	-1		± 2	± 13			LSB max
- Full Scale PSRR	$PSRR-$	-1		± 1.5	± 1.5		Notes 3, 4 $f_{in} = f_2$	LSB/V max
+ Full Scale PSRR	$PSRR+$	-1		± 1.5	± 1.5			LSB/V max
Signal-to-Noise Ratio								
With Filter	SNR_F	-1				70	$f_{in} = f_1$	dB min
Without Filter	SNR	-1				70	$f_{in} = f_2$	dB min
Total Harmonic Distortion								
With Filter	THD_F	-1				-72	$f_{in} = f_1$	dB max
Without Filter	THD	-1				-68	$f_{in} = f_2$	dB max
Intermodulation Distortion								
With Filter	IMD_F	-1				-72	$f_{in} = f_3, f_4$	dB max
Without Filter	IMD	-1				-68	$f_{in} = f_5, f_6$	dB max
REFERENCE								
Reference Voltage	V_{REF}	-1		-5.05 -4.95				V min V max
Reference Current	I_{REF}	-1	± 1					mA min
DIGITAL INPUTS AND OUTPUTS								
Input Voltage, Logic Low $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$, A0 D0-D7, PTC $\overline{EN}$ SAMPLE IN, CLK IN	V_{IL1} V_{IL2}	-1 -1		+0.8 +1.5	+0.8 +1.5			V max V max
Input Voltage, Logic High $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$, A0 D0-D11, PTC $\overline{EN}$ SAMPLE IN, CLK IN	V_{IH1} V_{IH2}	-1 -1		+2.0 +3.5	+2.25 +3.5			V min V min
Input Current $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$, A0 D0-D7, PTC $\overline{EN}$ SAMPLE IN, CLK IN	I_{IL} I_{I2}	-1 -1		± 200 ± 10	± 200 ± 10			μA max μA max

Table 1. (Continued on next page)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REV. A

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
DIGITAL INPUTS AND OUTPUTS (cont.)								
Output Voltage, Logic Low D0-D11, SAMPLE OUT	V _{OL1}	-1		0.4	0.4		I _{OL} = 4 mA I _{OL} = 3.2 mA	V max V max
$\overline{\text{IRQ}}$, PTC $\overline{\text{ENB}}$	V _{OL2}	-1		0.4	0.4		I _{OL} = 4 mA I _{OL} = 3.2 mA	V max V max
Output Voltage, Logic High D0-D11	V _{OH1}	-1		2.4	2.4		I _{OH} = -4 mA I _{OH} = -3.2 mA	V min V min
SAMPLE OUT	V _{OH2}	-1		4.0	4.0		I _{OH} = -0.4 mA	V min
High Impedance Leakage Current D8-D11	I _{OZ1}	-1		±10	±10			μA max
Off-State Leakage Current, $\overline{\text{IRQ}}$	I _{OZ2}	-1		±10	±10			μA max
RST Pulse Width	t _{RPW}	-1	10					ns min
FIFO Fall-Thru Time	t _{FT}	-1	800					ns max
$\overline{\text{IRQ}}$ Low to D0-D11 Valid	t _{DUAL}	-1	0				Note 5	ns max
POWER SUPPLY								
+ Analog Supply	+V _S	-1	+11.4 +15.75					V min V max
- Analog Supply	-V _S	-1	-11.4 -15.75					V min V max
Logic Supply	V _{DD}	-1		+4.75 +5.25	+4.75 +5.25			V min V max
+ Analog Supply Current	I _{S+}	-1		57				mA max
- Analog Supply Current	I _{S-}	-1		57				mA max
Logic Supply Current	I _{DD}	-1		15				mA max
Power Consumption	P _{D1}	-1		1.4			V _S = ±12 V	W max
	P _{D2}	-1		1.75			V _S = ±15 V	W max
READ CYCLE								
Read Cycle Time	t _{RC}	-1	25 35				Note 6 C _{OUT} = 30 pF C _{OUT} = 100 pF	ns min ns max
Data Access Time	t _A	-1	15 25	35	35		C _{OUT} = 30 pF C _{OUT} = 100 pF C _{OUT} = 150 pF	ns max ns max ns max
Out Low Impedance Time	t _{LZ}	-1	2					ns min
Out High Impedance Time	t _{HZ}	-1	15 25				C _{OUT} = 30 pF C _{OUT} = 100 pF	ns max ns max
Output Hold Time	t _{OH}	-1	2					ns min
A0 Valid to $\overline{\text{RD}}$ Low	t _{AORD}	-1	3					ns min
$\overline{\text{RD}}$ High to A0 Invalid	t _{RDAO}	-1	3					ns min
A0 Valid to $\overline{\text{CS}}$ Low	t _{AOCs}	-1	3					ns min
$\overline{\text{CS}}$ High to A0 Invalid	t _{CSAO}	-1	3					ns min
WRITE CYCLE								
Write Cycle Time	t _{WC}	-1	15					ns min
Write Pulse Width	t _{WP}	-1	5					ns min
Data Setup Time	t _{SU}	-1	2					ns min
Input Hold Time	t _{IH}	-1	4					ns min
A0 Valid to $\overline{\text{WR}}$ Low	t _{AOWR}	-1	3					ns min
$\overline{\text{WR}}$ High to A0 Invalid	t _{WRAO}	-1	3					ns min
A0 Valid to $\overline{\text{CS}}$ Low	t _{AOCs}	-1	3					ns min
$\overline{\text{CS}}$ High to A0 Invalid	t _{CSAO}	-1	3					ns min

NOTES

¹All specifications with +V_S = 15 V, -V_S = -15 V, V_{DD} = 5 V, C1 = C2 = C3 = C4 = 500 pF ±1%, unless otherwise noted.

F_{CLK} = 2.5 MHz, SAMPLE-IN connected to SAMPLE-OUT, PTC EN = Logic Low.

²Settling Time to 0.01%, 10 V Step.

³f1 = 38.7 kHz, f2 = 60.9 kHz, f3 = 32.8 kHz, f4 = 34.3 kHz, f5 = 58.7 kHz, f6 = 60.9 kHz.

⁴THD of harmonics 2-7 of the fundamental. SNR of fundamental less harmonics 2-7.

⁵ $\overline{\text{RD}}$, $\overline{\text{CS}}$, A0 = Logic Low and $\overline{\text{WR}}$, RST = Logic High

⁶C_{OUT} = 30 pF or 100 pF except as noted.

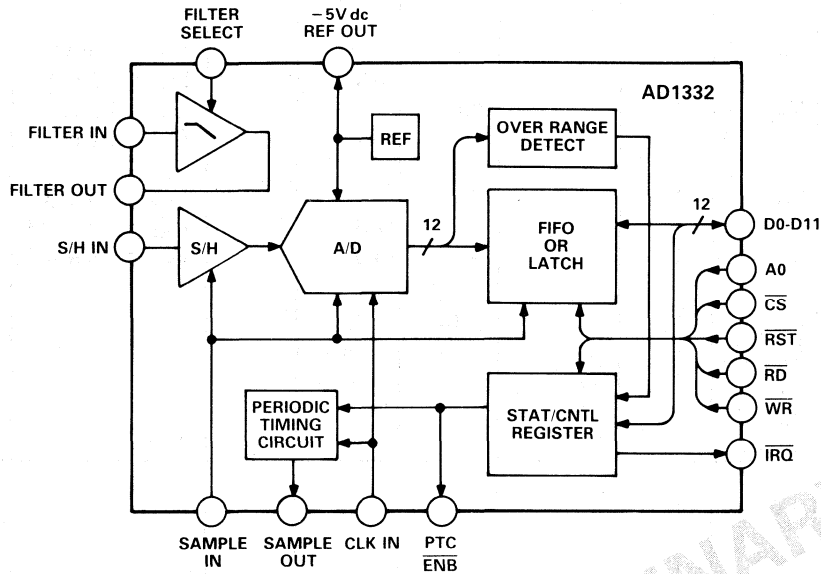
Table 1.

REV. A

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD1332

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

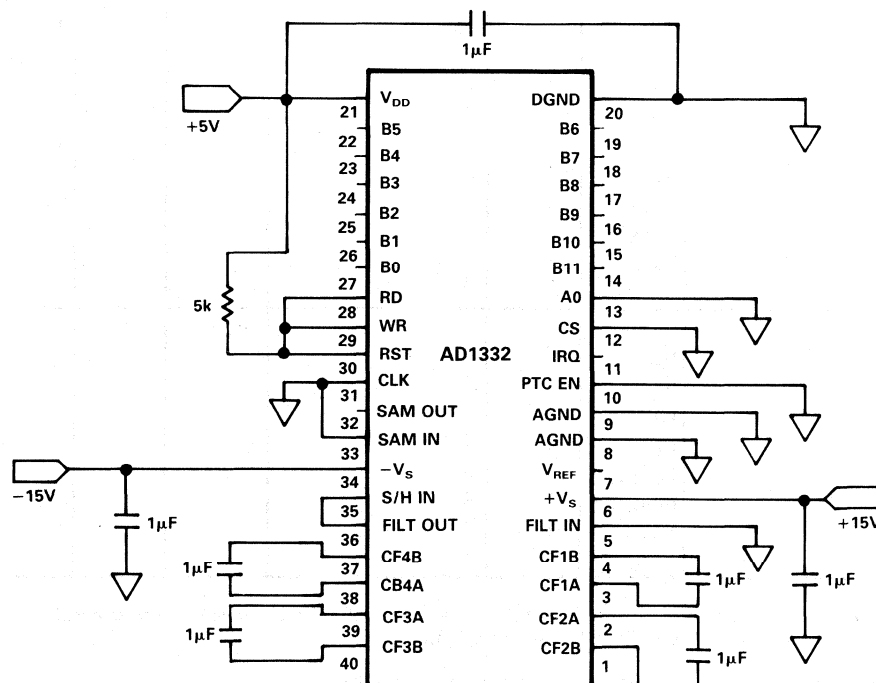
C2 _{WV}	0 1	40 0	C3 _{WV}
C2 _{VG}	0 2	39 0	C3 _{VG}
C1 _{VG}	0 3	38 0	C4 _{VG}
C1 _{WV}	0 4	37 0	C4 _{WV}
FILTERIN	0 5	36 0	FILTEROUT
+ V _S	0 6	35 0	S/HIN
REFOUT	0 7	34 0	- V _S
ASIG GND	0 8	33 0	SAMPLEIN
APWR GND	0 9	32 0	SAMPLE OUT
PTC ENB	0 10	31 0	CLKIN
IRQ	0 11	30 0	RST
CS	0 12	29 0	WR
A0	0 13	28 0	RD
(MSB) D11	0 14	27 0	D0 (LSB)
D10	0 15	26 0	D1
D9	0 16	25 0	D2
D8	0 17	24 0	D3
D7	0 18	23 0	D4
D6	0 19	22 0	D5
DGND	0 20	21 0	V _{DD}

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life/Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REV. A

1.1 Scope.

This specification covers the detail requirements for a hybrid, 12-bit analog-to-digital converter including quad sample-and-hold, reference, timing circuitry and FIFO memory.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD1334TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-40A.

1.3 Absolute Maximum Ratings.

Positive Analog Supply Voltage to Power/Signal Ground	+17 V
Negative Analog Supply Voltage to Power/Signal Ground	-17 V
Digital Supply Voltage to Digital Ground	+7 V
Power/Signal Ground to Digital Ground	-0.3 V to +0.3 V
Analog Input to Power/Signal Ground	$-V_S$ to $+V_S$
Digital Input to Power Ground	-0.3 V to +7 V
Digital Input to Digital Ground	-0.3 V to $V_{DD} + 0.3$ V
Analog Output Short Circuit Duration	Indefinite
Digital Output Short Circuit Duration	1 Output for 1 sec
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= TBD
θ_{JA}	= TBD

AD1334 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
SAMPLE-AND-HOLD								
Acquisition Time to 0.01%	SH _{TACQ}	–1	7.5					μs max
Droop Rate	SH _{DRP}	–1	1					mV/ms max
Droop Rate, over Temperature	SH _{TCDRP}	–1	Doubles					/10°C
Aperture Delay	SH _{AD}	–1	15				Note 3	ns max
Effective Aperture Delay	SH _{EAD}	–1	–700				Note 4	ns min
		–1	–850					ns max
S/H, MUX & A/D CONVERTER								
Input Impedance	AD _{ZIN}	–1	2					kΩ min
Input Voltage Range	AD _{VIN}	–1	±5					V
CLK IN Frequency	f _{CLK}	–1	1.0					MHz min
				2.5	2.5			MHz max
CLK Duty Cycle	AD _{DC}	–1	45					% min
			55					% max
Sampling Rate Per Channel	F _S	–1						
Simultaneous Mode (SIMULT = LOW)								
1 Channel	f _{SS1}	–1	67					kHz max
2 Channels	f _{SS2}	–1	46					kHz max
3 Channels	f _{SS3}	–1	35					kHz max
4 Channels	f _{SS4}	–1		28	28			kHz max
Independent Mode (SIMULT = HIGH)								
1 Channel	f _{SI1}	–1	67					kHz max
2 Channels	f _{SI2}	–1	67					kHz max
3 Channels	f _{SI3}	–1	44					kHz max
4 Channels	f _{SI4}	–1	93					kHz max
Integral Nonlinearity	AD _{ILE}	–1		±1	±1			LSB max
Resolution, NMC	AD _{NMC}	–1		12	12			Bits min
– Full-Scale Error	AD _{FSE–}	–1		±4	±13			LSB max
+ Full-Scale Error	AD _{FSE+}	–1		±4	±13			LSB max
– Full-Scale PSRR	PSRR–	–1		±1.5	±1.5			LSB/Vmax
+ Full-Scale PSRR	PSRR+	–1		±1.5	±1.5			LSB/Vmax
Signal-to-Noise Ratio	SNR	–1				70	Note 5 f _{IN} = f1	dB min
Total Harmonic Distortion	THD	–1				–76	f _{IN} = f1	dB max
Intermodulation Distortion	IMD	–1				–76	f _{IN} = f1, f2	dB max
Channel-to-Channel Isolation	CCI _L	–1					Note 6 f _{IN} = f1	dB min
						70		
REFERENCE								
Reference Voltage	V _{REF}	–1		–5.05				V min
				–4.95				V max
Reference Current	I _{REF}	–1		±1				mA min
DIGITAL INPUTS & OUTPUTS								
Input Voltage, Logic Low	V _{IL}	–1		0.8	0.8			V max
Input Voltage, Logic High	V _{IH}	–1		2.0	2.25			V min
Input Current	I _I	–1		±250	±250			μA max
Output Voltage, Logic Low	V _{OL1}	–1		0.4			I _{OL} = 4 mA	V max
	V _{OL2}	–1			0.4		I _{OL} = 3.2 mA	V max
Output Voltage, Logic High	V _{OH1}	–1		2.4			I _{OL} = –4 mA	V min
	V _{OH2}	–1			2.4		I _{OL} = –3.2 mA	V min
High Impedance Leak Current, D8–D13	I _{OZ}	–1		±10	±10			μA max
IRQ Off-State Leakage	I _{O2}	–1		±10	±10			μA max
RST Pulse Width	t _{RPW}	–1	10					ns min
FIFO Fall-Thru Time	t _{FT}	–1	800					ns max
IRQ LOW to D0–D13 Valid	t _{DUAL}	–1	0				Note 7	ns max

Table 1. (continued on next page)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
POWER SUPPLY								
+ Analog Supply	+V _S	-1	+11.4 +15.75					V min V max
- Analog Supply	-V _S	-1	-11.4 -15.75					V min V max
Digital Supply	V _{DD}	-1		+4.75 +5.25	+4.75 +5.25			V min V max
+ Analog Supply Current	I _S +	-1		49				mA max
- Analog Supply Current	I _S -	-1		49				mA max
Logic Supply Current	I _{DD}	-1		15				mA max
Power Consumption	P _{D1}	-1		1.2			V _S = ±12 V	W max
	P _{D2}	-1		1.5			V _S = ±15 V	W max
READ CYCLE						Note 8		
Read Cycle Time	t _{RC}	-1	25 35				C _{OUT} = 100 pF	ns min ns max
Data Access Time	t _A	-1	15 25				C _{OUT} = 30 pF	ns max
				35	35		C _{OUT} = 100 pF	ns max
							C _{OUT} = 150 pF	ns max
Out Low Impedance Time	t _{LZ}	-1	2					ns min
Out High Impedance Time	t _{HZ}	-1	15 25				C _{OUT} = 30 pF	ns max
							C _{OUT} = 100 pF	ns max
Output Hold Time	t _{OH}	-1	2					ns min
A0 Valid to RD Low	t _{AORD}	-1	3					ns min
RD High to A0 Valid	t _{RDAO}	-1	3					ns min
A0 Valid to CS Low	t _{AOCS}	-1	3					ns min
CS High to A0 Invalid	t _{CSAO}	-1	3					ns min
WRITE CYCLE								
Write Cycle Time	t _{WC}	-1	15					ns min
Write Pulse Width	t _{WP}	-1	5					ns min
Data Setup Time	t _{SU}	-1	2					ns min
Input Hold Time	t _{IH}	-1	4					ns min
A0 Valid to WR Low	t _{AOWR}	-1	3					ns min
WR High to A0 Invalid	t _{WRAO}	-1	3					ns min
A0 Valid to CS Low	t _{AOCS}	-1	3					ns min
CS High to A0 Invalid	t _{CSAO}	-1	3					ns min

NOTES

¹Specifications are per channel in 4-channel simultaneous mode SAMPLE 0-3 connected together and SIMULT $\overline{\text{EN}}$ = LOW, at FS = 28 kHz, and with SAMPLE 0-3 having an 88% duty cycle unless noted.

²All specifications with +V_S = 15 V, -V_S = -15 V, V_{DD} = 5 V, f_{CLK} = 2.5 MHz CONTROL $\overline{\text{EN}}$ = Logic Low unless otherwise noted.

³Aperture delay is the time delay from the SAMPLE input to S/H switch opening and is a measure of the digital time delay through S/H.

⁴Effective aperture delay is the difference between analog and digital time delays described in (2) and (3).

⁵THD of harmonics 2-7 of the fundamental. SNR of fundamental less harmonics 2-7.

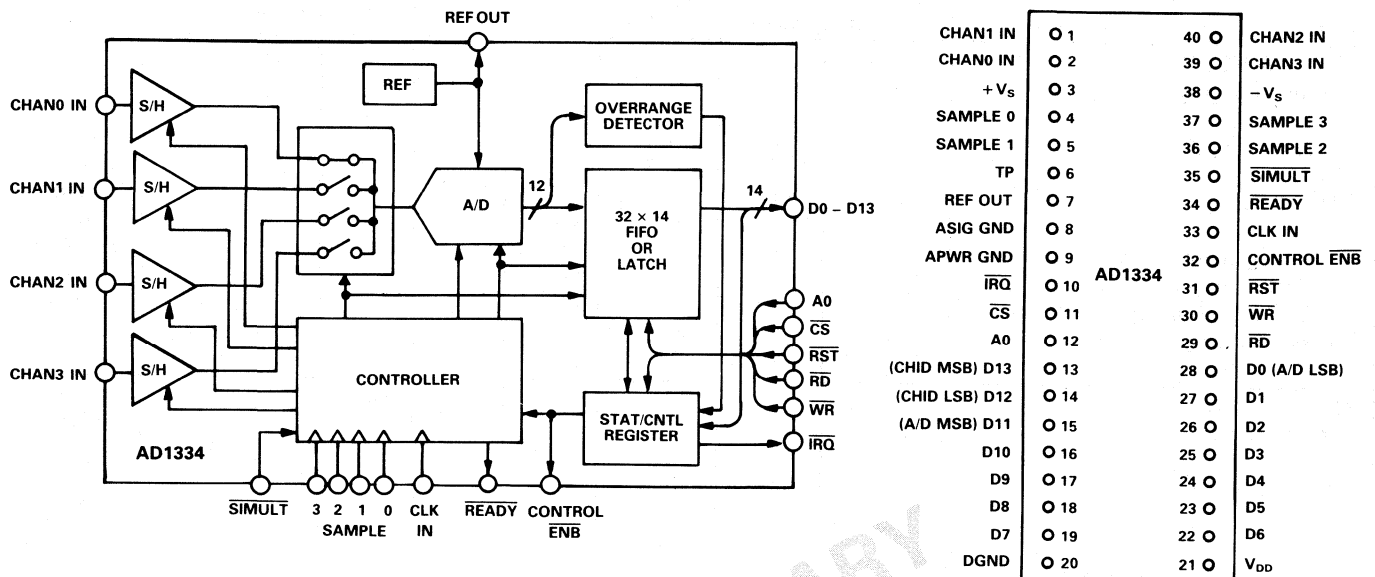
⁶Isolation of anyone channel from remaining three channels which have near maximum amplitude ac signals at their inputs.

⁷RD, CS, A0 = LOW; WR, RST = HIGH.

Table 1.

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3.2.1 Functional Block Diagram and Terminal Assignments.

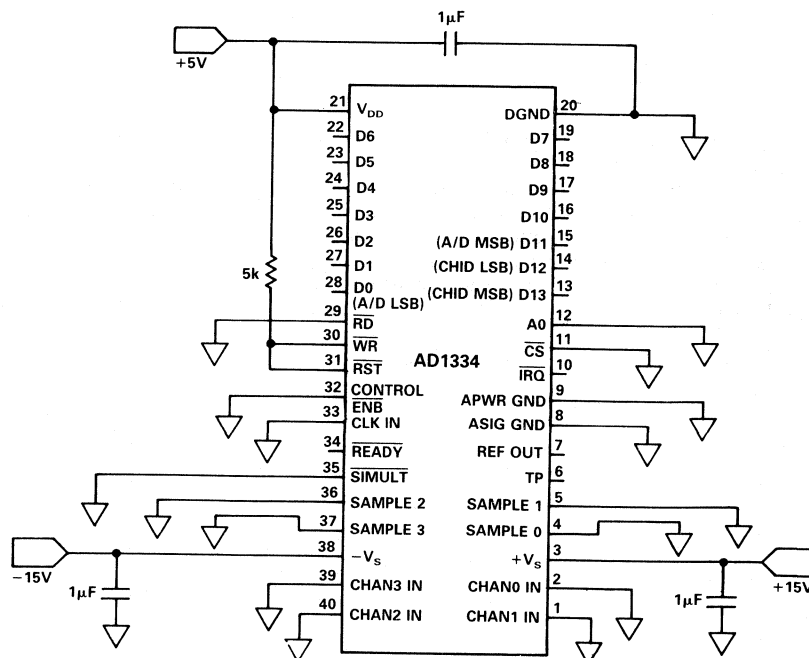


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life/Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for a hybrid multiplexer and track and hold amplifier combination.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	AD1362SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32E.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{IN} , Signal	$\pm V_S$
Positive Supply Voltage	+17V
Negative Supply Voltage	–17V
Logic Supply Voltage (V_{DD})	+5.5V
Signal Inputs	$\pm V_S$
Input Fault Current	$\pm 20\text{mA}$
Logic Inputs	+ V_{DD}
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= 7°C/W
θ_{JA}	= 40°C/W

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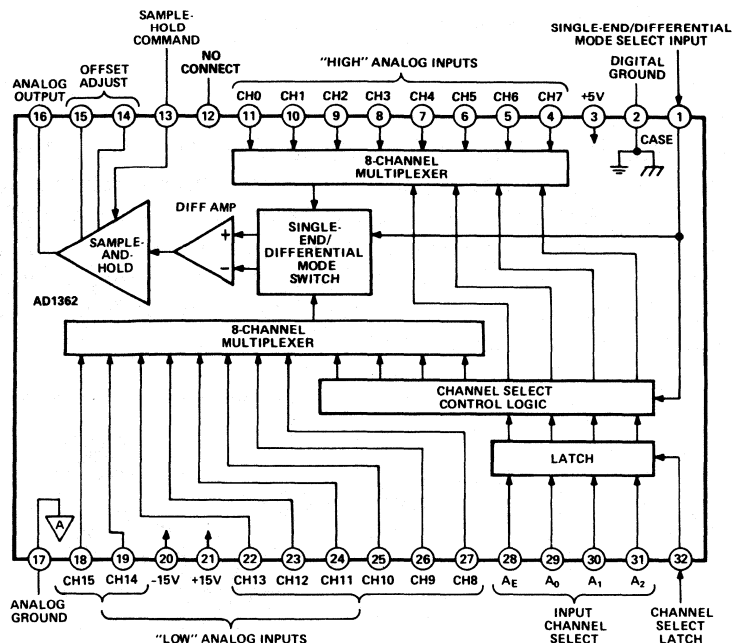
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition ¹	Units
Positive Supply Current	I _{CC}	– 1	23			30	No Load, Grounded	mA max
Negative Supply Current	I _{EE}	– 1	23			30	Inputs Track Mode	mA max
Logic Supply Current	I _{LOGIC}	– 1	23			40		mA max
Output Offset Voltage	V _{OS}	– 1	4.0	4.0			All Inputs Shorted to Analog Common Track Mode	± mV max
Channel-to-Channel Offset	V _{OS-CC}	– 1	2.5			2.5		± mV max
Common-Mode Rejection Ratio	CMRR	– 1	70			70	20V pk-pk max @ 1kHz on Diff Inputs	dB min
Input Bias Current	I _B	– 1	1			50		± nA max
Gain Error, FS	A _E	– 1	0.02	0.02				± % FSR
Crosstalk, CH-CH	V _{CT}	– 1	2.0			2.0	± 10V max on Adjacent Channels	– mV max
Droop Rate	V _{DRP}	– 1	2.0			2.0		mV/ms max
T/H Offset Pedestal	SH _{OS}	– 1	15			15	V _{IN} = 0V	± mV max
Linearity Error	LE	– 1	0.005				± 10V Input max	% FSR max
Number of Inputs	CH _N	– 1	16	16			Electrically Selectable Diff/SE	
Offset TC	TCV _{OS}	– 1	1.5		1.5		V _{IN} = 0V	± ppm/°C max
Gain TC	TCA _E	– 1	2.0		2.0		± V _{IN} = ± 10V	± ppm/°C max
Input Fault Current	I _F	– 1	20				± V _{IN} = ± 15V	mA max
Noise Error	EN	– 1	0.5				0.1 to 10MHz	mV pk-pk max
Noise Error Over Temperature	EN	– 1	1				0.1 to 10MHz – 55°C to + 125°C	mV pk-pk max
Aperture Delay	t _{AD}	– 1	100				50ns typ	ns max
Aperture Uncertainty	t _{AU}	– 1	500				100ps typ	ps max
Acquisition Time	t _{ACQ}	– 1	18				20V Step to 0.01% (10μs typ)	μs max
Feedthrough in Hold Mode	FT	– 1	– 70				20V pk-pk @ 1kHz	dB max
Digital Inputs (28-31)	V _{LOGIC}	– 1	1				TTL Compatible	LSTTL Loads max
Digital Input (Pin 1)	D _{INCH}	– 1	3				CMOS Compatible	TTL Loads max
T/H Input (Pin 13)	D _{INTH}	– 1	2				TTL Compatible	TTL Load max
Latch Input (Pin 32)	D _{INLCH}	– 1	8				TTL Compatible	LSTTL Loads max
Power Dissipation	P _D	– 1	800				No Load	mW max

NOTE.

¹T_A = +25°C and V_{CC} = ±15V, V_{DD} = +5V unless otherwise noted.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

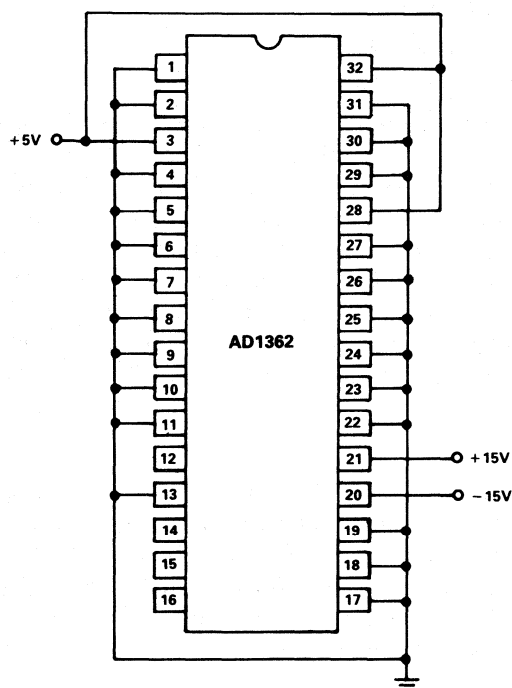


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Input Range.

The analog input range is $\pm 10\text{V FS}$ as specified in Table 1. When $\pm 12\text{V}$ supplies are used, the linear input range must be limited to $\pm 5\text{V FS max}$. Unused channels must be terminated at analog common or thru a resistive load to a stable voltage.

5.1 Offset Adjust.

The offset error is adjustable to zero using the circuit shown in Figure 1. The offset voltage of the AD1362 may be adjusted at either the Analog Input or ADC sections. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small ($<10\text{mV}$) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 1 is recommended. Under normal conditions all calibration is performed at the ADC section.

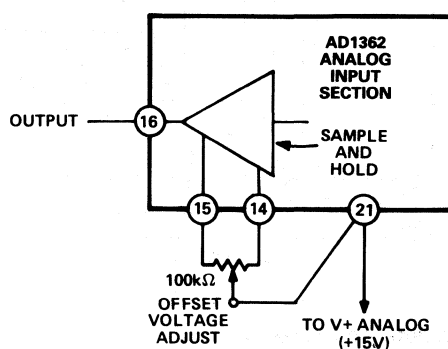


Figure 1. Analog Input Section Offset Voltage Adjustment

5.2 Digital Control Signals.

Single-Ended/Differential Mode Control

The AD1362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to Pin 1 of the Analog Input Section:

- “0”: Single-Ended (SE) (16 channels)
- “1”: Differential (DIFF) (8 channels)

When in the differential mode, a differential source may be applied between corresponding “High” and “Low” analog input channels. It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within $\pm 0.01\%$ of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the “Hold” mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding “High” and “Low” analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 2 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Pins 28-31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic “1”. Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS			ON CHANNEL (Pin Number)		
A2	A1	A0	Single Ended	Differential "Hi" "Lo"	
0	0	0	0 (11)	None	
0	0	1	1 (10)	None	
0	1	0	2 (9)	None	
0	1	1	3 (8)	None	
1	0	0	4 (7)	None	
1	0	1	5 (6)	None	
1	1	0	6 (5)	None	
1	1	1	7 (4)	None	
0	0	0	8 (27)	0 (11)	0 (27)
0	0	1	9 (26)	1 (10)	1 (26)
0	1	0	10 (25)	2 (9)	2 (25)
0	1	1	11 (24)	3 (8)	3 (24)
1	0	0	12 (23)	4 (7)	5 (23)
1	0	1	13 (22)	5 (6)	5 (22)
1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	15 (18)	7 (4)	7 (18)

Table 2. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within $\pm 0.01\%$ of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD1362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (Pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered). This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Pin 13) is normally connected to the Status output (Pin 20) from an analog-to-digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within $\pm 0.01\%$ of the final value before a new Convert Start command is issued.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Pin 17) and Digital Ground (Pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD1362 as possible. The lid is connected to Analog Ground to provide electrostatic shielding. If the grounds are not tied common on the same card with the AD1362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes. This will protect the AD1362 from possible damage caused by voltages in excess of ± 1 volt between the ground systems which could occur if the

key grounding card should be removed from the overall system. The device will operate properly with as much as $\pm 20\text{mV}$ between grounds, however this difference will be reflected directly as an input offset voltage.

Power Supply Bypassing: The $\pm 15\text{V}$ and $+5\text{V}$ power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. $1\mu\text{F}$ tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a $0.039\mu\text{F}$ ceramic capacitor.

Hold Capacitor

An internal 1500pF hold capacitor is included within the AD1362. Applications upgrading from the AD362, in which Pin 12 is the connection for an external hold capacitor, do not require removal of this capacitor since Pin 12 is not connected internally in the AD1362.

5.3 System Timing & Operation.

Interfacing to Popular Analog-to-Digital Converters

The AD1362 has been designed to interface directly to most analog-to-digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

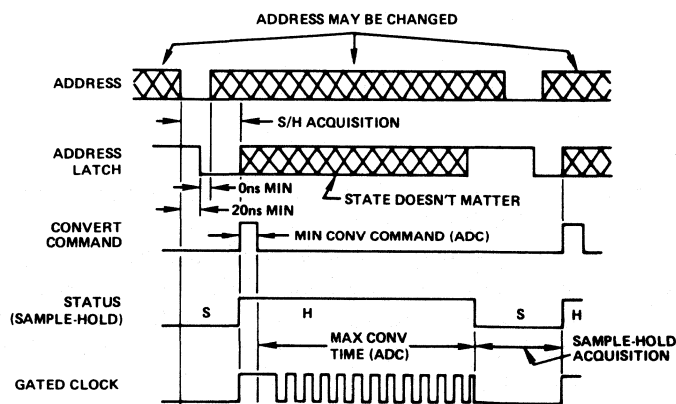


Figure 2. DAS Timing Diagram

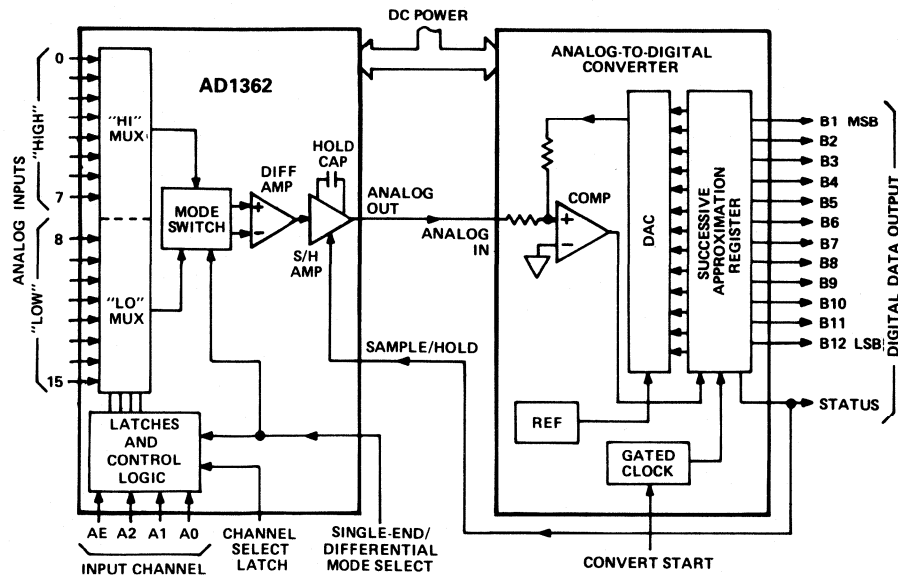


Figure 3. AD1362 with ADC as a Complete Data Acquisition

Figure 2 is a timing diagram for the AD1362 connected as shown in Figure 3 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12-bit type such as the AD573.

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data), the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

1.1 Scope.

This specification covers the detail requirements for a hybrid, fast, 16-bit successive approximation analog-to-digital converter including internal clock reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD1378SD/883B
-2	AD1378TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32E.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Logic Supply Voltage	$+7\text{ V}$
Analog Inputs (Pins 24 & 25)	$\pm 25\text{ V}$
Digital Inputs	$+5.5\text{ V}$
Junction Temperature	$+175^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 12^\circ\text{C/W}$
 $\theta_{JA} = 38^\circ\text{C/W}$

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Conditions ¹	Units
Analog Input Voltage Ranges	V _{IN}	–1, 2	±5, ±10 0 to +10 0 to +20					V
Input Impedance 0 to +5 V, ±2.5 V 0 to +10 V, ±5 V 0 to +20 V, ±10 V	R _{IN}	–1, 2	1.88 3.75 7.50					kΩ typ
Gain Error	V _{GE}	–1, 2	0.15	0.15			10 V Unipolar 20 V Bipolar	±%/FSR max
Gain Drift	V _{GD}	–1, 2	15		15		10 V Unipolar 20 V Bipolar	±ppm/°C max
Unipolar Offset Error	V _{OSE}	–1, 2	0.1	0.1			10 V Unipolar	±%/FSR max
Unipolar Offset Drift	V _{OSD}	–1, 2	4		4		10 V Unipolar	±ppm/°C max
Bipolar Offset Error	V _{OSE}	–1, 2	0.2	0.2			20 V Bipolar	±%/FSR max
Bipolar Offset Drift	V _{OSD}	–1, 2	10		10		20 V Bipolar	±ppm/°C max
Linearity Error	RA	–1	0.006	0.006		0.006	10 V Unipolar 20 V Bipolar	±%/FSR max
		–2	0.003	0.003		0.003	10 V Unipolar 20 V Bipolar	
Linearity Drift	L _D	–1	3		3		10 V Unipolar 20 V Bipolar	±ppm/°C max
		–2	2		2		10 V Unipolar 20 V Bipolar	
Differential Linearity Error	DNL	–1	2	2	2	2	10 V Unipolar 20 V Bipolar	±LSB ₁₄ max
		–2 ²	1	1	1	1	10 V Unipolar 20 V Bipolar	
+5 V Power Supply Sensitivity	PSRR	–1, 2	0.003	0.003			±5%	±%/V _S max
±15 V Power Supply Sensitivity	PSRR	–1, 2	0.005	0.005			±5%	±%/V _S max
Digital Output High Drive	V _{OH}	–1, 2	2.4	2.4			@ –100 μA	V min
Digital Output Low Drive	V _{OL}	–1, 2	0.4	0.4			@ 2.0 mA	V max
Digital Input Current Low Level	I _{INL}	–1, 2	–0.4	–0.4			V _{INL} = 0.4 V	mA max
Digital Input Current High Level	I _{INH}	–1, 2	0.02	0.02			V _{INH} = 2.7 V	mA max
Conversion Speed	t _C	–1, 2	17 15	17 15			16 Bit 14 Bit	μs max
+5 V Supply Drain	+I _{DD}	–1, 2	25		25			mA max
+15 V Supply Drain	+I _{CC}	–1, 2	25		25			mA max
–15 V Supply Drain	–I _{CC}	–1, 2	–40		–40			mA max
Power Dissipation	P _D	–1, 2	800		800			mW max
Power Supply Range	+V _{DD} ±V _{CC}	–1, 2	+5 ±15				±5% ±5%	V

NOTES

¹V_{CC} = ±15 V, V_{DD} = +5 V, T_A = +25°C unless otherwise noted.

²Guaranteed no missing codes –55°C to +125°C.

Table 1.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REV. A

6.0 Gain and Offset Adjustment.

Gain Adjustment

The gain adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300 k Ω resistor to the gain adjust Pin 29 as shown in Figure 1.

If no external trim adjustment is desired, Pin 27 (OFFSET ADJ) and Pin 29 (GAIN ADJ) may be left open.

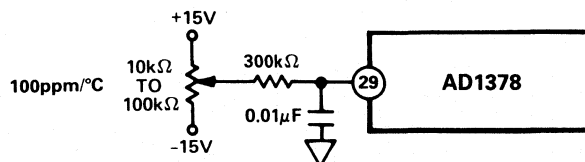


Figure 1. Gain Adjustment Circuit ($\pm 0.15\%$ FSR)

Offset Adjustment

The zero adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 M Ω resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 2, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200 ppm/°C tempco contributes a worst-case offset tempco of $32 \text{ LSB}_{14} \times 61 \text{ ppm/LSB}_{14} \times 1200 \text{ ppm/°C} = 2.3 \text{ ppm/°C}$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16 \text{ LSB}_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

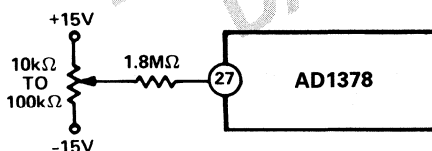


Figure 2. Offset Adjustment Circuit ($\pm 0.3\%$ FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 3.

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. (Comparator Input Pin 27 is quite sensitive to external noise pickup and should be guarded by analog common.)

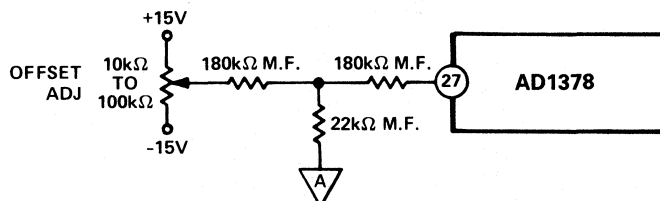


Figure 3. Low Tempco Zero Adjustment Circuit

6.1 Input Scaling.

The AD1378 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table 2. See Figure 4 for circuit details.

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
± 10 V	COB	27	Input Signal	24
± 5 V	COB	27	Open	25
± 2.5 V	COB	27	Pin 27	25
0 V to +5 V	CSB	22	Pin 27	25
0 V to +10 V	CSB	22	Open	25
0 V to +20 V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

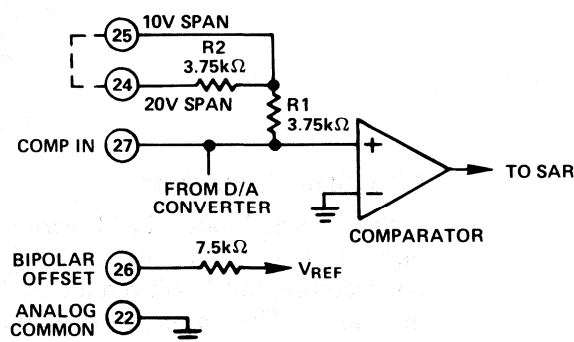


Table 2. AD1378 Input Scaling Connections

Figure 4. AD1378 Input Scaling Circuit

6.2 Digital Output Data.

Parallel data from TTL storage registers is in negative true form (Logic "1" = 0 V and Logic "0" = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data outputs change state on positive-going clock edges.

Analog Input Voltage Range		± 10 V	± 5 V	± 2.5 V	0 V to +10 V	0 V to +5 V
Code Designation		COB* or CTC**	COB* or CTC**	COB or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20 \text{ V}}{2^n}$	$\frac{10 \text{ V}}{2^n}$	$\frac{5 \text{ V}}{2^n}$	$\frac{10 \text{ V}}{2^n}$	$\frac{5 \text{ V}}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

NOTES

*COB = Complementary Offset Binary.

**CTC = Complementary Twos Complement – achieved by using an inverter to complement the most significant bit to produce (MSB).

***CSB = Complementary Straight Binary.

Table 3. Input Voltage Range and LSB Values

6.3 Clock Rate Control.

The AD1378 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multitrans trim potentiometer (TCR <100 ppm/°C) as shown in Figure 5. The integral linearity and differential linearity errors will vary with speed.

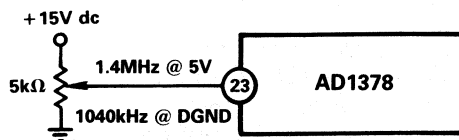


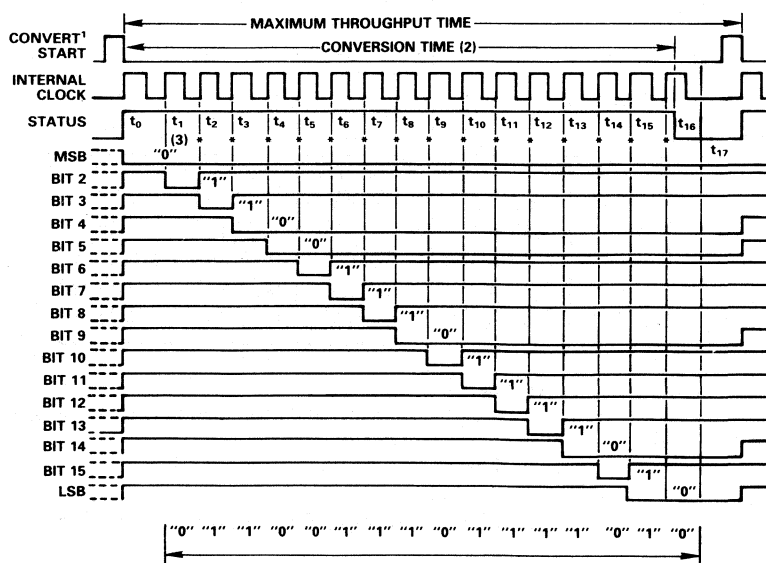
Figure 5. Clock Rate Control Circuit

6.3.1 Short Cycle Input.

A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 6 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flat resets after the Bit 10 decision (timing diagram of Figure 6). Short cycle connections and associated 8-, 10-, 12-, 13-, 14- and 15-bit conversion times are summarized in Table 4, for a 933 kHz clock.

Resolution Bits	(% FSR)	Maximum Conversion Time (μs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	17.1	t ₁₆	N/C (Open)
15	0.003	16.1	t ₁₅	16
14	0.006	15.0	t ₁₄	15
13	0.012	13.9	t ₁₃	14
12	0.024	12.9	t ₁₂	13
10	0.100	10.7	t ₁₀	11
8	0.390	8.6	t ₈	9

Table 4. Short Cycle Connections



NOTES:

1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 15μs FOR 14 BITS AND 14μs FOR 13 BITS (MAX).
3. MSB DECISION.
4. CLOCK REMAINS LOW AFTER LAST BIT DECISION.

Figure 6. Timing Diagram (Binary Code 0110011101110110)

REV. A

AD2700/AD2701/AD2702
1.1 Scope.

This specification covers the detail requirements for a hybrid precision voltage reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD2700SD/883B
-2	AD2700UD/883B
-3	AD2701SD/883B
-4	AD2701UD/883B
-5	AD2702SD/883B
-6	AD2702UD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-14C.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage ($+V_{IN}$)	-1		+20 V
	-2		+20 V
	-5		+20 V
	-6		+20 V
Supply Voltage ($-V_{IN}$)	-3		-20 V
	-4		-20 V
	-5		-20 V
	-6		-20 V
10 V Short Circuit Protection (to GND)			Continuous
Storage Temperature Range			-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)			$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 7^\circ\text{C/W}$
 $\theta_{JA} = 20^\circ\text{C/W}$

AD2700/AD2701/AD2702 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 7	Test Condition ¹	Units
Quiescent No Load Current	I_{CC}	-1, 2	14	14			$V_{CC} = +15\text{ V}$ No Load	+mA max
	I_{EE}	-3, 4	14	14			$V_{EE} = -15\text{ V}$ No Load	-mA max
	I_{CC}	-5, 6	17	17			$V_{CC} = +15\text{ V}$ $V_{EE} = -15\text{ V}$ No Load	+mA max
	I_{EE}	-5, 6	4	4			$V_{CC} = +15\text{ V}$ $V_{EE} = -15\text{ V}$ No Load	-mA max
Interim Output Error Initial End-Point Delta Limits	$+V_{RINT}$	-1, 2 -5, 6	5 10 5	5 10 5			+10.000 V Output	±mV max
Interim Output Error Initial End-Point Delta Limits	$-V_{RINT}$	-3, 4 -5, 6	5 10 5	5 10 5			-10.000 V Output	±mV max
Selection Output Error ²	$+V_R$	-1	5.0		8.0	5.0	+10.000 V Output	±mV max
	$+V_R$	-2, 6	2.5		5.5	2.5	+10.000 V Output	±mV max
	$+V_R$	-5	5.0		10.0	5.0	+10.000 V Output	±mV max
	$-V_R$	-3	5.0		8.0	5.0	-10.000 V Output	±mV max
	$-V_R$	-5	5.0		10.0	5.0	-10.000 V Output	±mV max
	$-V_R$	-4, 6	2.5		5.5	2.5	-10.000 V Output	±mV max
Positive Output Line Regulation	$+V_{RLINE}$	-1, 2 -5, 6	900	900			+10 V Output @ $V_{CC} = +13.5\text{ V}$ to +16.5 V	±μV max
Negative Output Line Regulation	$-V_{RLINE}$	-3, 4 -5, 6	900	900			-10 V Output @ $V_{EE} = -13.5\text{ V}$ to -16.5 V	±μV max
Positive Output Load Regulation	$+V_{RLOAD}$	-1, 2 -5, 6	500	500			+10 V Output @ 0 to 10 mA Load Change	±μV max
Negative Output Load Regulation	$-V_{RLOAD}$	-3, 4 -5, 6	500	500			-10 V Output @ 0 to 10 mA Load Change	±μV max
Positive Output Adjust Range ³	$+V_{RADJ}$	-1, 2 -5, 6	20	20			@ +10 V Output	±mV min
Negative Output Adjust Range ³	$-V_{RADJ}$	-3, 4 -5, 6	20	20			@ -10 V Output	±mV min
Output Current	$+I_L$ $-I_L$	-1, 2 -3, 4 -5, 6	10	10	5		Thru a Resistive Load Tied to Pin 7, Common	±mA min

NOTES

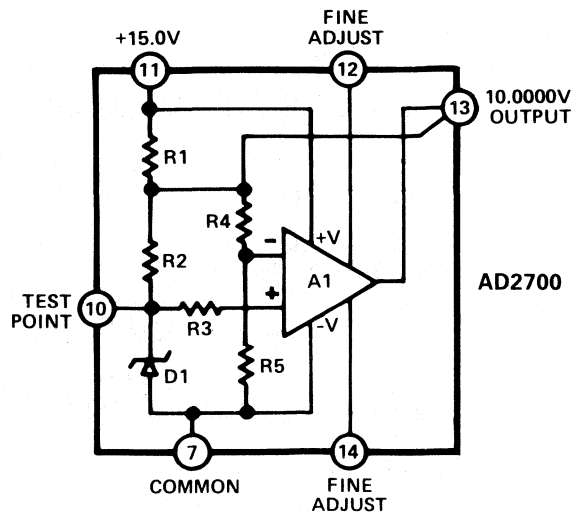
¹ $T_A = +25^\circ\text{C}$, $V_S = +15\text{ V}$ unless otherwise specified. All tests, after 3 minute warm-up period, at +15 V supplies and 2 kΩ load to common unless otherwise specified. All measurements are referenced to Pin 7 of the device.

²Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min} , T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C.

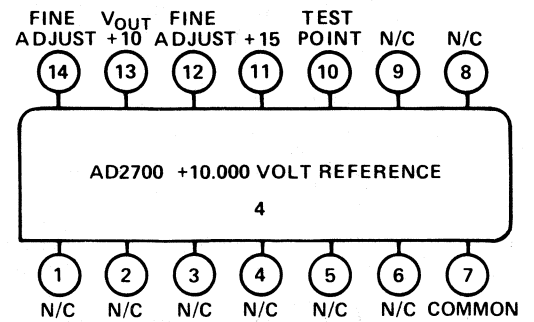
³See Figure 1 for trim circuits.

Table 1.

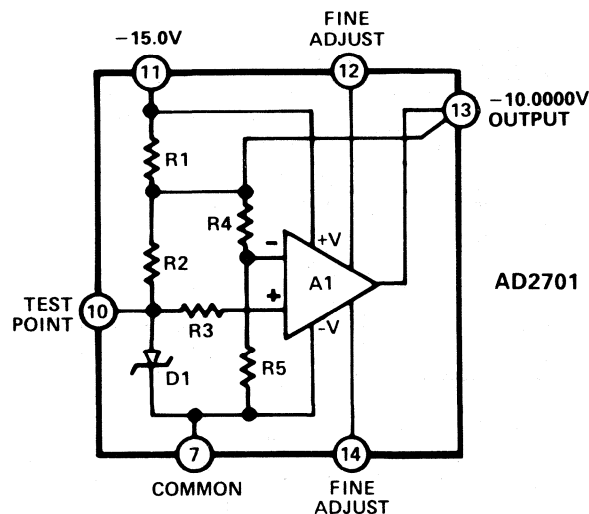
3.2.1 Functional Block Diagram and Terminal Assignments.



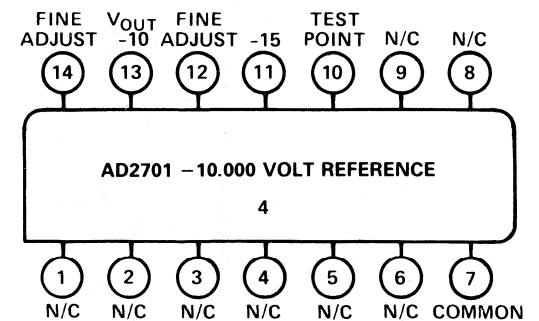
Device Type -1, -2



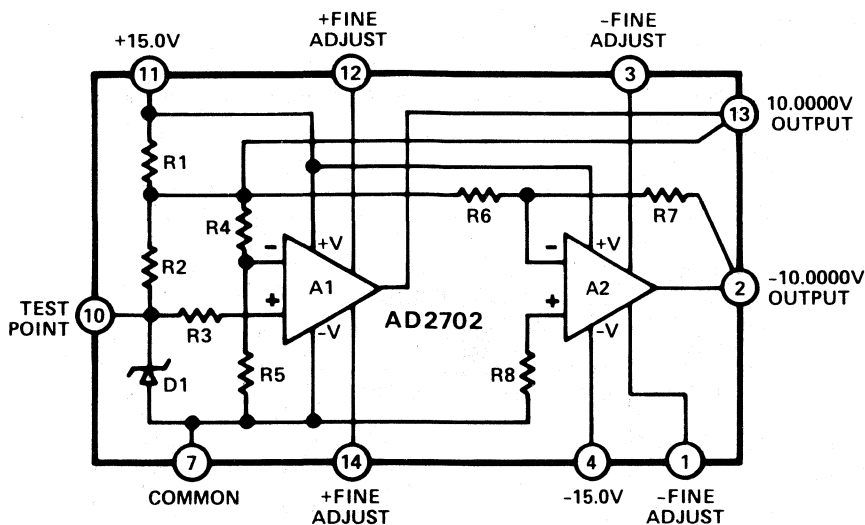
Device Type -1, -2



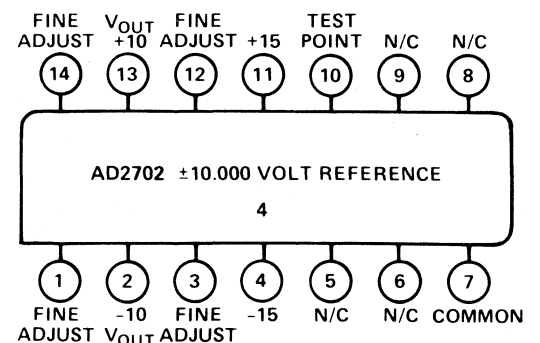
Device Type -3, -4



Device Type -3, -4



Device Type -5, -6



Device Type -5, -6

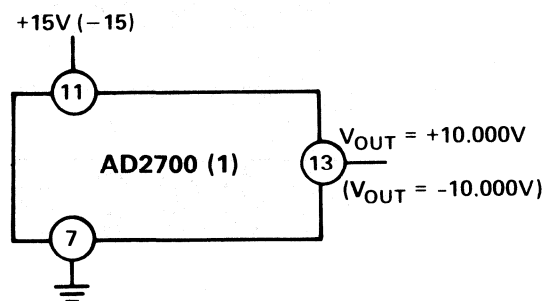
AD2700/AD2701/AD2702

3.2.4 Microcircuit Technology Group.

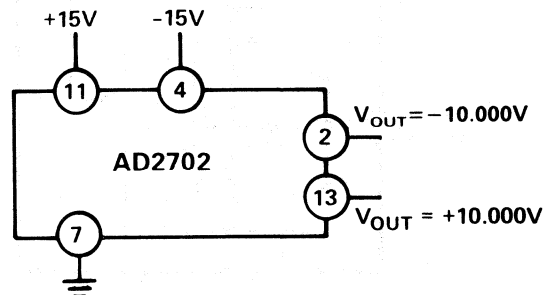
This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

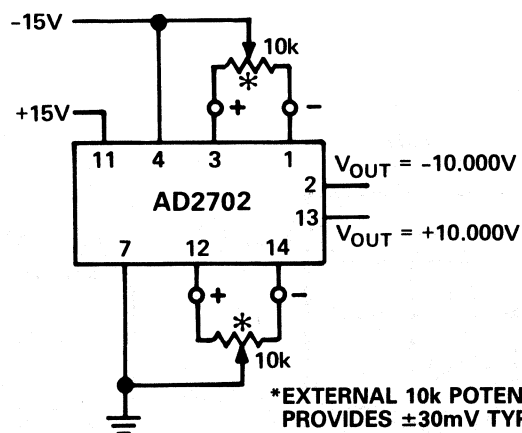
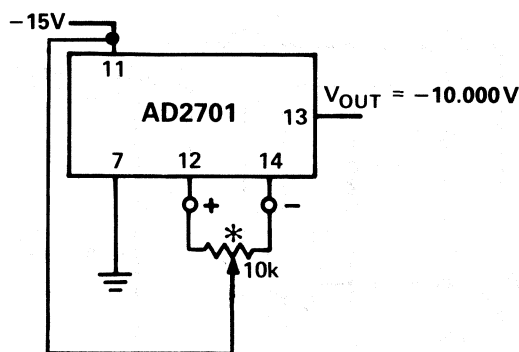
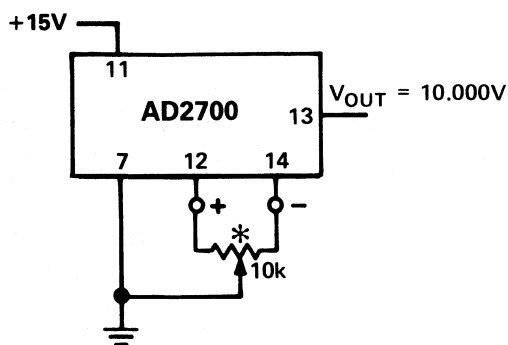
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Device Type -1, -2, (3), (4)



Device Type -5, -6



*EXTERNAL 10k POTENTIOMETER PROVIDES $\pm 30\text{mV}$ TYPICAL OUTPUT OFFSET ADJUST. TEMPERATURE EFFECT IS $\pm 4\mu\text{V}/^\circ\text{C}$ PER mV OF OFFSET CORRECTION TYPICAL (EXTERNAL ADJUSTMENT OPTIONAL).

Figure 1. Fine Trim Connections

1.1 Scope.

This specification covers the detail requirements for a hybrid, buffered, digital-to-analog converter with voltage output.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD3860SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-24B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Single Voltage $+V_S$		+18 V max
$-V_S$		–18 V max
$+V_{\text{LOGIC}}$		+7 V max
V_{IN} Digital V_{INL}		0 to $+V_{\text{LOGIC}}$
Short Circuit Protection to GND		Continuous
Storage Temperature Range		–65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	= 8°C/W
θ_{JA}	= 25°C/W

AD3860 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C (–55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1	2.0 (2.0)					V min
Digital Input Low Voltage	V _{IL}	–1	0.8 (0.8)					V max
Digital Input High Current	I _{IH}	–1	30 (30) 60 (60)			30	Data Inputs @ 2.0 V Register Input @ 2.0 V	μA max
Digital Input Low Current	I _{IL}	–1	600 (600) 1200 (1200)			600	Data Inputs @ 0.8 V Register Enable @ 0.8 V	μA max
Gain Error	A _E	–1	0.1	0.1			V _O = +FS, ±10 V Range	±% FSR max
Gain Error Temperature Coefficient	TCA _E	–1	(0.3)		0.3		V _O = +FS, ±10 V Range	±% FSR max
Unipolar Gain Error	V _{UGE}	–1	0.1	0.1			V _O = +FS 0 to 10 V Range	±% FSR max
Unipolar Gain Drift	V _{UGD}	–1	(0.3)		0.3		V _O = +FS 0 to 10 V Range	±% FSR max
Unipolar Offset Error	V _{OS}	–1	0.05	0.05			V _O = 0 V, +10 V Range	±% FSR max
Unipolar Offset Error Temperature Coefficient	TCV _{OS}	–1	(0.1)		0.1		Over Operating Temperature	±% FSR max
Bipolar Gain Error	V _{BGE}	–1	0.1	0.1			V _O = +FS, ±10 V Range	±% FSR max
Bipolar Gain Drift	V _{BGD}	–1	(0.3)		0.3		V _O = +FS, ±10 V Range	±% FSR max
Bipolar Offset Error	B _{POS}	–1	0.05	0.05			V _O = –FS, ±10 V Range	±% FSR max
Bipolar Offset Error Temperature Coefficient	TCB _{POS}	–1	(0.1)		0.1		V _O = –FS, ±10 V Range	±% FSR max
Bipolar Zero Error	B _{PZ}	–1	0.1				V _O = 0 V, ±10 V Range	±% FSR max
Bipolar Zero Error Temperature Coefficient	TCP _{PZ}	–1	(0.3)				V _O = 0 V, ±10 V Range	±% FSR max
Integral Nonlinearity	L _E	–1	1/2 (1/2)	1/2	1/2		Linearity ±10 V Range	±LSB max
Differential Nonlinearity Error	D _{LE}	–1	1 (1)	1	1		Monotonic Over Temperature	±LSB max
Output Voltage Range, Ideal	V _{OUT}	–1	+9.9952 (9.9952) –10.000 (–10.000)				±10 V Range	V Ideal
Output Current	I _{OUT}	–1	5.0 (5.0)			5.0	±10 V Range C _L = 250 pF, R _L = 2 kΩ	mA min
Input Resistance	R _{IN}	–1	N/A					
Reference Output Voltage Error	V _{REFER}	–1	126 126	126 126			Error @ No Load Error @ 2.5 mA Load	±mV max
Reference Output Voltage ² Temperature Coefficient	TCV _{REF}	–1	(126) (126)		126 126		Error @ No Load Error @ 2.5 mA Load	±mV max
Reference Output Current	I _{REF}	–1	2.5				For External Use	mA min
Slew Rate	V _{SL}	–1	10 (10)				±10 V Range	V/μs min
Output Voltage Settling Time	t _{SL}	–1	7 (7) 5 (5)				±10 V Range, 20 V Step ±5 V Range, 10 V Step	μs max
DC Feedthrough Error	FTE	–1	1	1			Latch @ +FS then Change to Offset	±mV max
DC Feedthrough Error Over Temperature	TCFTE	–1	(1)		1		Latch @ +FS then Change to Offset	±mV max

Table 1. (Continued on next page)

REV.C

Test	Symbol	Device	Design Limit @ +25°C (−55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Output Short Circuit Current	I_{SC}	−1	25 (25)					mA max
Power Supply Rejection Ratio	PSRR	−1	0.01 0.004	0.01 0.004	0.01 0.004		+15 V, ±0.5 V −15 V, ±0.5 V	±% FSR/% V_S max
Power Supply Current	I_{CC} I_{EE} I_{DD}	−1	+20 (+20) −30 (−30) +50 (+50)	+20 −30 +50	+20 −30 +50		+15 V_{CC} −15 V_{EE} +5 V_{LOGIC}	mA max
Power Dissipation	P_D	−1	1000 (1000)					mW max
Write Pulse Width	t_{NEPW}	−1	60					ns min
Data Setup Time	t_{SDE}	−1	40					ns min
Data Hold Time	t_{DH}	−1	10					ns min

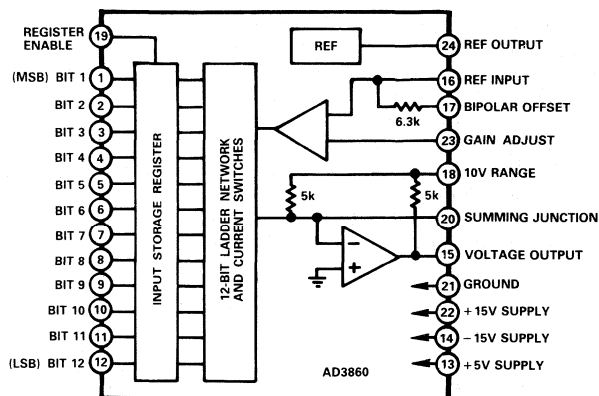
NOTES

¹Specified and tested at +25°C, ±15 V, +5 V, ±10 V range, no load conditions, internal reference unless noted otherwise in the table.

² $V_{REF} = +6.300$ V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

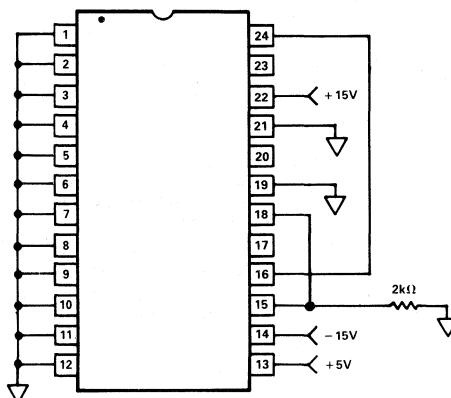


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



6.0 Output Range.

The analog input range is as specified in Table 2 when externally connected as shown in Table 3 below. The output range must be limited to ± 5 V full scale when operated with ± 12 V supplies.

OUTPUT VOLTAGE RANGE SELECTION

Output Range	0 to +10 V	± 5 V	± 10 V
Pin Connection			
Connect Pin 24 to	16	16	16
Connect Pin 17 to	21	20	20
Connect Pin 15 to	18	18	NC
Connect Pin 20 to	NC	17	17

Table 2.

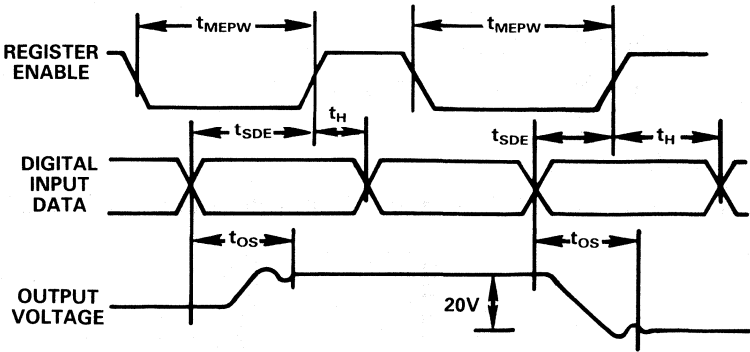
INPUT LOGIC CODING

Digital Input MSB LSB	Analog Output		
	0 to +10 V	± 5 V	± 10 V
0000 0000 0000	+9.9976 V	+4.9976 V	+9.9951 V
0000 0000 0001	+9.9951 V	+4.9951 V	+9.9902 V
0111 1111 1111	+5.0000 V	0.0000 V	0.0000 V
1000 0000 0000	+4.9976 V	-0.0024 V	-0.0049 V
1111 1111 1110	+0.0024 V	-4.9976 V	-9.9951 V
1111 1111 1111	0.0000 V	-5.0000 V	-10.0000 V

CODING NOTES:

- 1. For unipolar operation, the coding is complementary straight binary (CSB).
- 2. For bipolar operation, the coding is complementary offset binary (COB).
- 3. For FSR = 20 V, 1 LSB = 4.88 mV.
- 4. For FSR = 10 V, 1 LSB = 2.44 mV.

Table 3.



TIMING NOTES:

- t_{MEPW} MINIMUM ENABLE PULSE WIDTH IS 60 ns.
- t_{SDE} MINIMUM SETUP TIME DIGITAL INPUT DATA TO ENABLE IS 40 ns.
- t_H HOLD TIME IS DEFINED AS THE REQUIRED DELAY BETWEEN THE LEADING EDGE OF REGISTER ENABLE AND THE END OF VALID INPUT DATA AND IS 10 ns.
- t_{OS} OUTPUT SETTLING TIME FOR A 20 VOLT CHANGE TO $\pm 1/2$ LSB IS 7 μ s MAX.

Figure 1. Input Register Timing Diagram



12-Bit Successive Approximation High Accuracy A/D Converter

AD5200/AD5210 Series

1.1 Scope.

This specification covers the detail requirements for hybrid, 12-bit, successive approximation, high accuracy, analog-to-digital converters.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

	Device	(50 μ s Version) Part Number	Device	(13 μ s Version) Part Number
± 5 V Int Ref	-03	AD5201TD/883B	-11	AD5211TD/883B
± 5 V Ext Ref	-04	AD5204TD/883B	-12	AD5214TD/883B
± 10 V Int Ref	-05	AD5202TD/883B	-13	AD5212TD/883B
± 10 V Ext Ref	-06	AD5205TD/883B	-14	AD5215TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000:

Device Type	Package Outline
-03, -04	DH-24E
-05, -06	
-11, -12	DH-24E
-13, -14	

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage ($+V_{CC}$)	+18V
Negative Supply Voltage ($-V_{EE}$)	-18V
Logic Supply Voltage ($+V_{DD}$)	+7V
Analog Input Voltage	± 25 V
Digital Input Voltage	+5.5V
Reference Input Voltage	0 to -15V
(Ext. Ref versions only)	
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	+300 $^\circ\text{C}$
Junction Temperature	+175 $^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 5^\circ\text{C/W}$
 $\theta_{JA} = 40^\circ\text{C/W}$

AD5200/AD5210 Series – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Analog Input Voltage Ranges	V _{IN}	– 3, 11	± 5				Internal Reference	V FS
		– 4, 12					Ext. – 10.000 V _{REF}	
	V _{IN}	– 5, 13	± 10				Internal Reference	V FS
		– 6, 14					Ext. – 10.000 V _{REF}	
Linearity Error	L _E	All	1/2	1/2	1/2		At Major Carries (Abbreviated Test)	± LSB max
Differential Linearity Error ²	DNL	All	0.9	0.9	0.9		At Major Carries	± LSB max
Zero Error	Z _E	All	1	1	2		V _{IN} = 0V	± LSB max
± FS Absolute Accuracy Error Over Temperature	TC _{AE}	– 3, 5, 11, 13	0.4		0.4		With Internal Reference	± % FSR max
		– 4, 6, 12, 14	0.1		0.1		With Ext. – 10.000 V _{REF}	± % FSR max
± FS Absolute Accuracy Error @ +25°C	A _E	All	2	2			With Ext. – 10.000 V _{REF} on Ext. Ref. Versions	± LSB max
Conversion Time	t _{CONV}	– 11, 12, 13, 14	13	13			With 1MHz	μs max
	t _{CONV}	– 3, 4, 5, 6	50	50			With 260kHz Clock	μs max
Serial/Parallel Code Error Match	SP _{CM}	All	0	0			Random	± Bits
Logic Inputs	I _{INL} I _{INH} I _{INH}	All	0.6 0.04 1.0	0.6 0.04 1.0			V _{INL} = 0.3V V _{INH} = 2.4V V _{INH} = 5.5V	mA max
Logic Outputs	V _{OL} V _{OH}		0.4 2.4	0.4 2.4			I _{OL} = 3.2mA I _{OH} = – 80μA	V max V min
Short Circuit Current	I _{SC}		16	16			@ 0V	mA min
Clock Input Pulse Width	t _{CW}	All	100	100				ns min
Power Supply Rejection	PSRR	All	0.005			0.005	All Supplies ± 3% Variation	%/% max
Power Supply Current	I _{CC}	– 3, 4, 5, 6	28	28				mA max
	I _{EE}		35	35				
	I _{LOGIC}		68	68				
	I _{CC} I _{EE} I _{LOGIC}	– 11, 12, 13, 14	28 35 68	28 35 68				mA max
Power Supplies	V _{CC} V _{EE} V _{LOGIC}	All	+ 15 ± 10% – 15 ± 10% + 5 ± 10%					V
Power Dissipation	PD	– 4, 6, 12, 14	0.8			0.8		Watts max
		– 3, 5, 11, 13	1.0			1.0		

NOTES

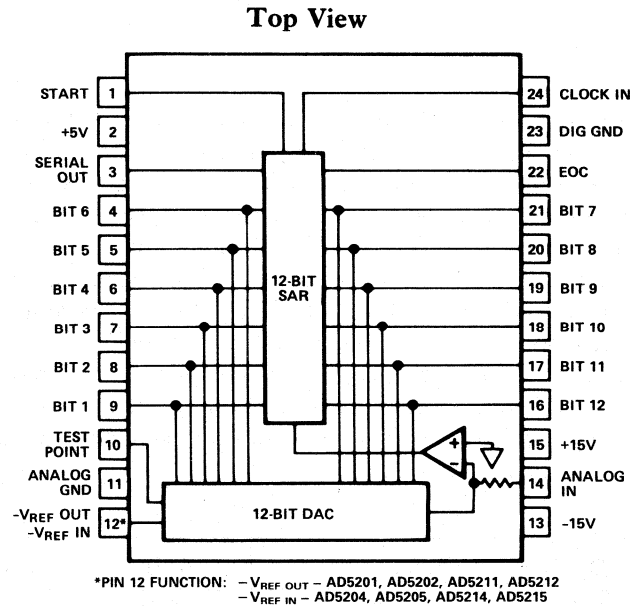
¹T_A = +25°C, V_{CC} = ± 15V, V_{DD} = +5V unless otherwise noted.

²Guaranteed no missing codes.

Table 1.

AD5200/AD5210 Series

3.2.1 Functional Block Diagram and Terminal Assignments.

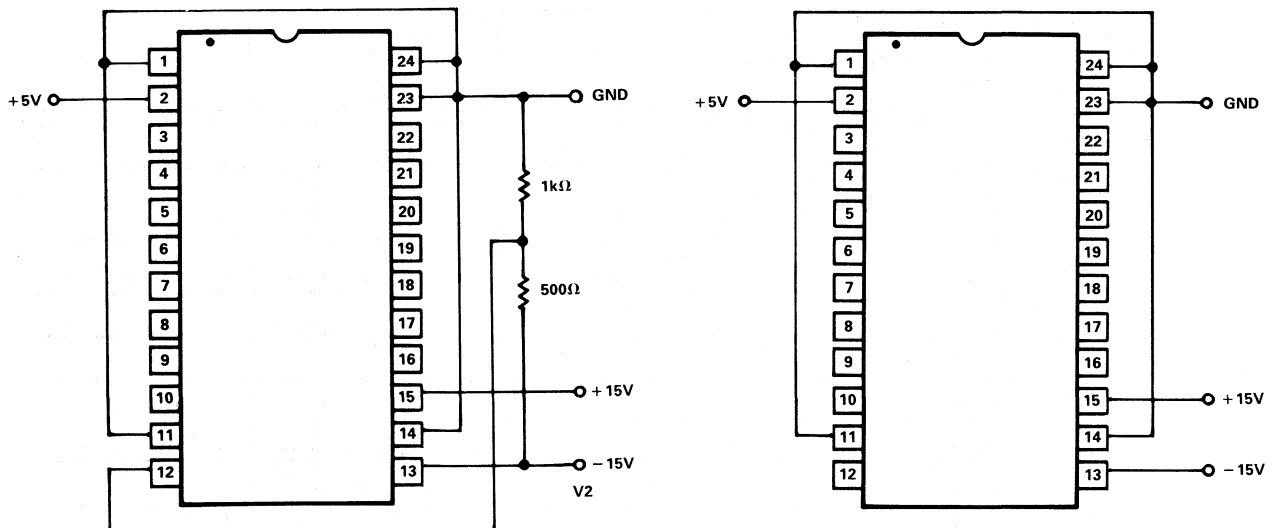


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Devices 04, 06, 12, 14

Devices 03, 05, 11, 13

AD5200/AD5210 Series

6.0 Input Range.

The analog input range for each device is specified in Table 1.

6.1 Digital Output Data.

Both parallel and serial data from TTL storage registers are in negative true form using complementary offset binary (COB) coding. Parallel data becomes valid approximately 40ns after the EOC STATUS flag returns to Logic “0”, permitting parallel data transfer to be clocked 40ns after the “1” to “0” transition of the EOC STATUS flag on pin 22. Serial data coding is also complementary offset binary (COB) coding. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges and bit decisions we made on following rising clock edges. Serial data is guaranteed valid 200ns after the bit decision, permitting serial data to be clocked directly into a receiving register on the following falling clock edge, if it occurs 200ns after the rising edge. There are 13 negative-going clock edges in the complete 12-bit conversion cycle. Using a 12-bit serial input register, the first edge shifts in an invalid bit into the register, which is shifted out on the 13th negative going clock edge. The digital output codes corresponding to analog input voltage for calibration and test are shown in Table 2 below.

03, 04, 11, 12	05, 06, 13, 14	MSB	LSB
+ 5.0000V	+ 10.000V	0 0 0 0 0 0 0 0 0 0	0
0.0000V	0.000V	1 0 0 0 0 0 0 0 0 0	0
– 4.9976V	– 9.995V	1 1 1 1 1 1 1 1 1 1	1

Table 2. Logic Coding (Complementary Offset Binary)

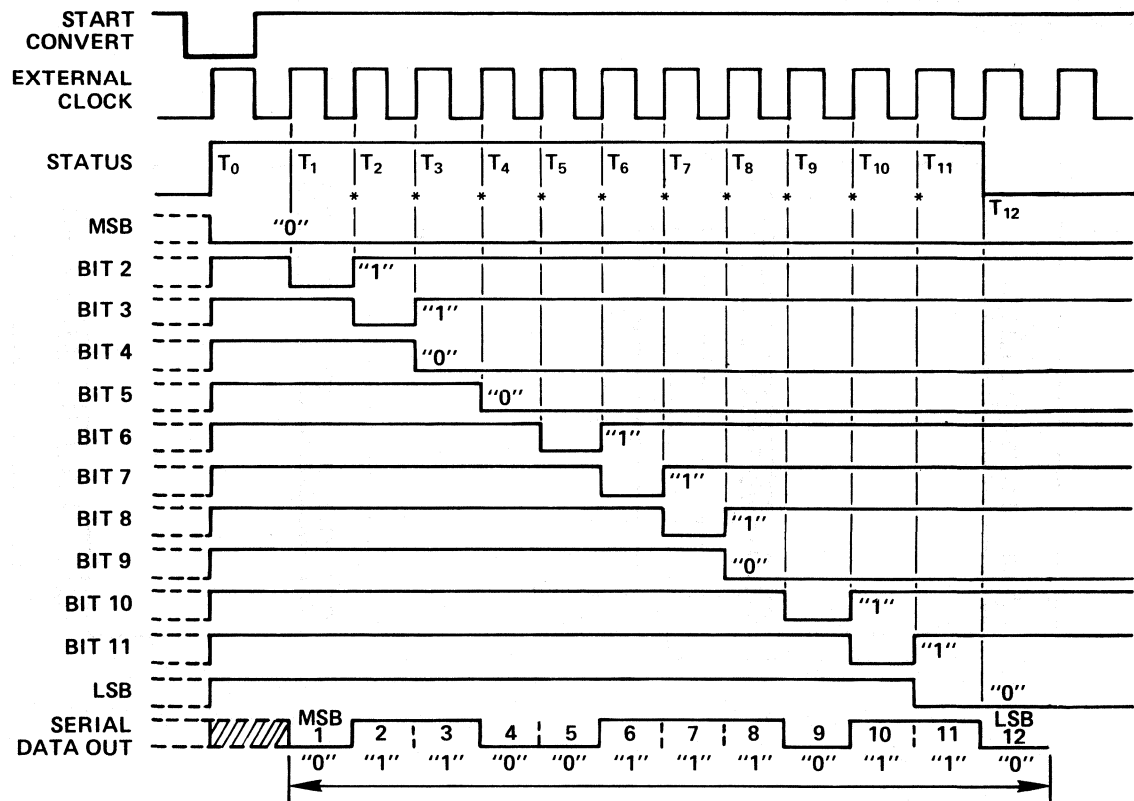


Figure 1. Timing Diagram

1.1 Scope.

This specification covers the detail requirements for a hybrid high speed 12-bit successive approximation analog-to-digital converter including internal clock, reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD5240BD/883B
-2	AD5240ZBD/883B
-3	AD5240SD/883B
-4	AD5240ZSD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32D.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Logic Supply Voltage	$+ 7\text{V}$
Analog Inputs (Pins 24, 25)	$\pm 25\text{V}$
Digital Inputs	$+ 5.5\text{V}$
Junction Temperature	$+ 175^\circ\text{C}$
Storage Temperature Range	$- 65^\circ\text{C}$ to $+ 150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+ 300^\circ\text{C}$

1.3.1 Operating Temperature Range.

The operating temperature range of this device is $- 25^\circ\text{C}$ to $+ 85^\circ\text{C}$ (-1, -2)
 $- 55^\circ\text{C}$ to $+ 125^\circ\text{C}$ (-3, -4).

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 8^\circ\text{C/W}$
 $\theta_{JA} = 38^\circ\text{C/W}$

AD5240 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group ² 2, 3	Sub Group 4	Test Condition ¹	Units
Analog Input Voltage Ranges	V _{IN}	–1, 3	±2.5, ±5, ±10 0 to 5 0 to 10					V
	V _{IN}	–2, 4	±2.5, ±5 0 to 5				±V _{CC} = ±12V +V _{DD} = +5V	V
Serial Parallel Code Match Error	SP _{CM}	–1, 2, 3, 4	0	0			Random Codes	± Bits
Input Impedance	R _{IN}	–1, 2, 3, 4	3			3	±5V Input Range	kΩ min
			7			7		kΩ max
Logic Outputs	V _{OL}	–1, 2, 3, 4	0.4			0.4	I _{OL} = 3.2mA	V max
	V _{OH}	–1, 2, 3, 4	2.4			2.4	I _{OH} = –80μA	V min
Buffer Amp Bias Current	I _B	–1, 2, 3, 4	100			100		± nA max
Buffer Amp Offset Error	B _{OS}	–1, 2, 3, 4	10			10		± mV max
Buffer Amp Common-Mode Rejection	B _{CMR}	–1, 2, 3, 4	70			70		dB min
Buffer Amp Settling Time	t _S	–1, 2, 3, 4	2				To 0.01% for 20V Step	μs max
Reference Output Error	V _{REF}	–1, 2, 3, 4	20	20			6.3V Nominal	± mV max
Reference Voltage Drift	V _{REF}	–1, 2, 3, 4	10		10			± ppm/°C max
Unipolar Gain Error ³	V _{GE}	–1, 2, 3, 4	0.3				0 to +10V Input Range	± % FSR max
Unipolar Offset Error	V _{OSE}	–1, 2, 3, 4	0.1					± % FSR max
Unipolar Offset Drift	V _{OD}	–1, 2, 3, 4	7		7			± ppm/°C max
Bipolar Gain Error ³	V _{GE}	–1, 2, 3, 4	0.4				+10V Input Range	± % FSR max
Bipolar Gain Drift	V _{GD}	–1, 2, 3, 4	25		25		±5V Range	± ppm/°C max
Bipolar Zero Error	B _{PZ}	–1, 2, 3, 4	0.2				±10V Input Range	± % FSR max
Bipolar Zero Drift	V _{BZD}	–1, 2, 3, 4	7		7		±5V Range	± ppm/°C max
Integral Linearity Error Over Temperature	L _E	–1, 2	1/2			1/2	Major Carries & Summations	± LSB max
		–1, 2			2			± ppm/°C max
		–3, 4			3			
Differential Linearity, Error ⁴	D _{LE}	–1, 2, 3, 4	0.75	1	1		Major Carries & Summations	± LSB max
Conversion Speed		–1, 2, 3, 4	5	5			Pin 17 Tied to +5V	μs max
± Power Supply Sensitivity	PSRR ₁	–1, 2, 3, 4	0.004			0.004	V _{CC} = ±13.5V to ±16.5V	± % FSR/ % V _{CC}
± 12V Power Supply Sensitivity	PSRR ₂	–2, 4	0.007				V _{CC} = +11.4V to ±16.5V	± % FSR/ % V _{CC}
+5V Power Supply Sensitivity	PSRR ₃	–1, 2, 3, 4	0.01			0.01	V _{DD} = +4.75V to +5.25V	± % FSR/ % V _{DD}
+15V Supply Drain	–I _{CC}	–1, 2, 3, 4	18			18		mA max
–15V Supply Drain	–I _{CC}	–1, 2, 3, 4	38			38		mA max
+5V Supply Drain	+I _{DD}	–1, 2, 3, 4	60			60		mA max
Power Dissipation	P _D	–1, 2, 3, 4	1450			1450		mW max

NOTES

¹T_A = +25°C and ±V_S = ±15V. V_{DD} = +5V unless otherwise specified.

²Subgroup 2 tests performed @ +85°C.

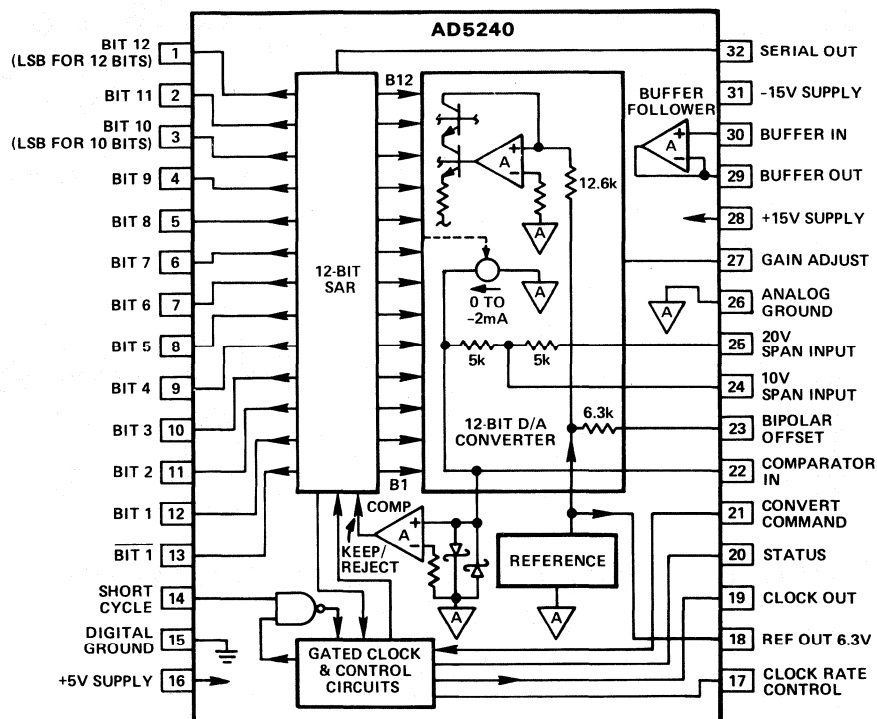
Subgroup 3 tests performed @ –25°C.

³Adjustable to zero.

⁴Guaranteed no missing codes –25°C to +85°C; for device –2, V_{CC} = ±12V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

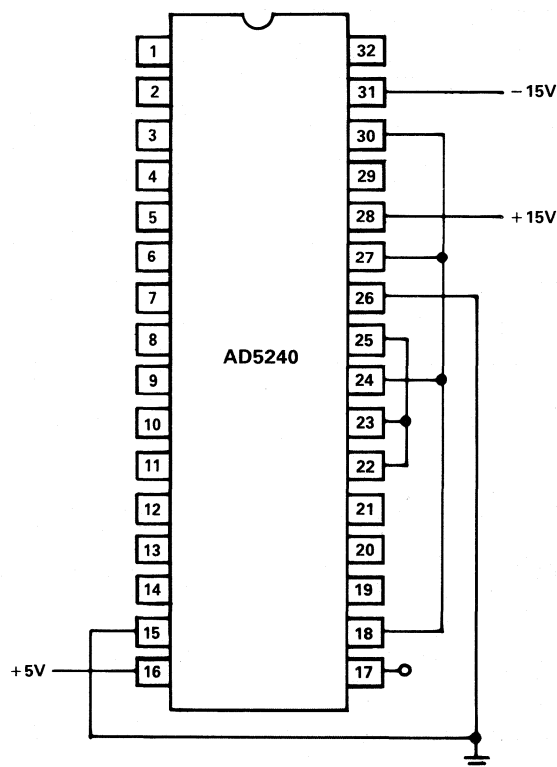


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD5240

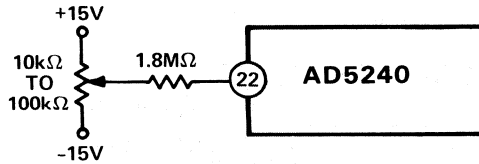


Figure 1. Adjustment Circuit

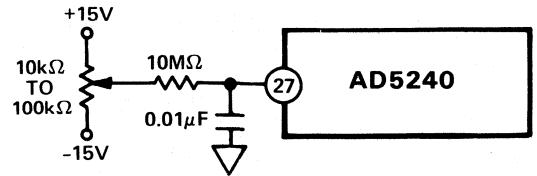


Figure 2. Gain Adjustment Circuit

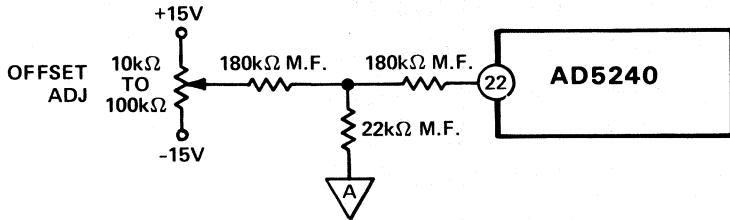


Figure 3. Low Tempco Zero Adjustment Circuit

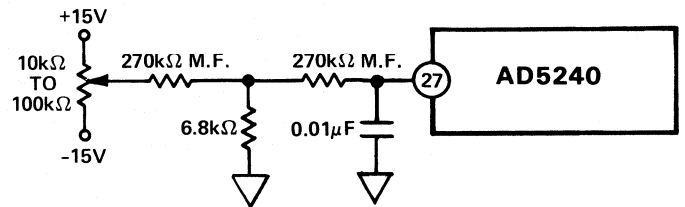
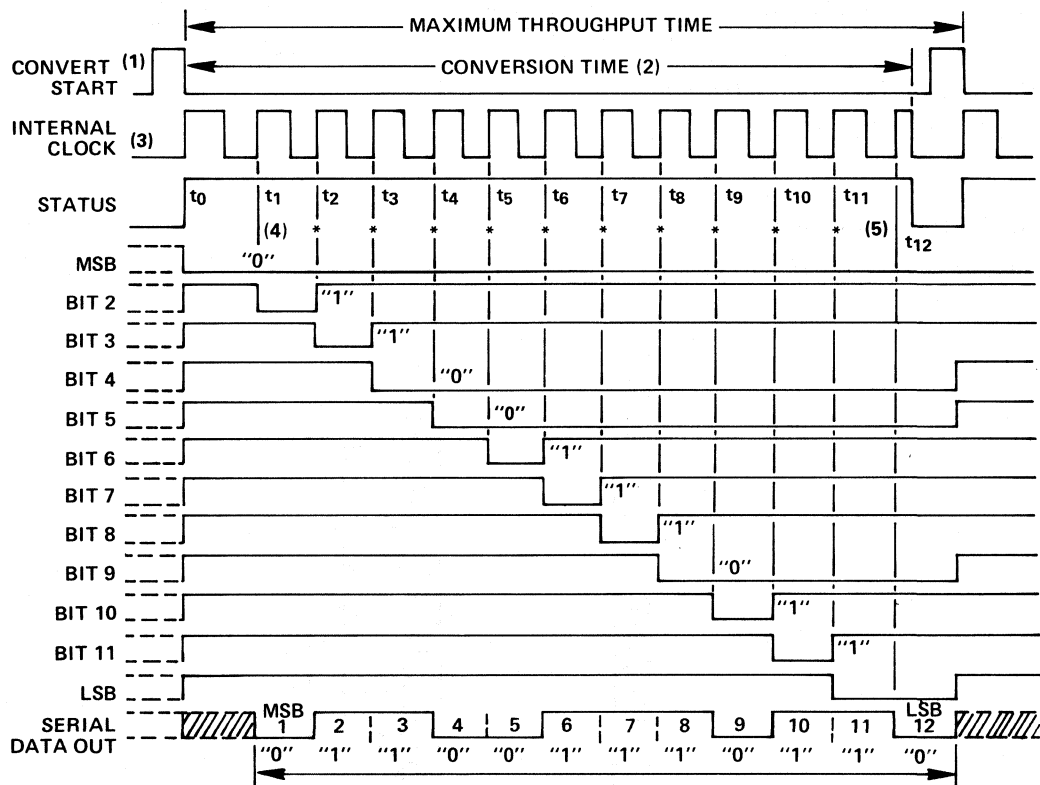


Figure 4. Low Tempco Gain Adjustment Circuit



NOTES

1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
 2. 5μs FOR 12 BITS AND 4.2μs FOR 10 BITS (MAX - PIN 17 TO +5V).
 3. FIRST CLOCK PULSE: 300(ns)H, 300(ns)L. SECOND THROUGH TWELFTH CLOCK PULSE: 100(ns)H, 300(ns)L.
 4. MSB DECISION.
 5. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW.
- *BIT DECISIONS

Figure 5. Timing Diagram (Binary Code 011001110110)

6.1 Digital Output Data.

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{Bit 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 50ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 5. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

The digital output codes corresponding to analog input voltages are shown in Tables 2 and 3.

INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range		$\pm 10\text{V}$	$\pm 5\text{V}$	$\pm 2.5\text{V}$	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{\text{FSR}}{2^n}$	$\frac{20\text{V}}{2^n}$	$\frac{10\text{V}}{2^n}$	$\frac{5\text{V}}{2^n}$	$\frac{10\text{V}}{2^n}$	$\frac{5\text{V}}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB	LSB					
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:

*COB = Complementary Offset Binary

**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit (MSB). MSB is available to pin 13.

***CSB = Complementary Straight Binary.

****Voltages given are the nominal value for transition to the code specified.

Table 2. Input Voltages and Code Definition

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
$\pm 10\text{V}$	COB or CTC	22	Input Signal	25	25
$\pm 5\text{V}$	COB or CTC	22	Open	24	24
$\pm 2.5\text{V}$	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table 3. AD5240 Input Scaling Connections

6.1.1 Short Cycle Input.

A Short Cycle input, pin 14, permits the timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision $t_{10} + 40\text{ns}$ in timing diagram of Figure 5. Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table 4.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	16	12	0.024	5.0	$t_{12} + 40\text{ns}$
2	16	10	0.100	4.1	$t_{10} + 40\text{ns}$
4	16	8	0.390	3.3	$t_8 + 40\text{ns}$

Table 4. Short Cycle Connections

1.1 Scope.

This specification covers the requirements for a fast settling, wide bandwidth dc-coupled transimpedance operational amplifier.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD9610TH/883B

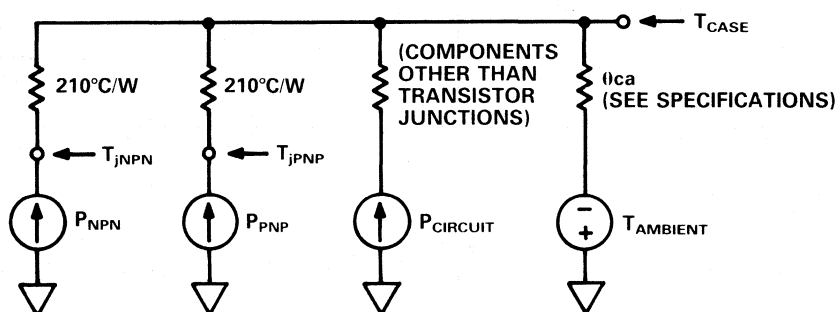
1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: H-12A. This package is non-standard to MIL-M-38510 Appendix C.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{ V}$
Power Dissipation	900 mW
Input Voltage	$\pm 8\text{ V}$
Junction Temperature	$+165^\circ\text{C}$
Operating Temperature Range (Case)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range (Case)	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	$+165^\circ\text{C}$

1.5 Thermal Characteristics.



$$P_{\text{CIRCUIT}} = I_{\text{CC}}[+V_{\text{CC}} - (-V_{\text{CC}})] \text{ WHERE } I_{\text{CC}} = 21\text{mA @ } \pm 15\text{V}$$

$$P_{\text{XXX}} = [(\pm V_{\text{CC}}) - V_{\text{OUT}} - I_{\text{COL}}^{(8)}] (I_{\text{COL}}) (\% \text{ DUTY CYCLE})$$

NOTE: XXX = NPN OR PNP

(FOR POSITIVE V_{OUT} AND V_{CC} , THIS IS POWER IN NPN OUTPUT STAGE;
FOR NEGATIVE V_{OUT} AND V_{CC} , THIS IS POWER IN PNP OUTPUT STAGE.
 $I_{\text{COL}} = V_{\text{OUT}}/R_{\text{LOAD}}$ OR 3.0mA, WHICHEVER IS GREATER.
FEEDBACK RESISTOR R_F IS INCLUDED IN R_{LOA} .)

$$T_{j(\text{PNP})} = P_{\text{PNP}} (210 + \theta_{\text{ca}}) + (P_{\text{CIRCUIT}} + P_{\text{NPN}}) (\theta_{\text{ca}}) + t_a \text{ SIMILAR FOR } T_{j(\text{NPN})}$$

AD9610TH – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group ¹ 1	Sub Group ¹ 2, 3	Sub Group ² 4	Sub Group ² 5, 6	Test Condition ³	Units
Power Supply Current	I _{CC}	–1	25	25	27				mA max
Input Offset Voltage	V _{OS}	–1	±1.0	±1.0	±4.0 ±2.5			T _C = –55°C T _C = +125°C	mV max
Input Bias Current, Inverting	I _{B–}	–1	±15	±15	±56 ±35			T _C = –55°C T _C = +125°C	µA max
Input Bias Current, Noninverting	I _{B+}	–1	±15	±50	±75 ±62			V _{OUT} = 0 V _{OUT} = 0, –55°C V _{OUT} = 0, +125°C	µA max
Output Voltage Swing	V _{OUT}	–1	±9	±9	±9			R _L = 200 Ω	mA max
Resistor Feedback	R _{FB}	–1		1490 1510					Ω min Ω max
Input Offset Voltage Tempco	TC _{VOS}	–1			±25			V _{OUT} = 0	µV/°C max
Input Bias Current Tempco, Inverting	TC _{IB–}	–1			±330			V _{OUT} = 0	nA/°C max
Input Bias Current Tempco, Noninverting	TC _{IB+}	–1			±200			V _{OUT} = 0	nA/°C max
Power Supply Rejection Ratio	PSRR	–1	35			35	35	10 V Supply Swing	dB min
Power Supply Sensitivity Referred to Input	PSSV	–1	50			50	50	ΔV _S = 10 V	dB min
	–PSS	–1	8			8	8	V _{OUT} = 0	µA/V max
	+PSS	–1	8			8	8		
Common Mode Rejection Ratio	CMRR	–1				35	35	5 V Supply Swing	dB min
Common Mode Sensitivity Referred to Input	–CMS	–1	8			8	8	5 V Supply Swing	µA/V max
	+CMS	–1	8			8	8	V _{OUT} = 5 V	dB min
	CMSV	–1	50			50	50		
Open Loop Gain	A _{OL}	–1	0.9			0.9	0.7	R _L = 200 Ω	MΩ min
Bandwidth	BW	–1	80			80	80	V _{OUT} = 1 mV p-p	MHz min
Amplitude of Peaking		–1	0.2			0.2	1	≤60 MHz, V _{OUT} = 100 mV p-p, +125°C	dB max
							+0.4	≤60 MHz, V _{OUT} = 100 mV p-p, –55°C	dB max
Total Harmonic Distortion	THD	–1	50			50	50	V _{OUT} = 2 V p-p F = 20 MHz	MHz min

NOTES

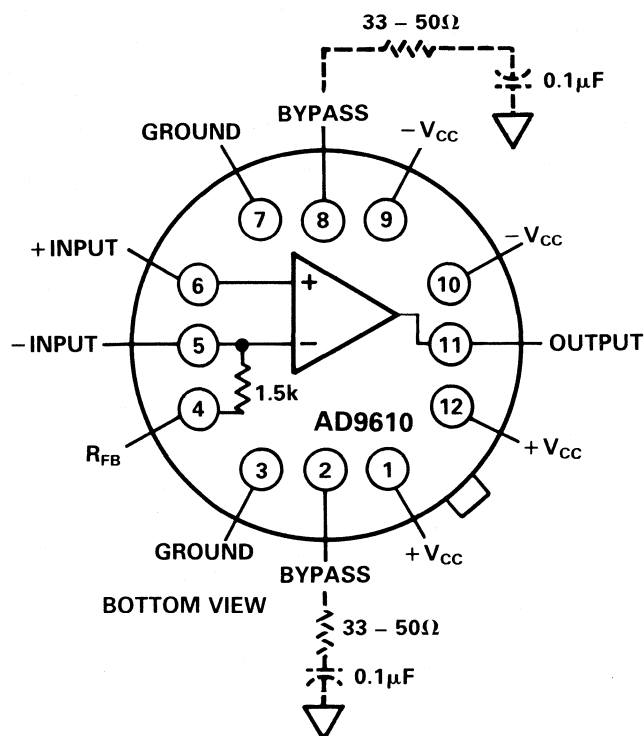
¹Unless otherwise specified, ±V = +15 V; A_V = –10; R_{FB} = 15 kΩ; no R_L for Subgroup 1, 2 and 3 tests.

²Unless otherwise specified, ±V = +15 V; A_V = –10; R_{IN} = 150 Ω; R_{FB} = 1.5 kΩ; R_L = 200 Ω for Subgroup 4, 5 and 6 tests.

³T_A = +25°C unless otherwise noted

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

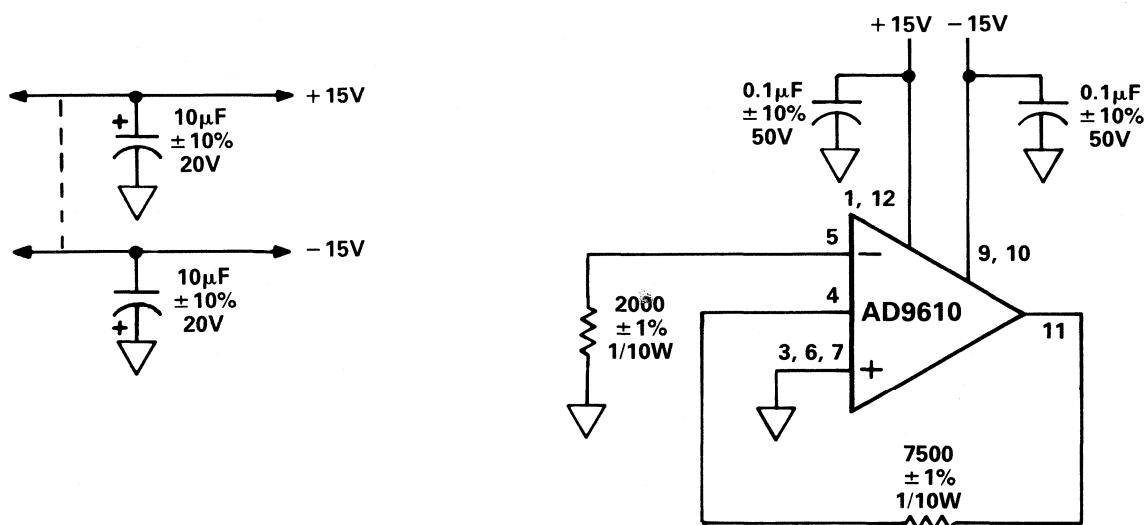


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements of a hybrid, high speed, 12-bit successive approximation analog-to-digital converter including internal clock, reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD ADC85S-12/883B
-2	AD ADC85SZ-12/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32D.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Logic Supply Voltage	$+7\text{V}$
Analog Inputs (Pins 24, 25)	$\pm 25\text{V}$
Digital Inputs	$+5.5\text{V}$
Junction Temperature	$+175^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 8^\circ\text{C}/\text{W}$
 $\theta_{JA} = 38^\circ\text{C}/\text{W}$

AD ADC85 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Test Condition ¹	Units
Analog Input Voltage Ranges	V _{IN}	– 1	± 2.5, ± 5, ± 10 0 to 5 0 to 10						V
	V _{IN}	– 2	± 2.5, ± 5 0 to 5					± V _{CC} = ± 12V + V _{DD} = + 5V	V
Input Impedance			3					10V Range	kΩ min
Buffer Amp Bias Current	I _B	– 1, 2	100				100		± nA max
Buffer Amp Offset Error		– 1, 2	10				10		± mV max
Buffer Amp Common-Mode Rejection		– 1, 2	70				70		dB min
Buffer Amp Settling Time		– 1, 2	2					T _A = 25°C To 0.01% for 10V Step	μs max
Reference Output Error	V _{REF}	– 1, 2	15	15				6.3V Nominal	± mV max
Reference Voltage Drift	V _{REFD}	– 1, 2	20		20			+ 5V Input Range	± ppm/°C max
Unipolar Gain Error ²	V _{GE}	– 1, 2	0.25	0.25				0 to 10V Input Range	± % FSR max
Unipolar Offset Error ²	V _{OSE}	– 1, 2	0.2	0.2				0 to 10V Input Range	± % FSR max
Unipolar Offset Drift	V _{OSD}	– 1, 2	5		5			0 to 10V Input Range	± ppm/°C max
Bipolar Gain Error ²	V _{GE}	– 1, 2	0.25	0.25				± 10V Input Range	± % FSR max
Bipolar Gain Drift	V _{FSE}	– 1, 2	25		25			± 10V Input Range	± ppm/°C max
Bipolar Offset Error ²	V _{OSE}	– 1, 2	0.25	0.25				± 10V Input Range	± % FSR max
Bipolar Offset Drift	V _{OSD}	– 1, 2	10		10			± 5V Input Range	± ppm/°C max
Linearity Error	RA	– 1, 2	1/2				1/2	Major Carries & Summations	± LSB max
Differential Linearity Error ³	DNL	– 1, 2	1		1		1	Major Carries & Summations	± LSB max
+ 5V Power Supply Sensitivity	PSRR ₁	– 1, 2	0.01				0.01	+ V _{DD} = 4.75V to 5.25V	± % FSR/% max
± 15V Power Supply Sensitivity	PSRR ₂	– 1	0.04				0.04	± V _{CC} = ± 14.55V to 15.45V	± % FSR/% max
± 12V Power Supply Sensitivity	PSRR	– 2	0.04				0.04	± V _{CC} = ± 11.4V to ± 12.6V	± % FSR/% max
Clock Adjust		– 1, 2	0.1	1.0				To 10V	μs/V min
Conversion Speed ⁴	t _C	– 1, 2	10 8.4			10 8.4		To 12 Bits To 10 Bits	μs max
Serial/Parallel Code Match Error	SP _{CM}	– 1, 2	0				0		± Bits
Output High Drive	V _{OH}	– 1, 2	2.4				2.4	@ – 80μA	V min
Output Low Drive	V _{OL}	– 1, 2	0.4				0.4	@ 3.2mA	V max
+ 5V (+ V _{DD}) Supply Drain	+ I _{DD}	– 1, 2	140				140	All Bits On	+ mA max
+ 15V (+ V _{CC}) Supply Drain	+ I _{CC}	– 1, 2	25				25	All Bits On	+ mA max
– 15V (– V _{CC}) Supply Drain	– I _{CC}	– 1, 2	35				35	All Bits On	– mA max
Total Power Dissipation	P _D	– 1, 2	1.5				1.5	All Bits On	W max

Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Test Condition ¹	Units
Power Supply Range	$+V_{DD}$ $\pm V_{CC}$	-1	$\pm 5\%$ $\pm 10\%$					For Rated Accuracy	
	$+V_{DD}$ $+V_{CC}$	-2	$\pm 5\%$ $+11.4V$ to $+16.5V$					For Rated Accuracy	

NOTES

¹ $V_{CC} = \pm 15V$, $V_{DD} = +5V$ unless otherwise noted.

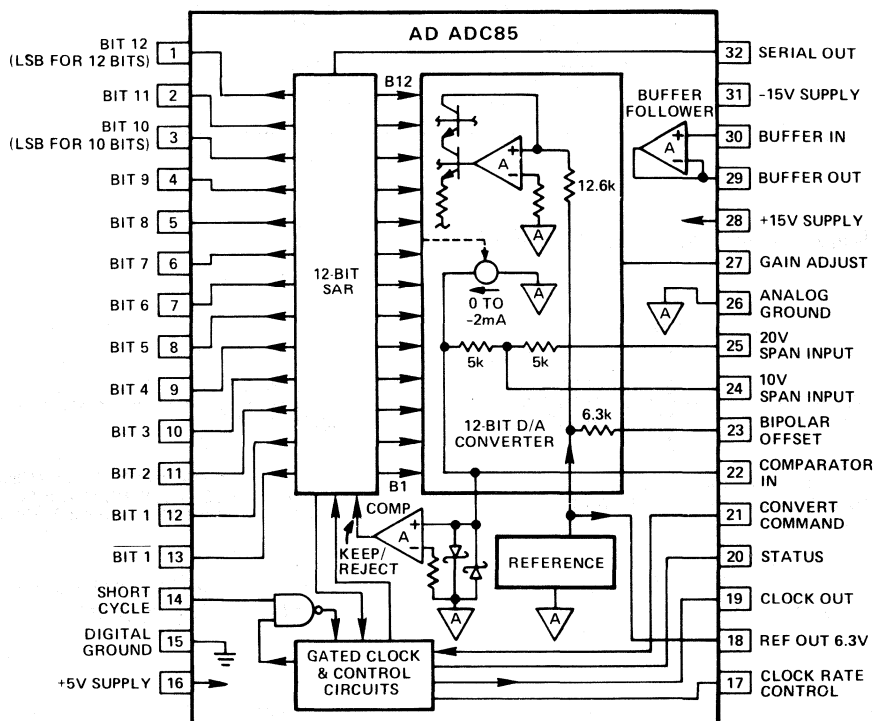
²Adjustable to zero.

³ $V_{CC} = \pm 12$ for the -2 version. No missing codes guaranteed with internal clock.

⁴With internal clock, Pin 17 tied to +5V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



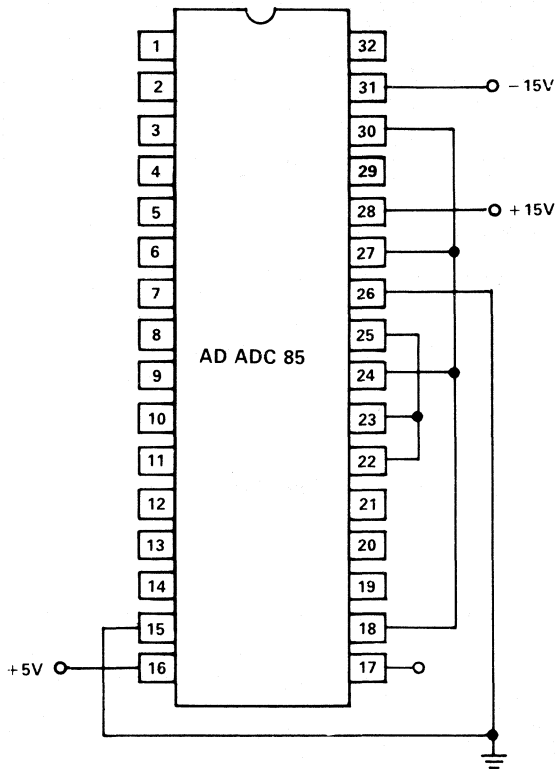
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

AD ADC85

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



6.1 Clock Rate Control Alternate Connections.

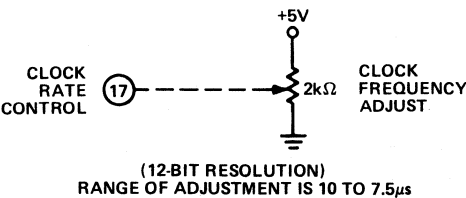


Figure 1. 12-Bit Clock Rate Control Optional Fine Adjust

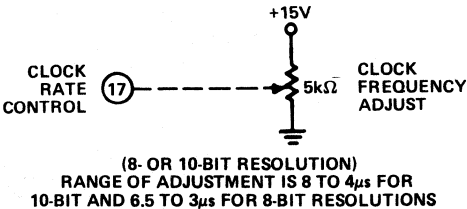


Figure 2. 8-Bit Clock Rate Control Optional Fine Adjust

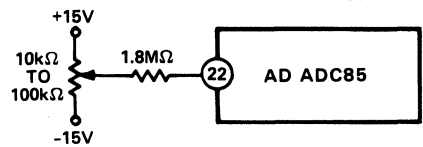


Figure 3. Offset Adjust Circuit

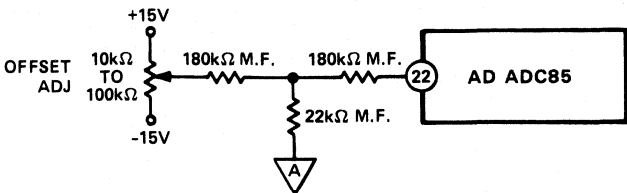


Figure 4. Low Tempco Zero Adjustment Circuit

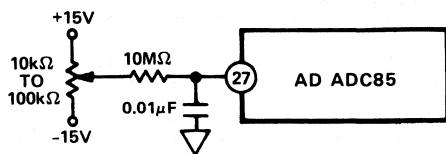


Figure 5. Gain Adjustment Circuit

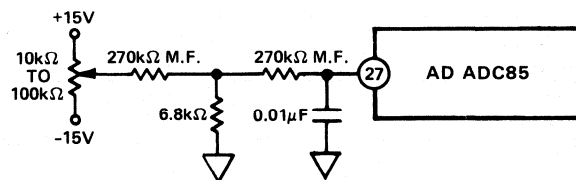
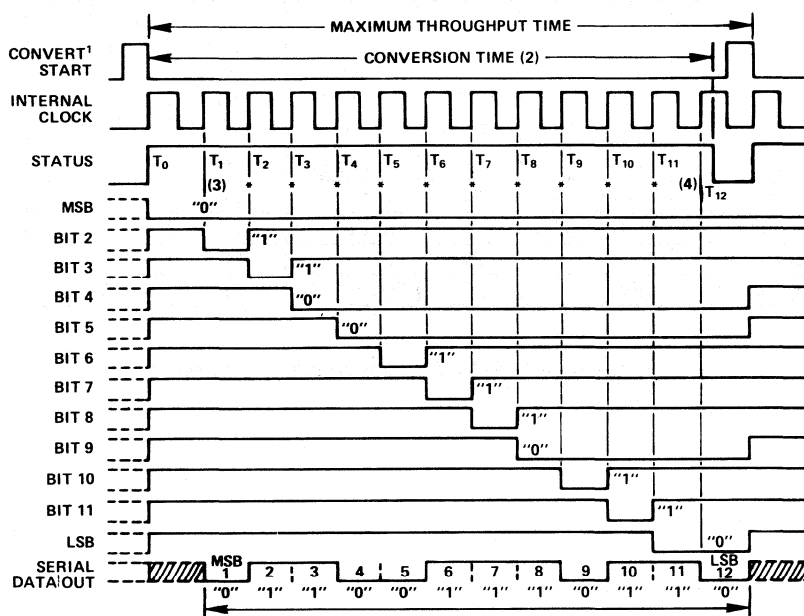


Figure 6. Low Tempco Gain Adjustment Circuit

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10	$t_{12} + 40\text{ns}$
2	16	10	0.100	6	$t_{10} + 40\text{ns}$
4	28	8	0.390	3.2	$t_8 + 40\text{ns}$

Table 2. Short Cycle Connections



NOTES

1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 10μs FOR 12 BITS AND 6μs FOR 10 BITS (MAX).
3. MSB DECISION.
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LO.

* BIT DECISIONS.

Figure 7. Timing Diagram (Binary Code 011001110110)

INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range		$\pm 10V$	$\pm 5V$	$\pm 2.5V$	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB LSB						
000 ... 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V
111 ... 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:

*COB = Complementary Offset Binary

**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit (MSB). MSB is available to pin 13.

***CSB = Complementary Straight Binary.

****Voltages given are the nominal value for transition to the code specified.

Table 3. Input Voltages and Code Definition

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
$\pm 10V$	COB or CTC	22	Input Signal	25	25
$\pm 5V$	COB or CTC	22	Open	24	24
$\pm 2.5V$	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table 4. AD ADC85 Input Scaling Connections

1.1 Scope.

This specification covers the device requirements for a high performance 12-bit hybrid digital-to-analog converter. (The monolithic version is detailed on page 619.)

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD DAC85MILCBI-V/883B
-2	AD DAC85MILCBI-I/883B
-3	AD DAC87CBI-V/883B
-4	AD DAC87CBI-I/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-24A.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage V_{CC} to Digital Return	+18V
Negative Supply Voltage V_{EE} to Digital Return	-18V
Positive Supply Voltage V_{DD} to Digital Return	+7V
Digital Input Voltage to Digital Return	0V to V_{DD}
Output Short Circuit Duration (to Ground Only)	25ms
Junction Temperature	+175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 7^\circ\text{C/W}$
 $\theta_{JA} = 37^\circ\text{C/W}$

AD DAC85/AD DAC87 – SPECIFICATIONS

Test	Symbol	Device	Design Limit +25°C (–55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
Logic Levels								
Digital Input High	V _{IH}	–1, 2, 3, 4	2.0			2.0		+ V min
Digital Input Low	V _{IL}	–1, 2, 3, 4	0.8			0.8		+ V max
Digital Input High Current	I _{IH}	–1, 2, 3, 4	1			1	V _{IH} = 5.0V	– μA min
			250			250		+ μA max
Digital Input Low Current	I _{IL}	–1, 2, 3, 4	10			10	V _{IL} = +0.8V	– μA min
			100			100		+ μA max
Gain Error ³	A _E	–1, 2	0.3	0.3			Input Bits = 0000 0000 0000 To Input Bits = 1111 1111 1111 Unipolar V _{FSR} = 10V	± % FSR max
		–3, 4	0.2			0.2		
Gain Error Drift	TCA _E	–1, 2	20		20		Input Bits = 0000 0000 0000 Unipolar = 0 to +10V	± ppm/°C max
		–3, 4	25		25		Unipolar = 0 to +10V	
Unipolar Offset	V _{OS}	–1, 2	0.15	0.15			Input Bits = 1111 1111 1111 Unipolar V _{FSR} = 10V	± % FSR max
		–3, 4	0.10			0.10		
Unipolar Offset Drift	TC _{VOS}	–1, 2, 3, 4	3		3		Input Bits = 1111 1111 1111 Unipolar V _{FSR} = 10V	± ppm/°C max
Bipolar Offset	B _{POE}	–1, 2	0.15	0.15			Input Bits = 1111 1111 1111	± % FSR max
		–3, 4	0.10			0.10		
Bipolar Offset Drift	TCB _{POE}	–1, 2, 3, 4	10		10		Input Bits = 1111 1111 1111	± ppm/°C max
Unipolar Zero Error Current Output	I _{OS}	–2, 4	3	3			Input Bits = 1111 1111 1111	μA max
Bipolar Zero Error Current Output	I _{BPZE}	–2, 4	3	3			Input Bits = 0111 1111 1111	μA max
Bipolar Gain Error Current Output	I _{BPGE}	–2, 4	0.96			0.96	Input Bits = 0000 0000 0000	– μA max
			1.04			1.04		– μA min
Bipolar Offset Error Current Output	I _{BPOE}	–2, 4	0.96			0.96	Input Bits = 1111 1111 1111	+ μA min
			1.04			1.04		+ μA max
Unipolar Gain Error Current Output	I _{OG E}	–2, 4	2.3995			2.3995	Input Bits = 0000 0000 0000	– μA min
			1.5995			1.5995		– μA max
Bipolar Zero Error	B _{PZ}	–1, 2	0.15	0.15			Input Bits = 0111 1111 1111	± % FSR max
		–3, 4	0.10			0.10		
Compliance Voltage	C _V	–2, 4	2.5					– V min
			10					+ V max
Differential Linearity Error	D _{LE}	–1, 2, 3, 4	1/2	1/2			(Abbreviate Codes Test)	± LSB max
Differential Linearity Error T _A @ T _{min} to T _{max}	TC _{DLE}	–1, 2 –3, 4	1.0		1.0		(Abbreviate Codes Test) (Monotonic Over Temperature Range)	± LSB max
Linearity Error	LE	–1, 2, 3, 4	0.5	0.5			(Abbreviate Codes Test)	± LSB max
Linearity Error T _A @ T _{min} to T _{max}	TC _{LE}	–1, 2, 3, 4	0.75		0.75		(Abbreviate Codes Test)	± LSB max
Positive Summation Error	E _{PE}	–1, 2, 3, 4	0.50	0.50				± LSB max
Negative Summation	E _{NE}	–1, 2, 3, 4	0.50	0.50				± LSB max
Positive Summation Error Drift	E _{PETC}	–1, 2, 3, 4	0.75		0.75			± LSB max
Negative Summation Error Drift	E _{NETC}	–1, 2, 3, 4	0.75		0.75			± LSB max
Reference Output Error	V _{REF}	–1, 3	126			126	V _{REF} = 6.3V	± mV max

Table 1. (Continued on next page)

AD DAC85/AD DAC87

Test	Symbol	Device	Design Limit +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ^{1, 2}	Units
Reference Output Temperature Coefficient	TCV _{REF}	-1 -3	(20) (10)		20 10			± ppm/°C max
Settling Time	t _{SL}	-1, 3	7				Settling Time to ± 0.01% FSR for FSR Change (2kΩ 500pF with 10k Feedback Resistor)	μs max
	t _{SL}	-1, 3	3				Small Signal Change (1LSB) Settling within 1/2LSB	μs max
	t _{SL}	-2, 4	300				Settling Time to ± 0.01% of FSR for FSR Change 10 to 100Ω Load	ns typ
	t _{SL}	-2, 4	1				For 1kΩ Load	μs typ
+5V Supply Current Drain	+I _D	-1, 2, 3, 4	20			20		+ mA max
+15V Supply Current Drain	+I _{CC}	-1, 2, 3, 4	20			20		+ mA max
-15V Supply Current Drain	+I _{EE}	-1, 2, 3, 4	35			35		- mA max
Power Supply Gain Sensitivity Δ Gain	PSRR	-1, 3	0.003			0.003	+5V, +15V, -15V; Supplies ± 5% Variation	± %/FS/%V _S
Power Supply Gain Sensitivity Δ Gain T _{min} to T _{max}	TCPSRR	-1, 3	(0.03)				+5V, +15V, -15V; Supplies ± 5% Variation	± %/FS/%V _S

NOTES

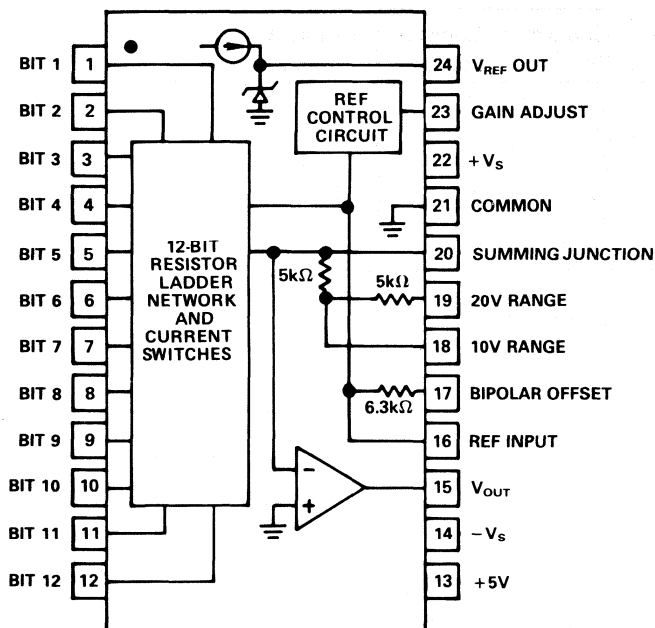
¹T_A = +25°C and ±V_S = ±15V unless otherwise specified.

²V_{SS} = ±15V, V_D = +5V unless otherwise noted.

³Adjustable to zero.

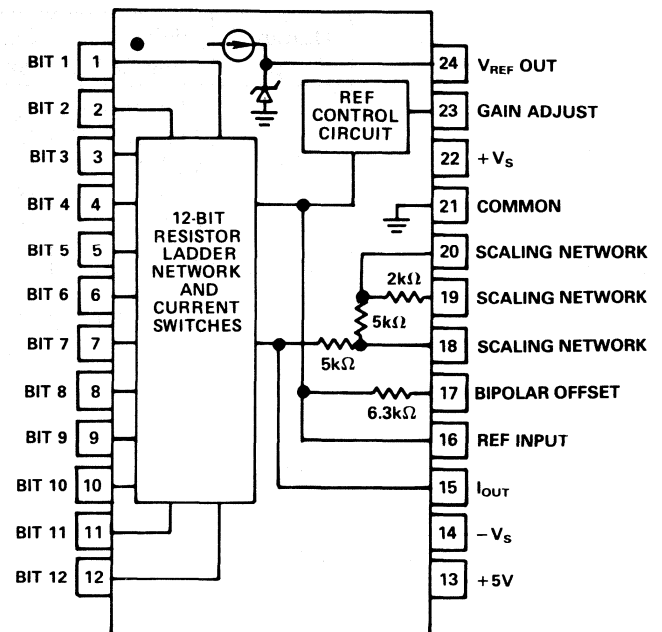
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Device - 1 or 3

Voltage Model Functional Diagram
and Pin Configuration



Device - 2 or 4

Current Model Functional Diagram
and Pin Configuration

REV. C

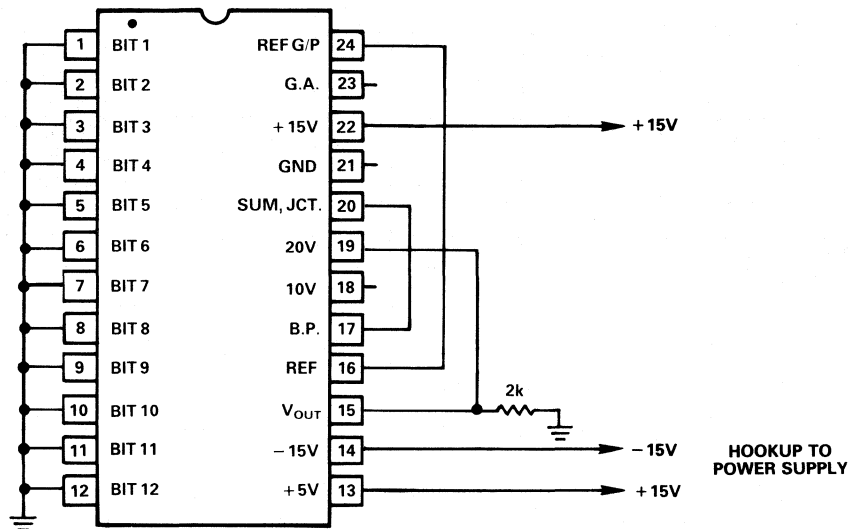
AD DAC85/AD DAC87

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

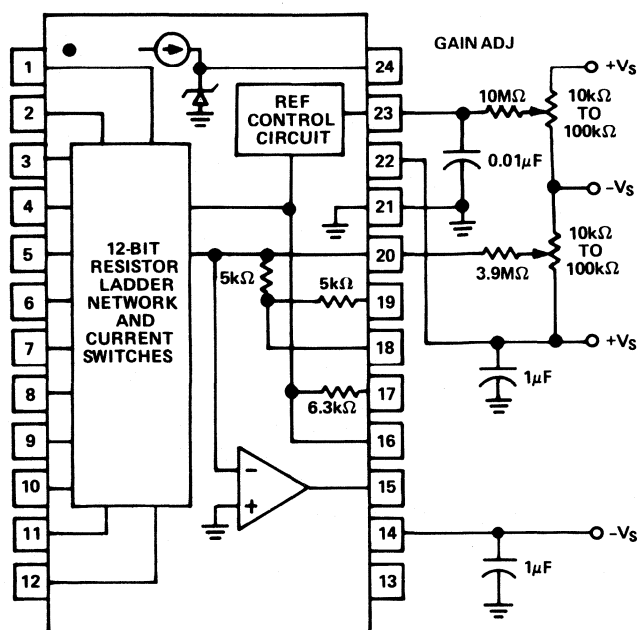
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



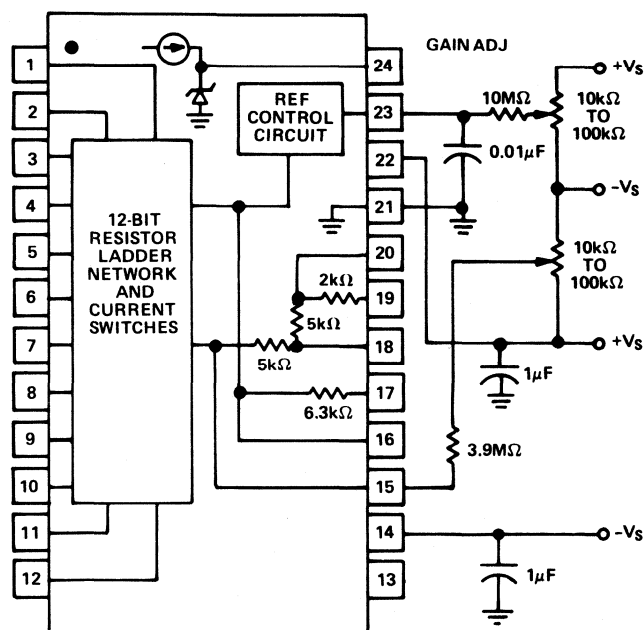
Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
± 10V	COB or CTC	19	20	15	24
± 5V	COB or CTC	18	20	N.C.	24
± 2.5V	COB or CTC	18	20	20	24
0 to + 10V	CSB	18	21	N.C.	24
0 to + 5V	CSB	18	21	20	24
0 to + 10V	CCD	19	N.C.	15	24

Table 2. Digital Input/Analog Output



Device – 1 or 3

External Adjustment and Voltage
Supply Connection Diagram



Device – 2 or 4

External Adjustment and Voltage
Supply Connection Diagram

Digital Input		Analog Output			
12 Bit Resolution		Voltage*		Current	
MSB	LSB	0 to +10V	± 10V	0 to – 2mA	± 1mA
CBI Model	0 0 0 0 0 0 0 0 0 0 0 0	+ 9.9976V	+ 9.9951V	– 1.9995mA	– 0.9995mA
	0 1 1 1 1 1 1 1 1 1 1 1	+ 5.0000V	00000V	– 1.0000mA	0.0000mA
	1 0 0 0 0 0 0 0 0 0 0 0	+ 4.9976V	– 0.0049V	0.488mA	+ 1.000mA
	1 1 1 1 1 1 1 1 1 1 1 1	0.0000V	– 10.0000V	0.0000mA	0.488μA
	1LSB	2.44mV	4.88mV	– 0.9995mA	+ 0.0005mA

*To obtain values for other binary ranges 0 to + 5V range: divide 0 to + 10 values by 2;
± 5V range: divide ± 10V range values by 2; ± 2.5V range: divide ± 10V range values by 4.

Table 3. Output Voltage Range Connections-Voltage

1.1 Scope.

This specification covers the requirements for an ultrahigh speed current output digital-to-analog converter.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	HDS-1250TM/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: M-24A. This package is non-standard to MIL-M-38510 Appendix C.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 17\text{ V}$
Power Dissipation	1.09 W
Digital Inputs	0 to +8 V
Junction Temperature	+165°C
Operating Temperature Range (Case)	-55°C to +125°C
Storage Temperature Range (Case)	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 12^\circ\text{C/W}$
 $\theta_{JA} = 34^\circ\text{C/W}$

HDS-1250TM – SPECIFICATIONS

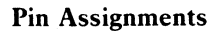
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 5, 6	Sub Group 9	Test Conditions ¹	Units
Positive Power Supply Current (+V _S)	I _{CC}	–1		54	54				Bits 1–12 Off	mA max
Negative Power Supply Current (–V _S)		–1		19	19				Bits 1–12 Off	mA max
Unipolar Offset	V _{OS}	–1	+0.5	1.5	1.5				Bits 1–12 Off	μA max
High Level Input Current	I _{IH}	–1	40	40					Bits 1–12 On; V _{IN} = 2.5 V	μA max
					100				Bits 1–12 On; T _C = +125°C; V _{IN} = 2.5 V	
					40				Bits 1–12 On; T _C = –55°C; V _{IN} = 2.5 V	
Bit 1 Low Level Input Current	I _L	–1		7.0	7.0				Bits 1–12 Off; V _{IN} = 0 V	mA max
Bits 2–12 Low Level Input Current				3.5	3.5				Bits 1–12 Off; V _{IN} = 0 V	mA max
Power Supply Rejection Ratio	PSRR	–1		0.06	0.08				Bits 1–12 On; ±V _S = ±14.5 V – ±15.5 V	%/% max
Bipolar Zero		–1	±0.1			±0.2			Bit 1 On; Bits 2–12 Off; Bipolar On	% FS max
Bipolar Offset	BP _{OS}	–1	±0.25			±0.5			Bits 1–12 Off; Bipolar On	% FS max
Unipolar Full Scale	U _{FS}	–1	±0.25			±0.25			Bits 1–12 On; Output = I _{OUT}	% FS max
Differential Nonlinearity	DNL	–1	±0.25				–1.0		Output = I _{OUT} All Major Carries	LSB min
						±0.5				
							2.0			LSB max
Integral Nonlinearity	INL	–1	±0.25			±0.5	±1.5		Output = I _{OUT} ; Best Straight Line Fit	LSB max
Unipolar Full-Scale Gain		–1	±0.1			±0.25				% FS max
Unipolar Full-Scale Gain Tempco		–1	±30				±60		Bits 1–12 On; Output = I _{OUT}	ppm/°C max
Unipolar Full-Scale Voltage		–1				±0.25			Bits 1–12 On; Output = V _{OUT} Using R _{LOAD}	% FS max
Bipolar Gain		–1				±6.25			Bits 1–12 On Bipolar On	% FS max
Bipolar Offset Tempco		–1	±15				±30		Bits 1–12 Off Bipolar On	ppm/°C max
Bipolar Zero Tempco		–1					±75		Bipolar On; Bit 1 On; Bits 2–12 Off	ppm/°C max
Settling Time	t _S	–1	35					35	Output = V _{OUT} ; See Note 2	ns max
High Level Input Current	I _{IN}	–1	40	40					Bits 1–12 On; V _{IN} = 7.0 V	μA max
					100				TC = +125°C	
					40				TC = –55°C	

NOTES

¹T_A = +25°C unless otherwise specified.

²With internal R_{LOAD} and LSB step at midscale to 0.1%.

Table 1.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

1.1 Scope.

This specification covers the detail requirements for a fast settling, video operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	HOS-050A/883B
-2	HOS-060SH/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: H-12A (Note: Nonstandard to MIL-M-38510 Appendix C).

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$ (V_S)
Maximum Power Dissipation	(See Figure 2)
Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{jc} = 55^\circ\text{C/W}$
 $\theta_{ja} = 70^\circ\text{C/W}$

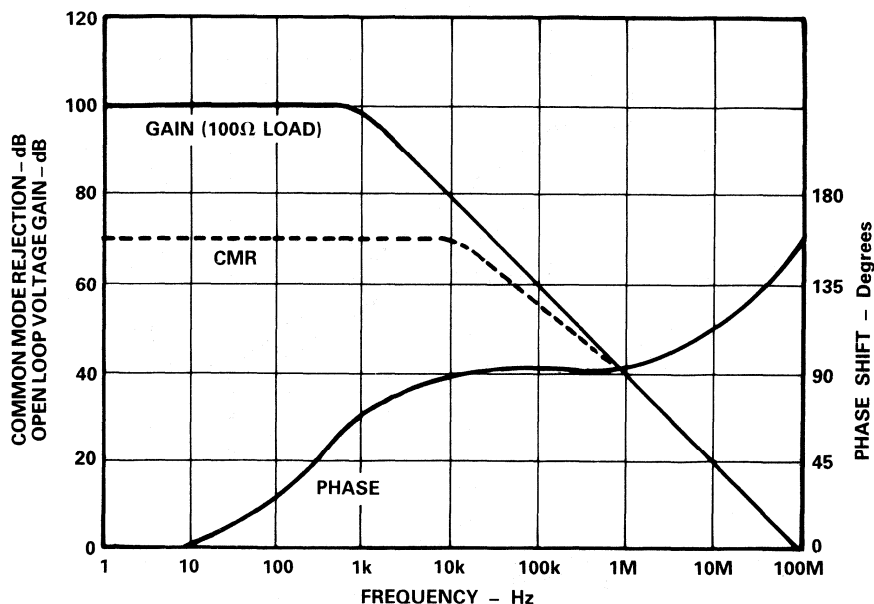


Figure 1. Frequency Response

HOS-050A/HOS-060SH – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 5	Sub Group 6	Test Condition	Units
Input Offset Voltage	V_{OS}	-1 -2	15 1	15 1	18.5 2				$R_S = 100k\Omega$	$\pm$ mV max
Input Bias Current	I_B	*	2	2	50					$\pm$ nA max
Input Offset Current	I_{OS}	*	0.1	0.1	25					nA max
Power Supply Current	I_{CC}	*	25	25						mA max
Output Voltage Swing -	V_{OUT}	*	-10	-10	-10				$R_L = 200\Omega$	V max
Output Voltage Swing +	V_{OUT}	*	10	10	10				$R_L = 200\Omega$	V min
Power Supply Rejection Ratio	PSRR	*	50			50	50	50	-12 to -18 & +15 V_S +12 to +18 & -15 V_S	dB min
Large Signal Voltage Gain	A_{VS}	*	80			80	80	80	$R_L = 200\Omega$	dB min
Voltage Gain	A_V	*	80			80	80	80	$F = 1kHz, R_L = 200\Omega$	dB min
Common-Mode Rejection Ratio	CMRR	*	60			60	55	55	$V_{IN} = 10V$	dB min
Input Offset Tempco	$\Delta V/\Delta T$	-1	35			35				$\pm$ $\mu V/^\circ C$ max
Slew Rate	t_{SR}	*	230			230	210	210	$A_V = -1, R_L = 200\Omega$ $A_V = 2, R_L = 200\Omega$	V/ μs min
Settling Time to 1% of Final Value	t_{SL}	*	100			100			$R_L = 200\Omega, A_V = 1$	ns max

NOTE

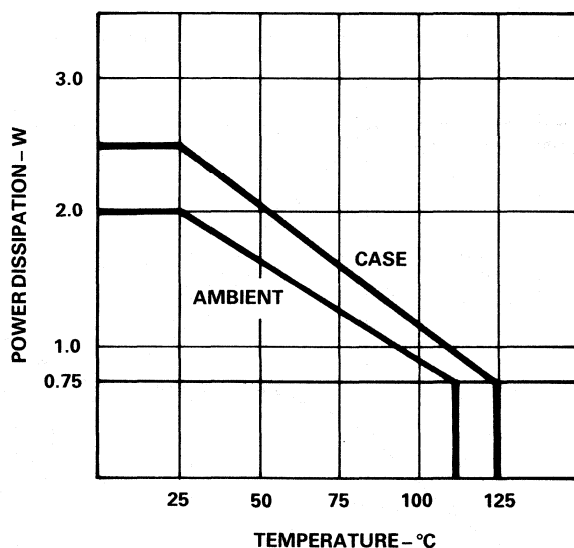
*Specifications for -1 are equivalent to -2.

Table 1.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 55^\circ C/W$

$\theta_{JA} = 70^\circ C/W$

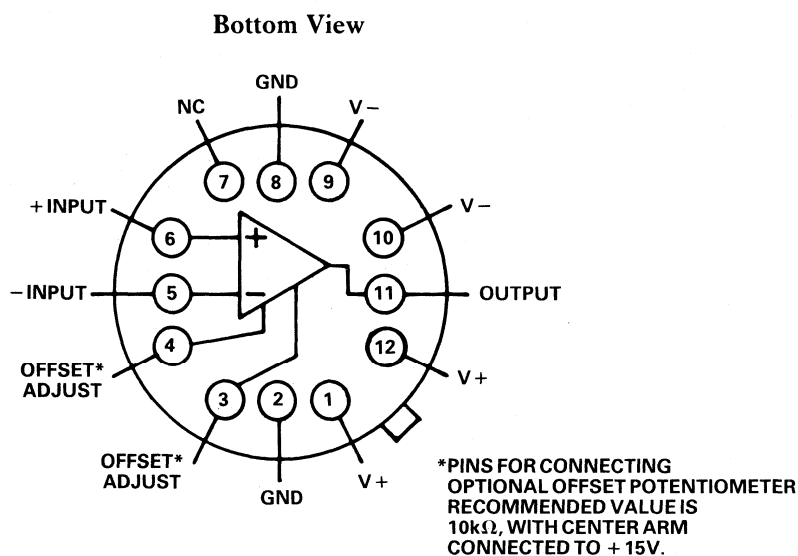


$\theta_{JA} = 70^\circ C/W.$
 $\theta_{JC} = 55^\circ C/W.$

Figure 2. Power Dissipation vs. Temperature

REV. A

3.2.1 Functional Block Diagram and Terminal Assignments.

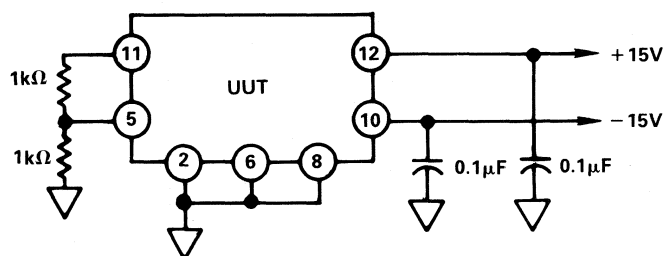


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



1.1 Scope.

This specification covers the detail requirements for an ultrahigh speed hybrid microcircuit track-and-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	HTC-0300AM/883B
–2	HTC-0300ATD/883B

1.2.3 Case Outline.

See Appendix I of General Specification ADI-H-1000: package outline: M-24A for –1, DH-24B for –2.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage (V_{CC}) to Common	+18V
Negative Supply Voltage (V_{EE}) to Common	–18V
+5 Volt Supply Voltage (V_I) to Common	–0.5V to +7V dc
Analog Input Voltage Range	$\pm V_{CC}$
Digital Inputs	–0.5V to +5.5V dc
Output Current	$\pm 50\text{mA}$
Operating Case Temperature Range	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Junction Temperature	175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 23^\circ\text{C/W}$
 $\theta_{JA} = 43^\circ\text{C/W}$

HTC-0300A – SPECIFICATIONS

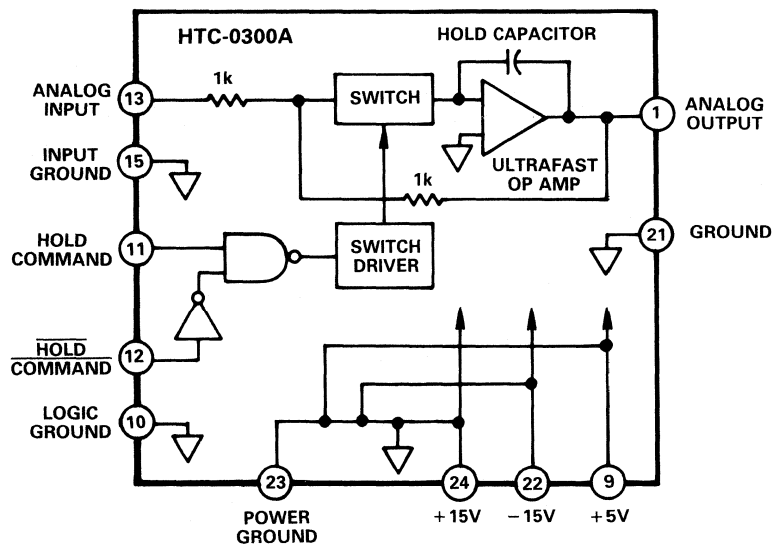
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 5, 6	Sub Group 7, 8	Test Condition ¹	Units
V _{CC} Supply Current	I _{CC}	– 1, 2	25	25	25				V _{IN} = 0V V (Pins 11 & 12) = 0V	+ mA max
V _{EE} Supply Current	I _{EE}	– 1, 2	25	25	25				V _{IN} = 0V V (Pins 11 & 12) = 0V	– mA max
V _{LOG} Supply Current	I _L	– 1, 2	5	5	5				V _{IN} = 0V V (Pins 11 & 12) = 0V	+ mA max
Total Power Consumption	P _D	– 1, 2	775	775	775				V _{IN} = 0V V (Pins 11 & 12) = 0V	mW max
Logic Input Current	I _{IH} I _{IL}	– 1, 2	1	1	1				V _{IH} = 2.4V V _{IL} = 0.4V	± µA max
High-Level Input Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0				V _{IN} = 0V	V min
Low-Level Input Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8				V _{IN} = 0V	V max
Input Offset Voltage	V _{IO}	– 1, 2	5	5	15					± mV max ± ppm FSR/°C
Input Resistance	R _I	– 1, 2	950 1050	950 1050	950 1050					Ω min Ω max
Gain Error	A _E	– 1, 2	0.1	0.1	0.15					% max
Gain Linearity Error	A _L	– 1, 2	0.01	0.01	0.01					% FS max
Power Supply, V _{CC} Rejection Ratio	PSRR +	– 1, 2	0.5	0.5	0.5				14.25 ≤ V _{CC} ≤ 15.75 V _{IN} = – 10V, V ₁₁ & V ₁₂ = 0V	± mV/V max
Power Supply, V _{EE} Rejection Ratio	PSRR –	– 1, 2	0.5	0.5	0.5				– 15.75 ≤ V _{EE} ≤ – 14.25 V _{IN} = + 10V, V ₁₁ & V ₁₂ = 0V	± mV/V max
Hold Step (Pedestal Voltage)	V _{HS}	– 1, 2	20			20	8 8			± mV max ± ppm of FSR/°C
Hold Mode Droop	V _{HD}	– 1, 2	5			5	1.8		T _C = 25°C T _C = 125°C	± µV/µs max ± mV/µs max
Track-to-Hold Transient	V _{TTH}	– 1, 2	380			380	380			mV p-p max
Acquisition Time	T _{AQ}	– 1, 2	200 170					200 170	10V Step to ± 1mV 10V Step to ± 10mV	ns max
Transient Response Settling Time, Track to Hold	TR _(TS)	– 1, 2	100 85					100 85	Settling to ± 1mV Settling to ± 10mV	ns max
Feedthrough Rejection Ratio	FRR	– 1, 2	64					64	V _{IN} = 20V p-p @ 2.5MHz, T _C = 25°C	dB min
Output Resistance	R _O	– 1, 2	0.25					0.25		Ω max
Output Slew Rate	ΔV _D /Δt	– 1, 2	220			220	220			V/µs min
Small Signal Bandwidth	BW	– 1, 2	8			8	8			MHz min

NOTE

¹T_A = +25°C unless otherwise specified

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

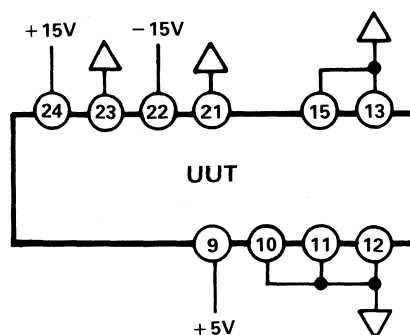
PIN	FUNCTION	PIN	FUNCTION
1	ANALOG OUTPUT	13	ANALOG INPUT
2	N/C	14	N/C
3	N/C	15	INPUT GROUND
4	N/C	16	N/C
5	N/C	17	N/C
6	N/C	18	N/C
7	N/C	19	N/C
8	N/C	20	N/C
9	+5V	21	GROUND
10	GROUND	22	-15V
11	HOLD	23	GROUND
12	HOLD	24	15V

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ASIC CAPABILITY

	Page
Combined Analog and Digital Application Specific Integrated Circuits (ASIC) Capability	998

Application Specific Integrated Circuits

Analog Devices offers a full spectrum of capabilities in mixed-signal application specific integrated circuits (ASICs). These chip-level systems can implement combined analog/digital designs with 12-bit accuracy and 16-bit resolution that formerly required board-level solutions.

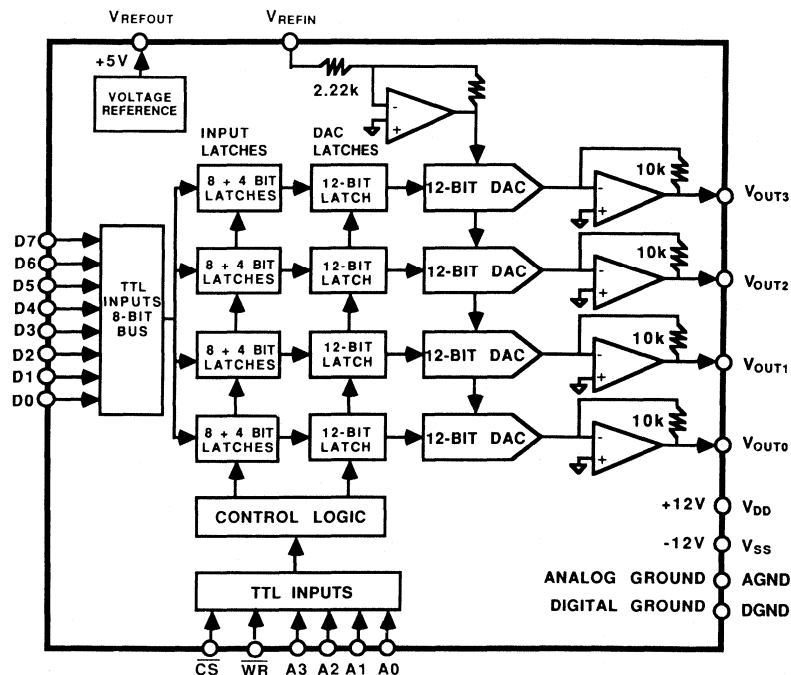
Analog Devices can incorporate most of the functions of its standard monolithic parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, England and Ireland.

Analog's multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products can be processed in full MIL-38510 certified facilities.

DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are two Linear System Macros, a custom chipset and a semicustom chip.



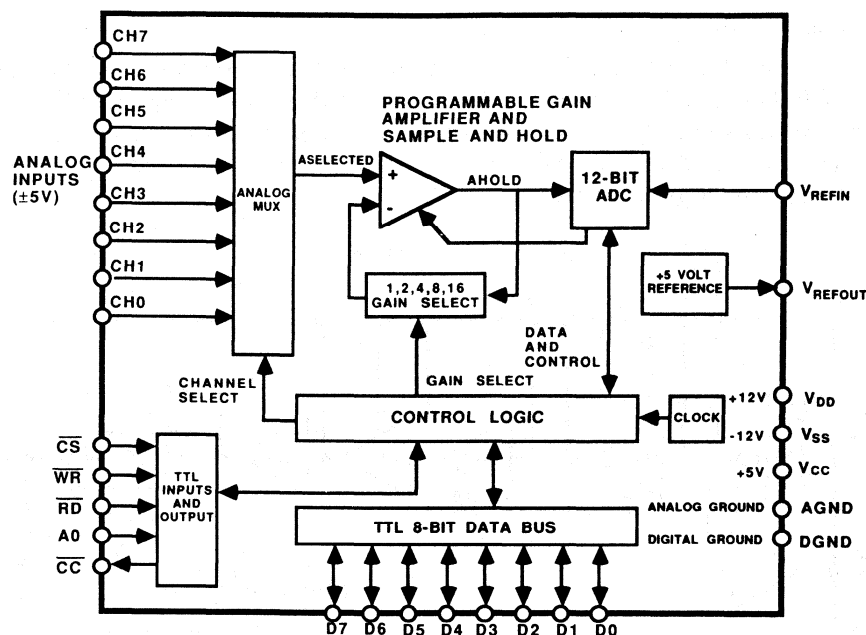
AD75004 Quad DAC

AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously.

AD75003 Data Acquisition System

This DAS converts analog signals on 8 input channels to 12-bit values and interfaces via an 8-bit parallel bus. The chip integrates an 8-channel multiplexer, programmable-gain amplifier, sample-and-hold and 12-bit A/D converter with internal voltage reference.



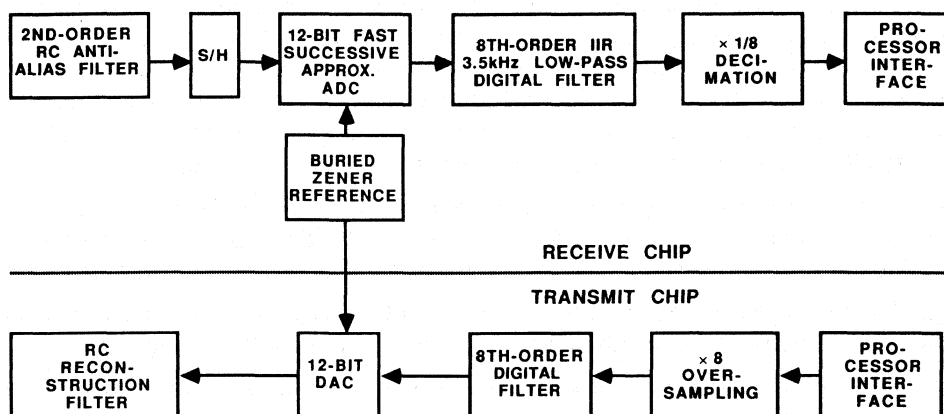
AD75003 Data Acquisition System

Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. One such device is a semicustom, serial-interface DAS. The AD75003 design was altered to have programmable gains of 1 to 20 instead of 1 to 16, and a serial UART instead of an 8-bit parallel interface. In addition to the AD75003 functions, this part contains a precision instrumentation amplifier, a programmable line-frequency notch filter, a 7-bit trim DAC and a temperature sensor.

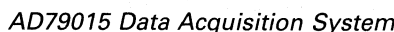
Modem Chipset

Library cells can be combined to form macro building blocks for high speed modems. This two-chip design concept filters and converts data to interface a digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an antialiasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter and decimation. On the other chip, transmit data is $8 \times$ oversampled, then goes to an 8th-order filter, a 12-bit DAC and an active reconstruction filter.



High Speed Modem Chipset

This circuit is a complete data acquisition system for biomedical signals (i.e., ECG and EEG) with a throughput of 10,000 samples per second. It provides high accuracy, high stability and functional completeness in a small 28-pin PLCC package. It includes a high-performance instrumentation amp, band-pass and notch filters, and a 12-bit ADC with on-chip reference. It also includes a fast 8/12-bit serial port to interface to most microprocessor systems.



Analog Devices' semicustom and custom circuits are fabricated using the same high performance processes as our standard ICs. These technologies include two mixed bipolar-CMOS processes and a high voltage CMOS process. These processes include thin-film resistors which may be laser trimmed for precise matching and stable performance over a wide temperature range.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 volts to split ± 15 V, with signal levels ranging from single-ended +3 V to ± 10 V. These processes are ideally suited for applications in data acquisition, instrumentation, industrial automation and telecommunications.

The following table summarizes the processes available for designing ASICs. Other processes in development offer even higher speed, denser logic and higher integration of analog and digital functions.

ANALOG DEVICES HIGH-PERFORMANCE PROCESSES FOR ASICS

Process	Power	Signal	Features
BiMOS II	± 12 V	± 8 V	Wide Variety of Precision Linear and Digital Functions
LC ² MOS	+5 V to ± 15 V	+3 V to ± 10 V	Wide Variety of Precision Linear and Digital Functions
HVS	+5 V to ± 22 V	+2 V to ± 18 V	High Voltage Switches, Muxes and Logic Functions

CELL LIBRARIES

Cell libraries for the bipolar CMOS processes are described below. These libraries are growing with the development of new processes, macrocells and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available Linear System Macros.

Operational amplifiers are available in bipolar, JFET and CMOS configurations. Representative bipolar op amp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC²MOS process offers JFET op amps, including an AD711 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

Digital-to-analog converters range in resolution from 8 to 14 bits, and include cells similar to the AD667 and AD1856. Analog-to-digital converters vary from 8 to 16 bits in resolution, and include cells equivalent to the AD7572 and AD674. One half-flash ADC cell converts to 8-bit accuracy in 500 nanoseconds, and one successive approximation cell converts to 12 bits in 5 microseconds.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low-voltage bandgap references comparable to the AD584 and low noise buried Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

Topology: all classical filter types

Frequency Range: 200 Hz to 20 kHz (switched-cap) or 100 Hz to 1 MHz (RC)

Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)

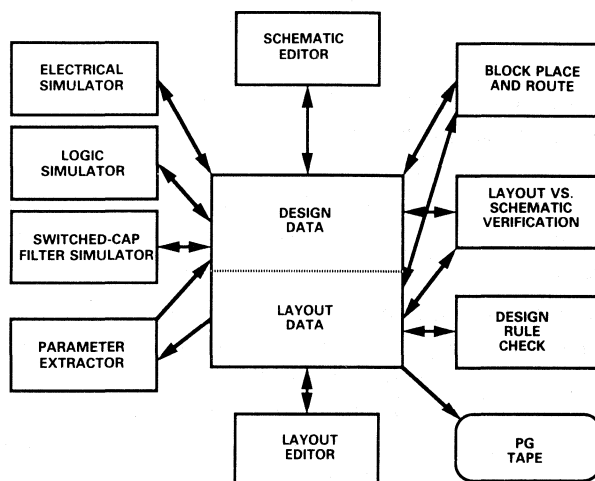
Signal/Noise and THD: >72 dB, compatible with 12-bit data acquisition.

Logic cells include gates, counters, registers, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports as well as synchronous serial ports and UARTs.

COMPUTER-AIDED DESIGN TOOLS

Designing a high performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before sign-off for final layout and fabrication.

The overall work flow through the CAD environment is shown below. Key to meeting the special challenges of mixed analog/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called JANUS, to address these issues and to implement turnkey designs.



Computer Aided Design Flow

The JANUS schematic editor offers numerous time-saving techniques, and provides for specification of such data as wire widths, routing layers, and routing priorities. It automatically generates a netlist used by subsequent tools.

Analog uses several simulators, including electrical, logic and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as op amps, or sensitive digital cells such as dynamic RAM.

Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The JANUS mixed-signal simulator combines an event-driven simulator with Newton-Raphson methods. It dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to automatically create a physical representation of the circuit schematic. This layout may be optimized through conventional interactive polygon-pushing.

The JANUS routing editor is driven by the connectivity of the schematics, but allows great freedom to manually control the routing of critical analog signal paths or power/ground lines, while autorouting non-critical nets and spacing the layout to achieve automatic enforcement of layout rules. The JANUS routing editor uses up to three interconnect levels and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, Teradyne, Hewlett Packard and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modeling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below.

This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

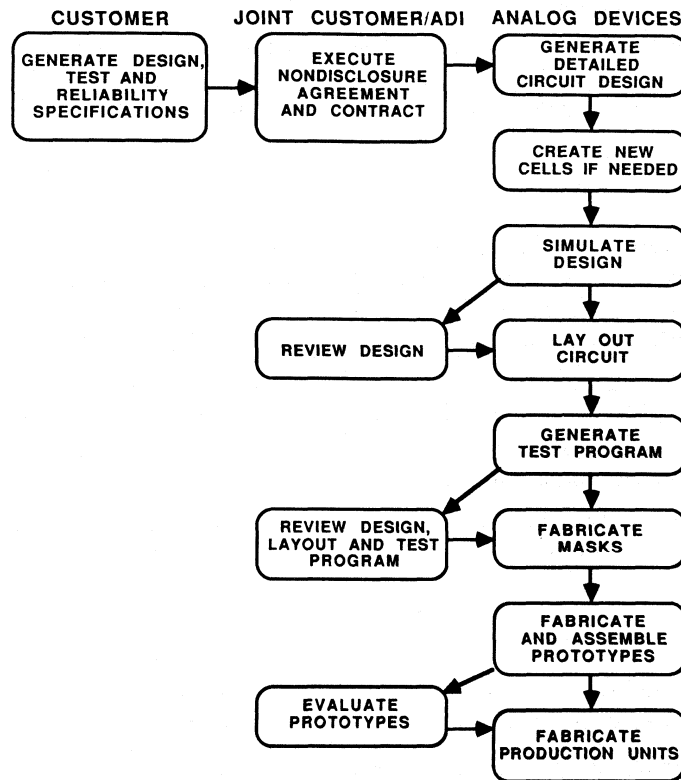
Available Packages

- Pin-grid array (PGA): 68 to 144 pins
- Leaded ceramic chip carrier (LDCC): 44 pins
- Leadless ceramic chip carrier (LCC): 20 to 68 I/Os
- Plastic quad flat pack (PQFP): 100 pins
- Plastic leaded chip carrier (PLCC): 20 to 68 pins
- Plastic dual in-line package (DIP): 14 to 64 pins
- Side-brazed DIP: 14 to 64 pins
- Frit-seal DIP (Cerdip): 14 to 40 pins
- Small outline (SO): 14 to 28 pins

PROGRAM RESPONSIBILITIES AND INTERFACES

The following figure shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices sales engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.



Program Responsibilities and Interfaces

MILITARY GRADE ASIC AND USIC CAPABILITIES

Analog Devices has produced numerous ASIC and USIC products compliant to MIL-STD-883C as well as customer source control drawings. In addition ASIC designs can be offered to Standard Military Drawings.

Appendix 1

Package Outline Information

ADI-M-1000/ADI-H-1000

	Page
Package Information Summary	1007
Package Outline Dimensions	1009

1. Introduction

2. Methodology

3. Results

Package Information Summary

		MIL-M-38510 Applicable Configuration	Page
ADI Letter Designator			
METAL CANS			
H-02A	2-Lead Metal Can		1042
H-03A	3-Lead TO-52		1043
H-03B	3-Lead TO-5 Style		1044
H-08A	8-Lead TO-99	A-1	1045
H-08B	8-Lead TO-99 Style		1046
H-10A	10-Lead TO-100	A-2	1047
H-12A	12-Lead		1048
FLAT PACKS			
F-2A	2-Lead		1036
F-100A	100-Lead		1037
SIDE BRAZED DIPS			
D-14	14-Lead	D1-3	1009
D-16	16-Lead	D2-3	1010
D-18	18-Lead	D6-3	1011
D-20	20-Lead	D8-3	1012
D-24	24-Lead	D3-3	1013
D-28	28-Lead	D10-3	1014
D-40A	40-Lead	D5-3	1015
D-48A	48-Lead		1016
D-64A	64-Lead		1017
CERDIPS			
Q-8	8-Lead	D4-1	1050
Q-14	14-Lead	D1-1	1051
Q-16	16-Lead	D2-1	1052
Q-18	18-Lead	D6-1	1053
Q-20	20-Lead	D8-1	1054
Q-24	24-Lead	D3-1	1055
Q-28	28-Lead	D10-1	1056
SIDE BRAZED DIPS			
DH-24A	24-Lead Ceramic (Small Cavity)		1021
DH-24C	24-Lead Ceramic (Large Cavity)		1023
DH-24E	24-Lead Ceramic (Large Cavity)		1024
DH-28	28-Lead Ceramic (Large Cavity)		1025
DH-32B	32-Lead "Skinny" Ceramic		1027
DH-32C	32-Lead Ceramic (Small Cavity)		1028
DH-32D	32-Lead Ceramic (Medium Cavity)		1029
BOTTOM BRAZED DIPS			
DH-14A	14-Lead Ceramic (Large Capacity)		1018
DH-14-C	14-Lead Ceramic		1020
DH-24B	24-Lead Ceramic		1022
DH-28A	28-Lead Ceramic		1026
DH-32E	32-Lead Ceramic		1030
DH-40A	40-Lead Ceramic		1031

ADI Letter Designator	Description	MIL-M-38510 Applicable Configuration	Page
METAL PLATFORM DIPS			
DH-14B	14-Lead		1019
M-24A	24-Lead		1049
LEADLESS CHIP CARRIERS			
E-20A	20-Terminal Ceramic	C-2	1032
E-28A	28-Terminal Ceramic	C-4	1033
E-52A	52-Terminal Ceramic	C-6	1034
E-68A	68-Terminal Ceramic	C-7	1035
PIN GRID ARRAY			
G-68A	68-Lead Ceramic		1038
G-84A	84-Lead Ceramic		1039
G-100A	100-Lead Ceramic		1040
G-144A	144-Lead Ceramic		1041

DIMENSIONING SYMBOLS

The symbols used are the same as those used in MIL-M-38510 Appendix-C.

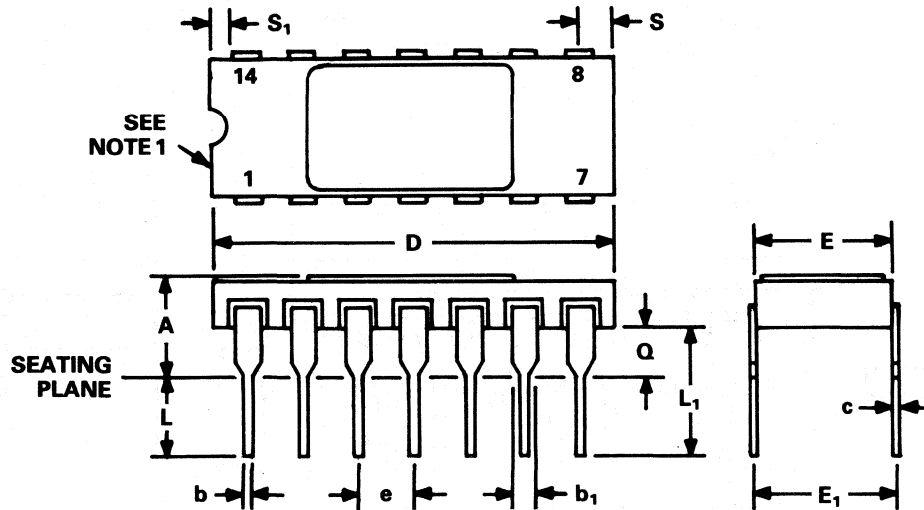
To designate a dimension of a diameter, the lower case Greek letter ϕ (phi) will be added as a prefix to the dimension symbol.

- A— Body dimensions.
- ϕb — Terminal lead diameters.
- b— Terminal lead widths.
- c— Terminal lead thicknesses.
- ϕD — Body diameters.
- D— Body lengths.
- E— Body widths.
- e— Terminal lead spacings.
- F— Flange dimensions.
- k— Index dimensions, lengths.
- L— Terminal lead lengths.
- Q— Standoff height. The height from the seating plane or a reference plane parallel to the seating plane.
- R— Radius dimensions.
- S— Distance between terminal leads and the body end.
- α — Angular dimensions.

Package Outline Dimensions

D-14

14-Pin Side Brazed

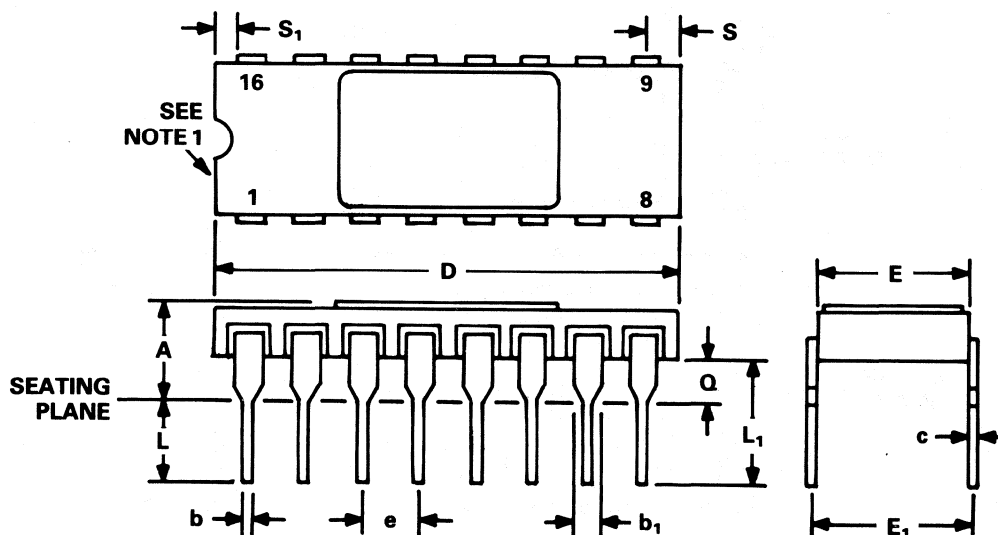


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twelve spaces.

D-16
16-Pin Side Brazed



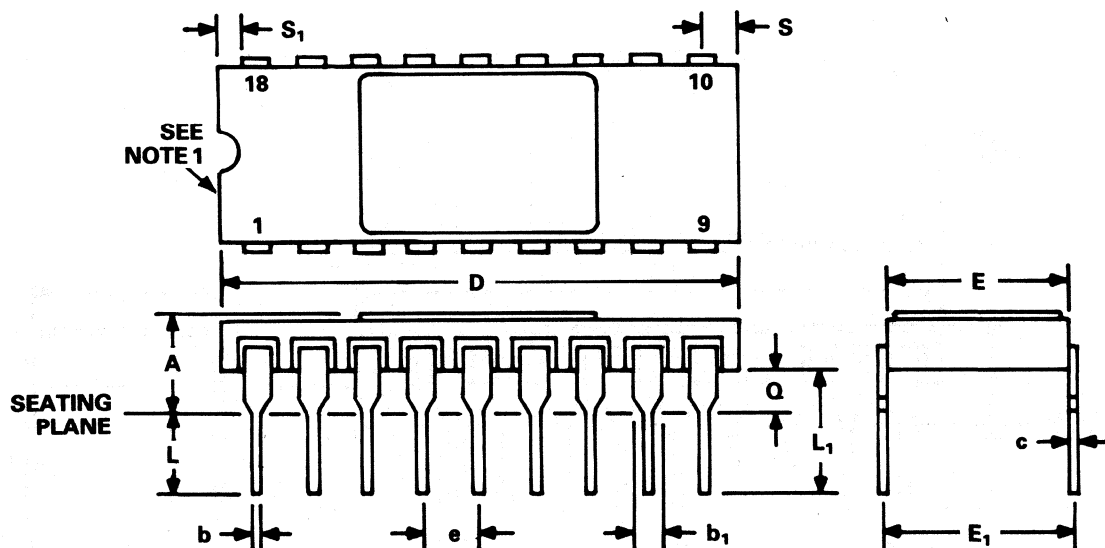
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b ₁	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L ₁	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S ₁	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

D-18

18-Pin Side Brazed

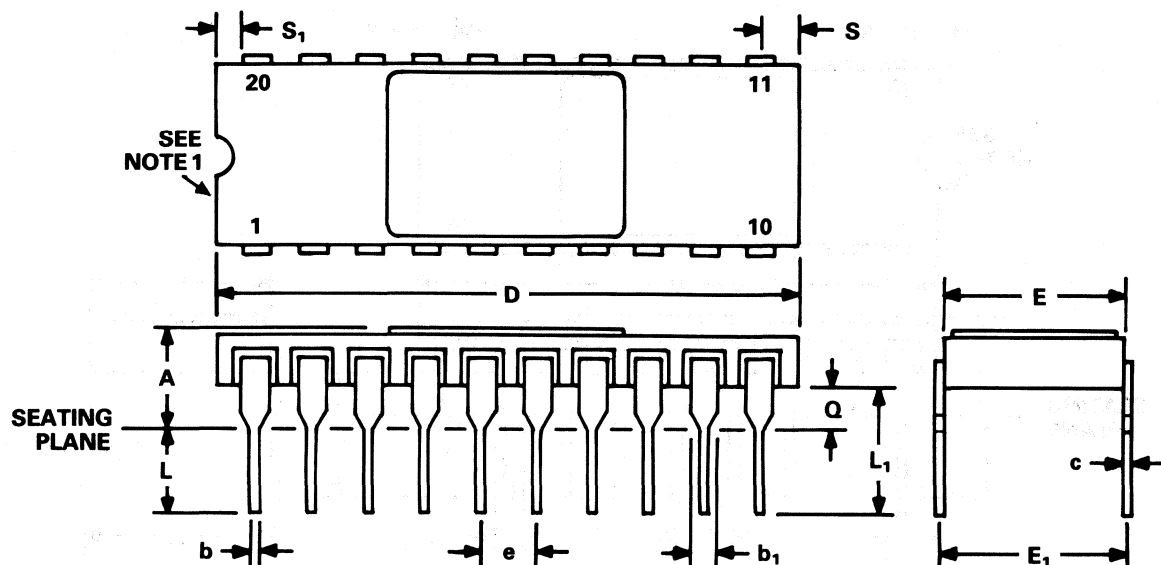


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b ₁	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L ₁	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S ₁	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

D-20
20-Pin Side Brazed

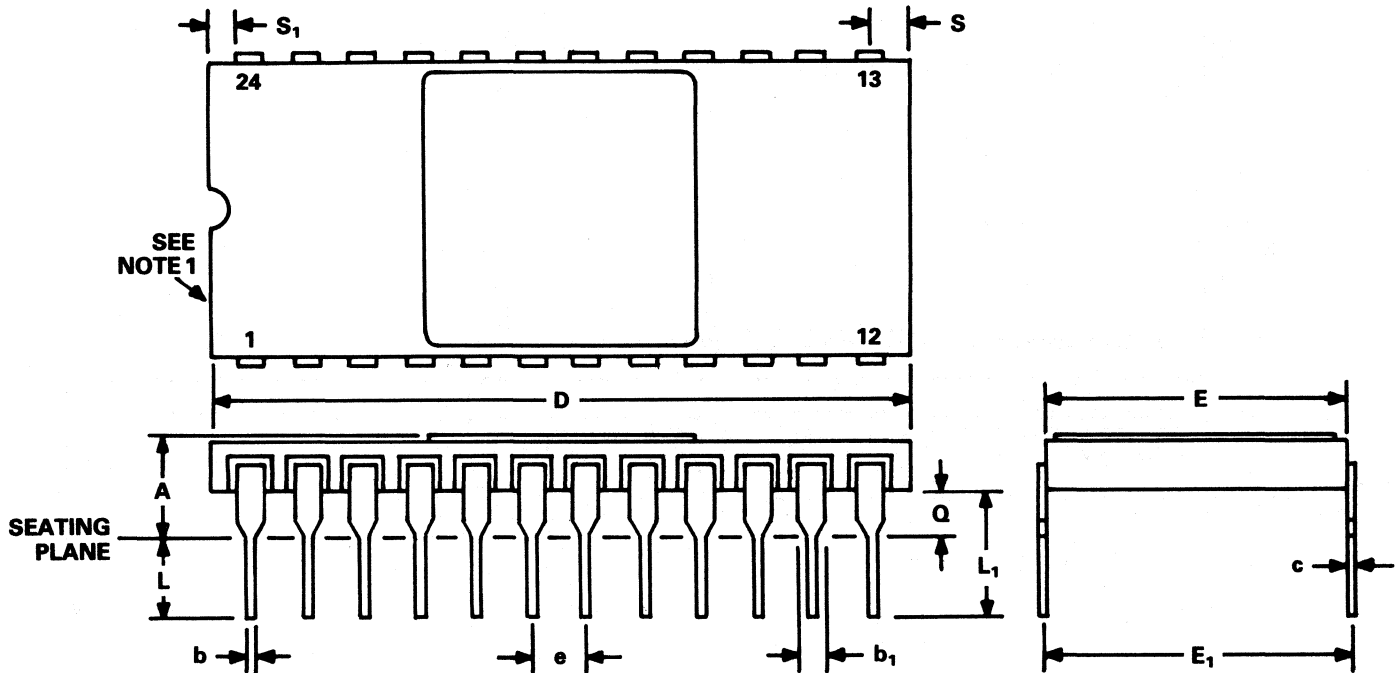


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Eighteen spaces.

D-24
24-Pin Side Brazed

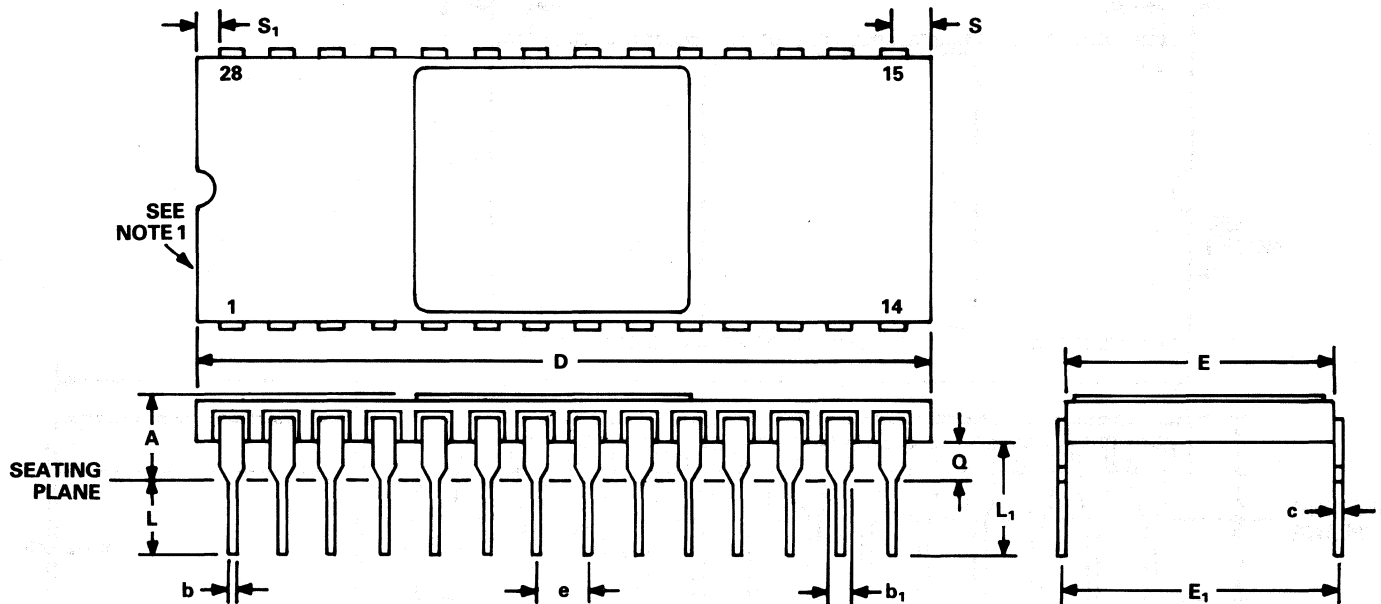


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.290		32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.100 BSC		2.54 BSC		7
L	0.120	0.200	3.05	5.08	
L_1	0.150		3.81		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

D-28
28-Pin Side Brazed

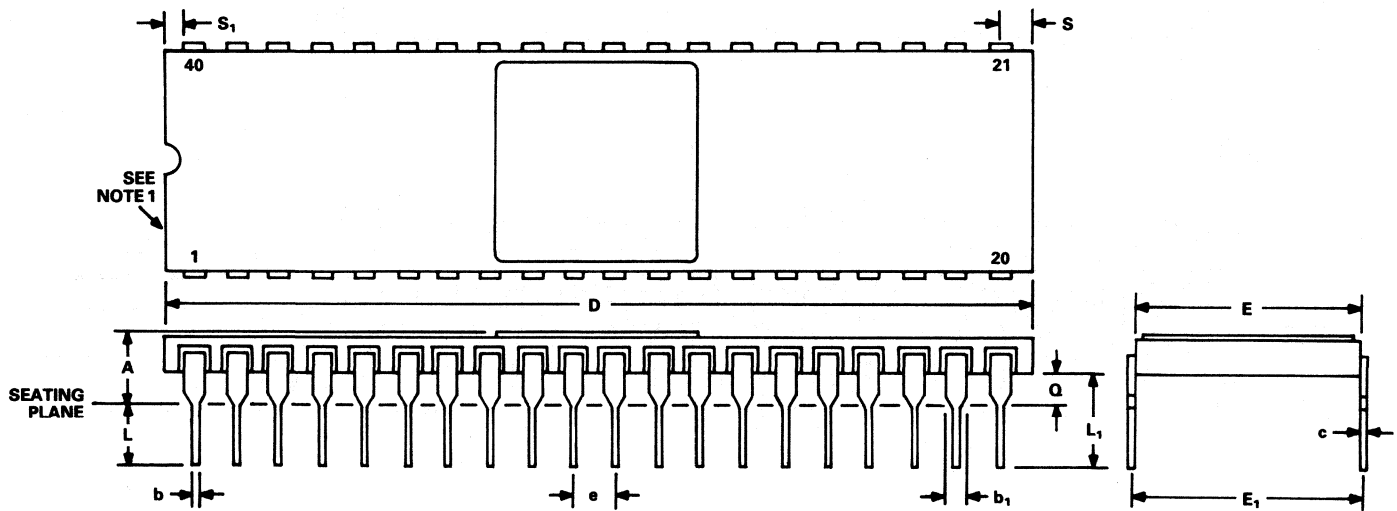


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.232		5.84	
b	0.014	0.023	0.36	0.58	6
b_1	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.100		2.54	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

D-40A
40-Pin Side Brazed

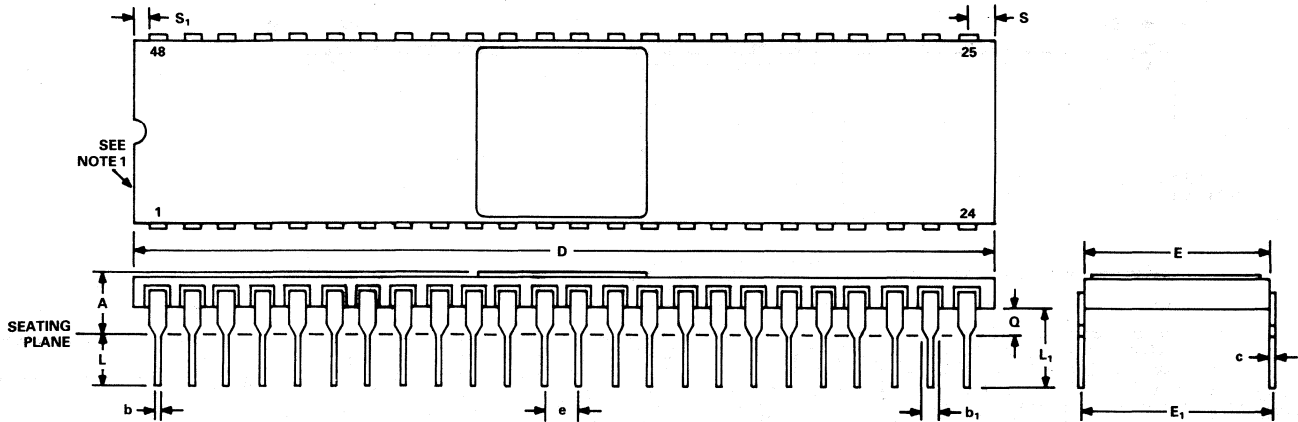


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b ₁	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		2.096		53.24	4
E	0.510	0.620	12.95	15.75	4
E ₁	0.590	0.630	13.21	16.00	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L ₁	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S ₁	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Thirty-eight spaces.

D-48A
48-Pin Side Brazed

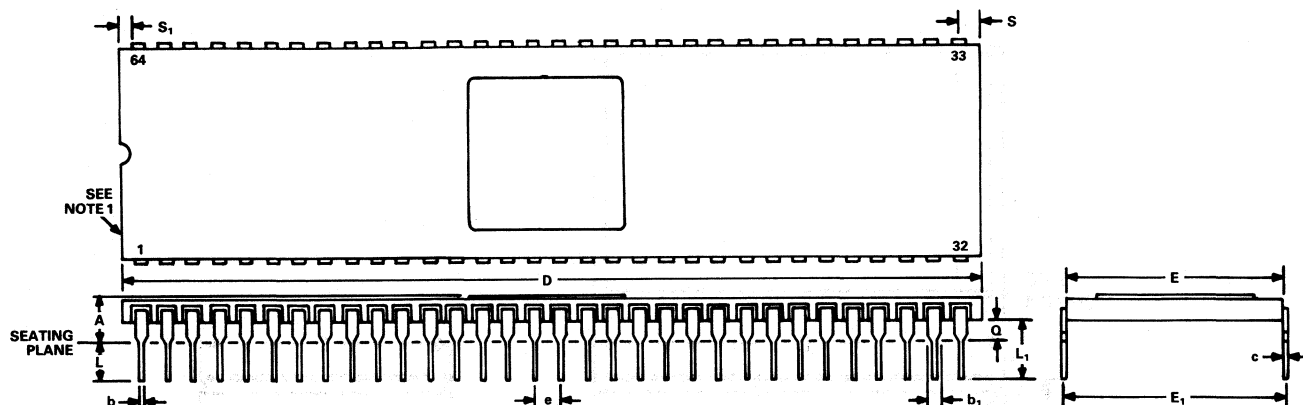


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b ₁	0.038	0.065	0.96	1.65	2, 6
c	0.008	0.015	0.20	0.38	6
D		2.450		62.23	4
E	0.590	0.620	12.95	15.75	4
E ₁	0.520	0.630	13.21	16.00	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L ₁	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S ₁	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Forty-six spaces.

D-64A
64-Pin Side Brazed

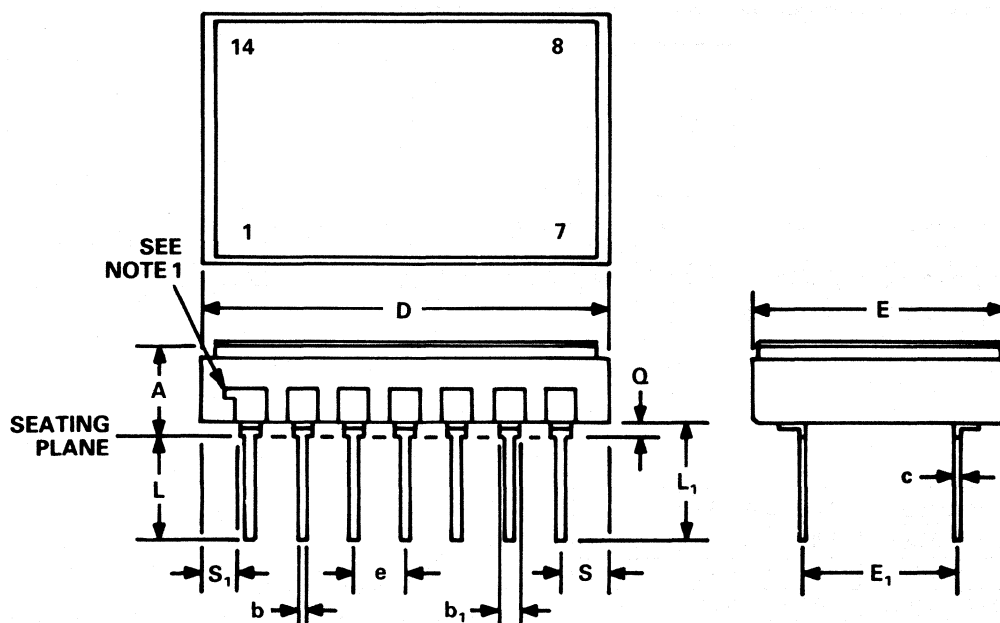


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b ₁	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		3.24		82.30	4
E	0.870	0.920	20.33	23.37	4
E ₁	0.880	0.940	22.35	23.88	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L ₁	0.150		3.81		
Q	0.015	0.07	0.38	1.67	3
S		0.100		2.49	5
S ₁	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixty-two spaces.

DH-14A
14-Pin Bottom Brazed Ceramic Platform



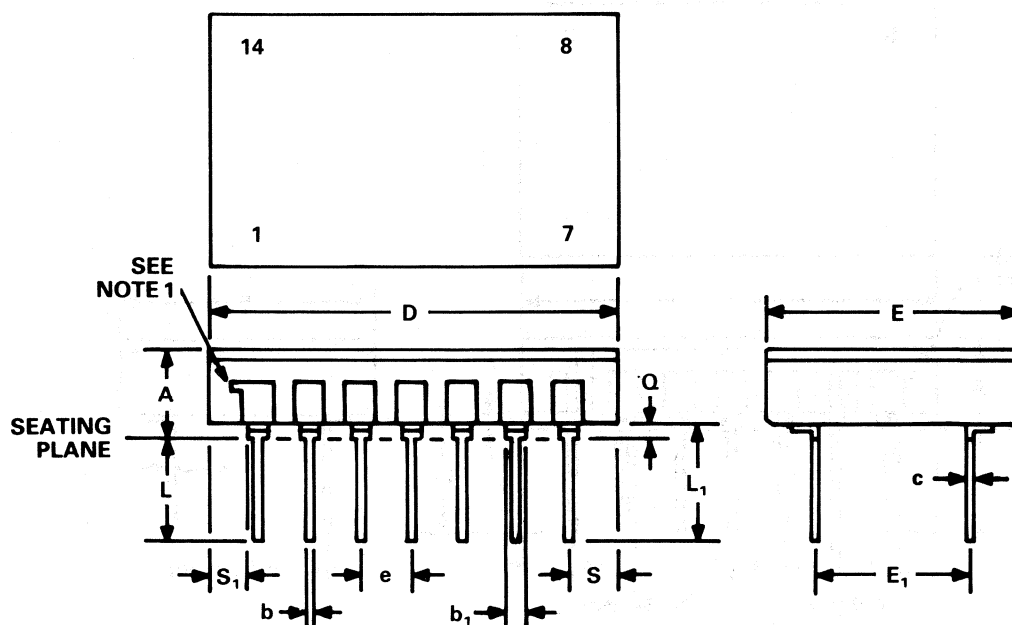
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		0.805		20.45	
E	0.480	0.505	12.19	12.83	
E ₁	0.290	0.320	7.37	8.13	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.125	0.200	3.18	5.08	
L ₁	0.180		4.57		
Q	0.015	0.040	0.38	1.02	2
S		0.098		2.49	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twelve spaces.

DH-14B

14-Pin Bottom Brazed Ceramic (Large Capacity)

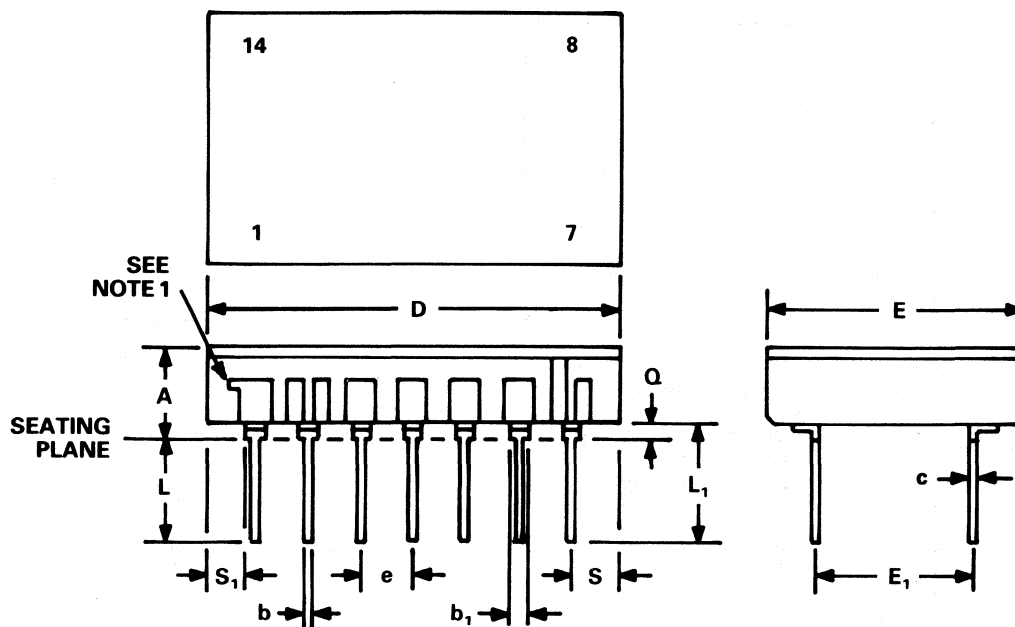


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.220	3.56	5.59	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D	0.835	0.875	21.21	22.23	
E	0.480	0.510	12.19	12.95	
E ₁	0.295	0.305	7.49	7.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.150	0.200	3.05	5.08	
L ₁	0.180		4.57		
Q	0.015	0.035	0.38	1.91	2
S		0.137		3.48	4
S ₁	0.060		1.52		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twelve spaces.

DH-14C
14-Pin Bottom Brazed Ceramic

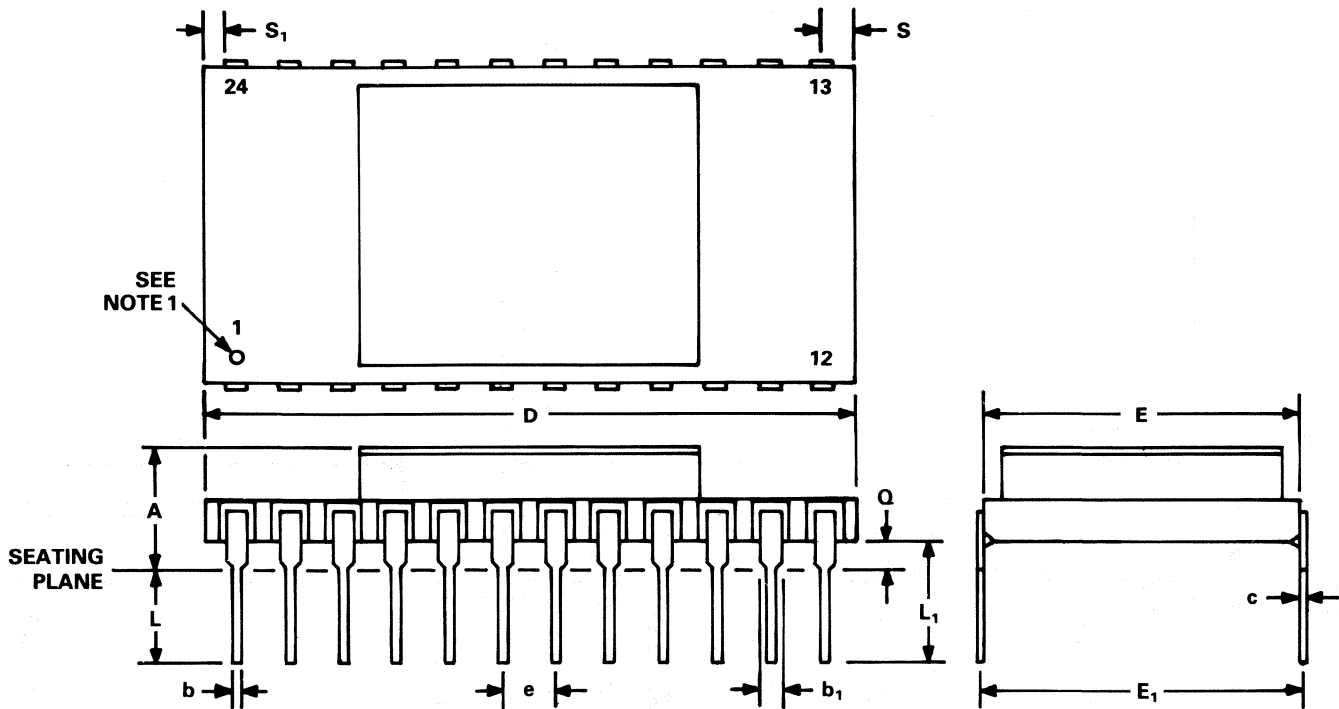


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.200	3.56	5.08	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D	0.770	0.810	19.56	20.57	
E	0.480	0.510	12.19	12.95	
E ₁	0.295	0.305	7.49	7.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.150	0.200	3.81	5.08	
L ₁	0.180		4.57		
Q	0.015	0.035	0.38	0.89	2
S		0.137		3.48	4
S ₁	0.060		1.52		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twelve spaces.

DH-24A
24-Pin Side Brazed (Small Cavity)

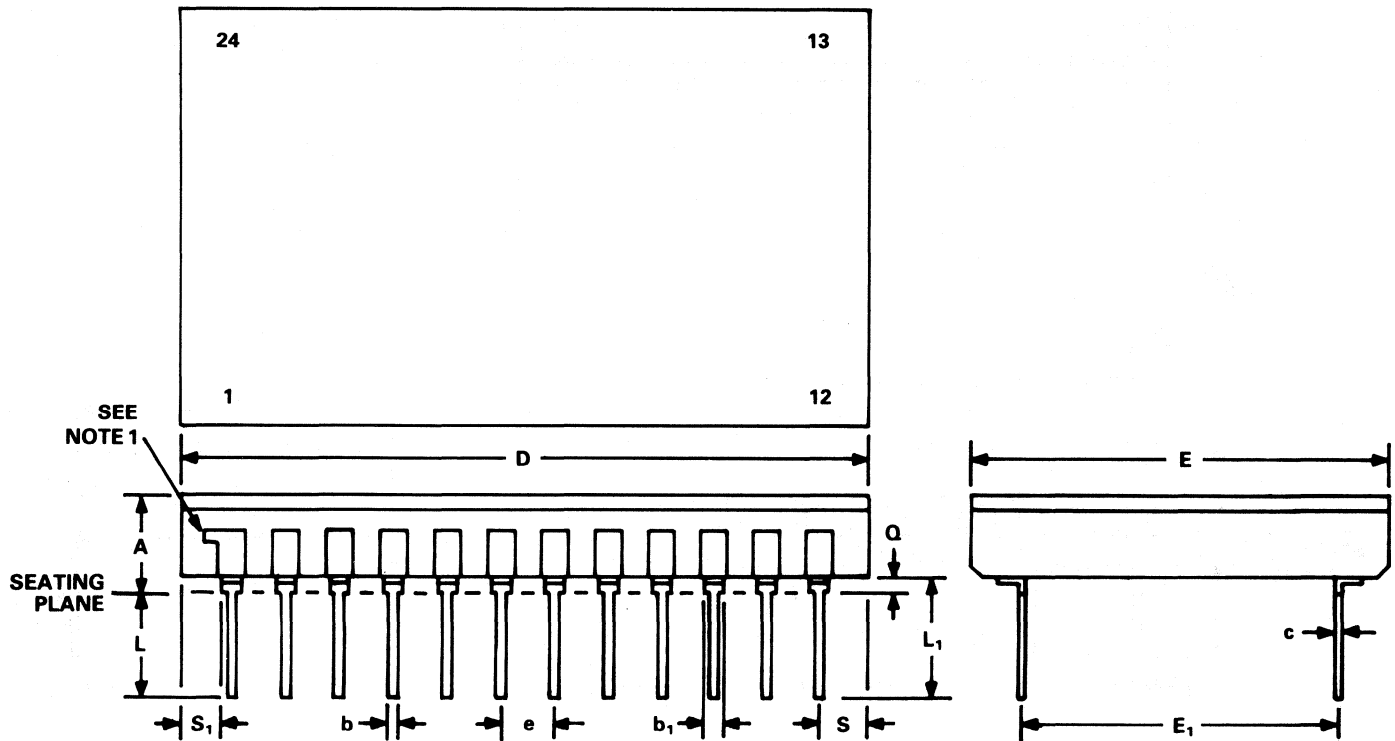


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b ₁	0.038	0.065	0.96	1.65	
c	0.008	0.015	0.20	0.38	
D		1.212		29.69	
E	0.580	0.600	14.21	14.70	
E ₁	0.590	0.620	14.99	15.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120	0.200	3.05	5.08	
L ₁	0.180		4.57		
Q	0.015	0.075	0.38	1.91	2
S		0.098		2.49	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twenty-two spaces.

DH-24B
24-Pin Bottom Brazed Ceramic Platform



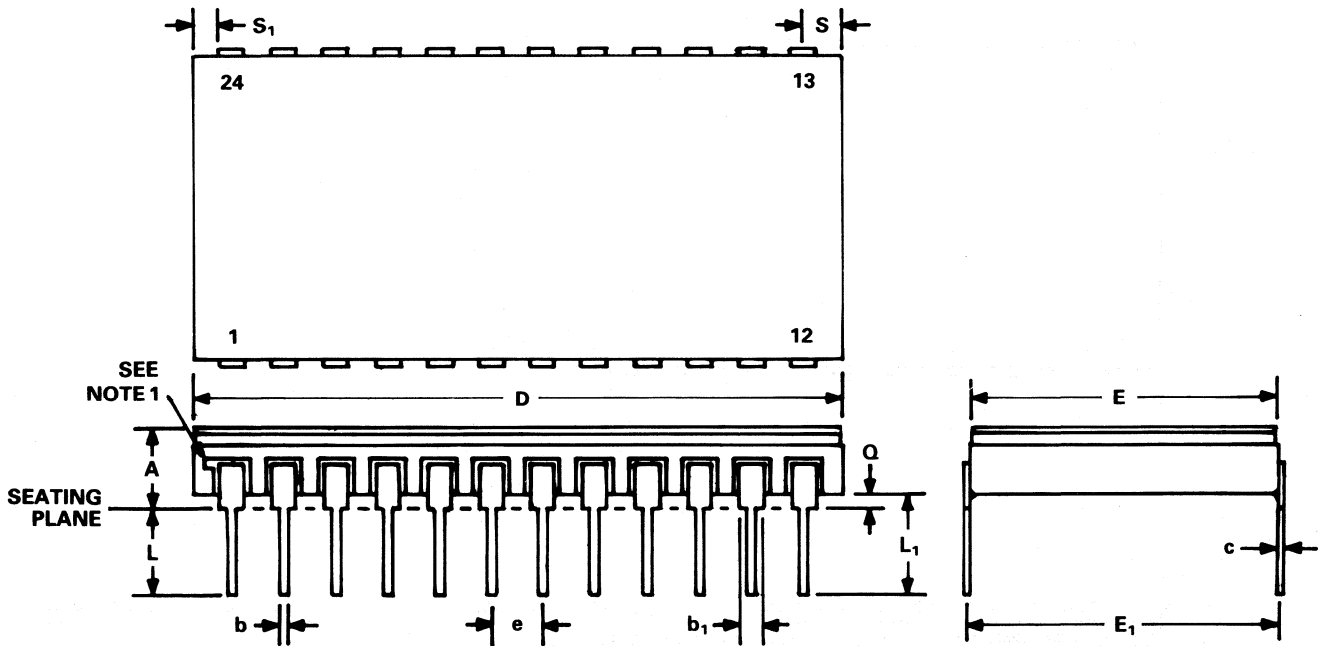
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		1.320		33.53	
E	0.770	0.810	19.56	20.57	
E ₁	0.550	0.620	14.99	15.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120	0.200	3.05	5.08	
L ₁	0.180		4.57		
Q	0.015	0.075	0.38	1.91	2
S		0.098		2.49	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twenty-two spaces.

DH-24C

24-Pin Side Brazed (Large Cavity)



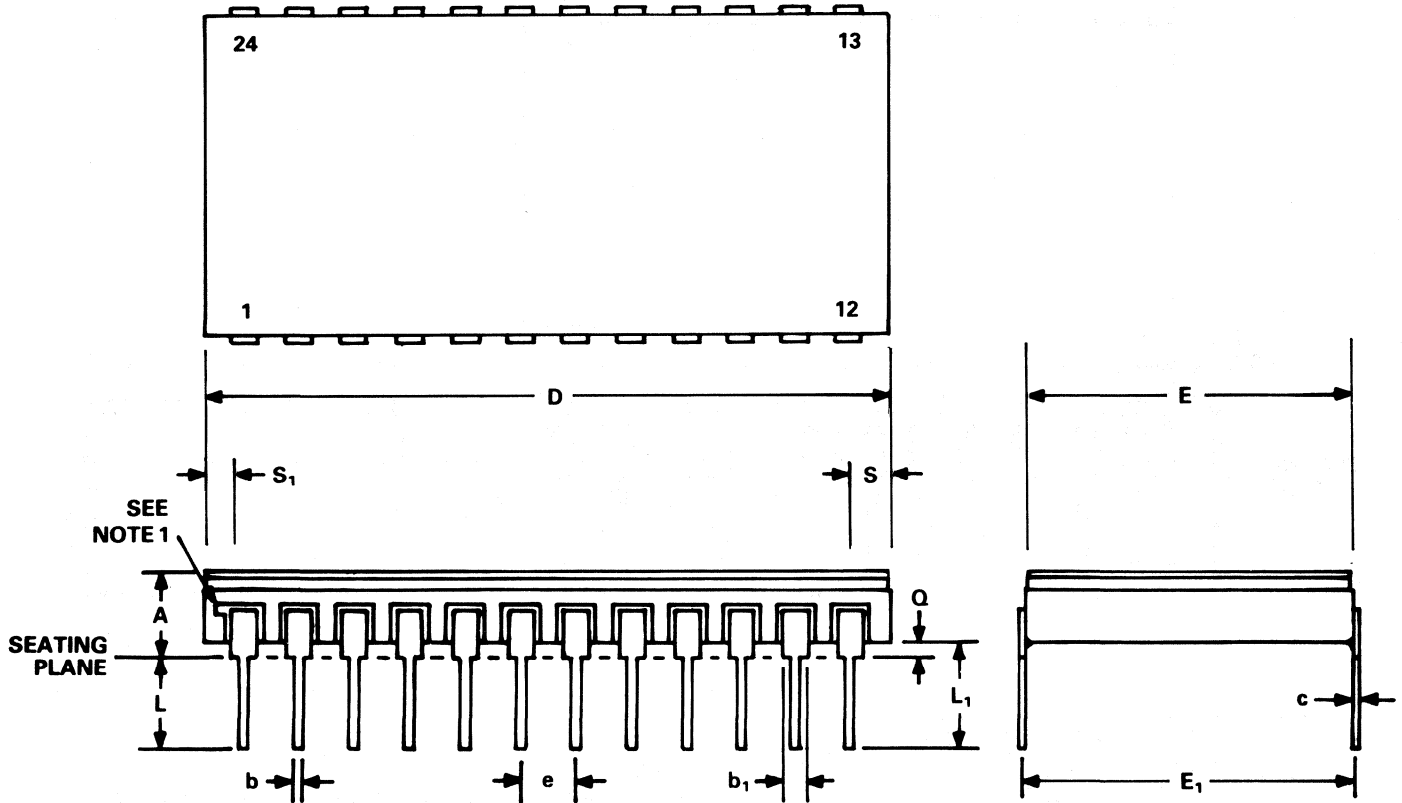
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.245		6.22	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		1.270		31.11	
E	0.585	0.610	14.33	15.49	
E ₁	0.590	0.620	14.99	15.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120	0.200	3.05	5.08	
L ₁	0.180		4.57		
Q	0.015	0.075	0.38	1.91	2
S		0.098		2.49	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twenty-two spaces.

DH-24E

24-Pin Side Brazed (Large Cavity)



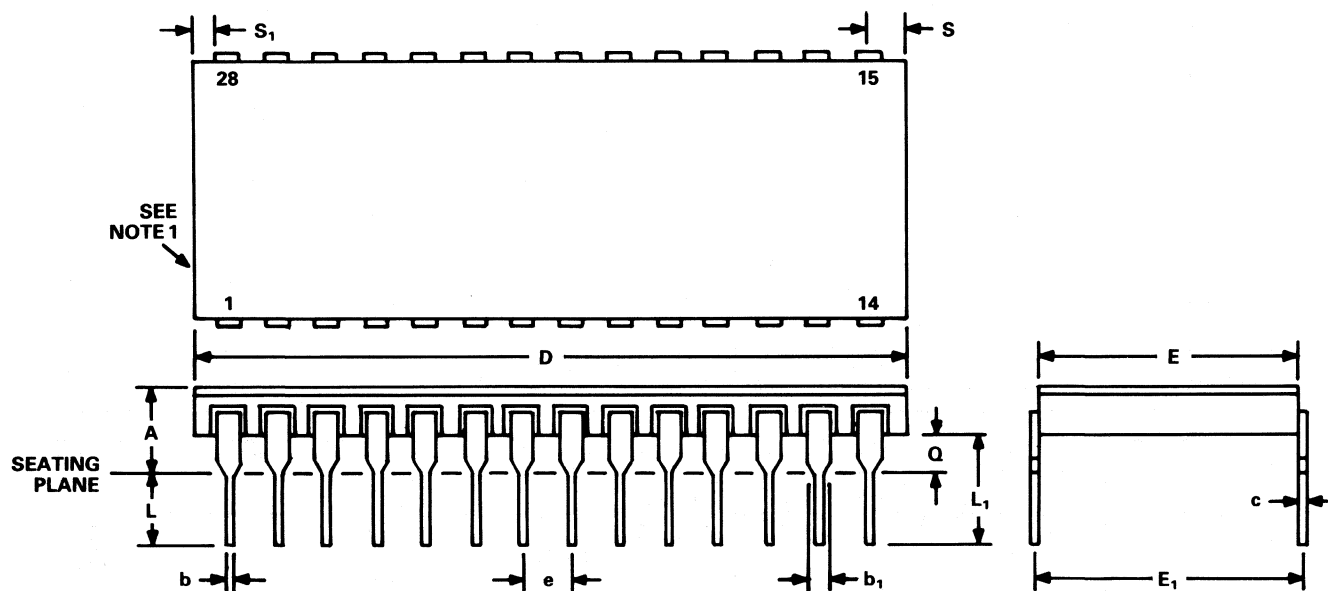
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.245		6.22	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		1.270		31.11	
E	0.585	0.610	14.33	15.49	
E ₁	0.590	0.620	14.99	15.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120	0.200	3.05	5.08	
L ₁	0.180		4.57		
Q	0.015	0.075	0.38	1.91	2
S		0.098		2.49	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of all the leads.
6. Twenty-two spaces.

REV. A

DH-28
28-Pin Seam Seal

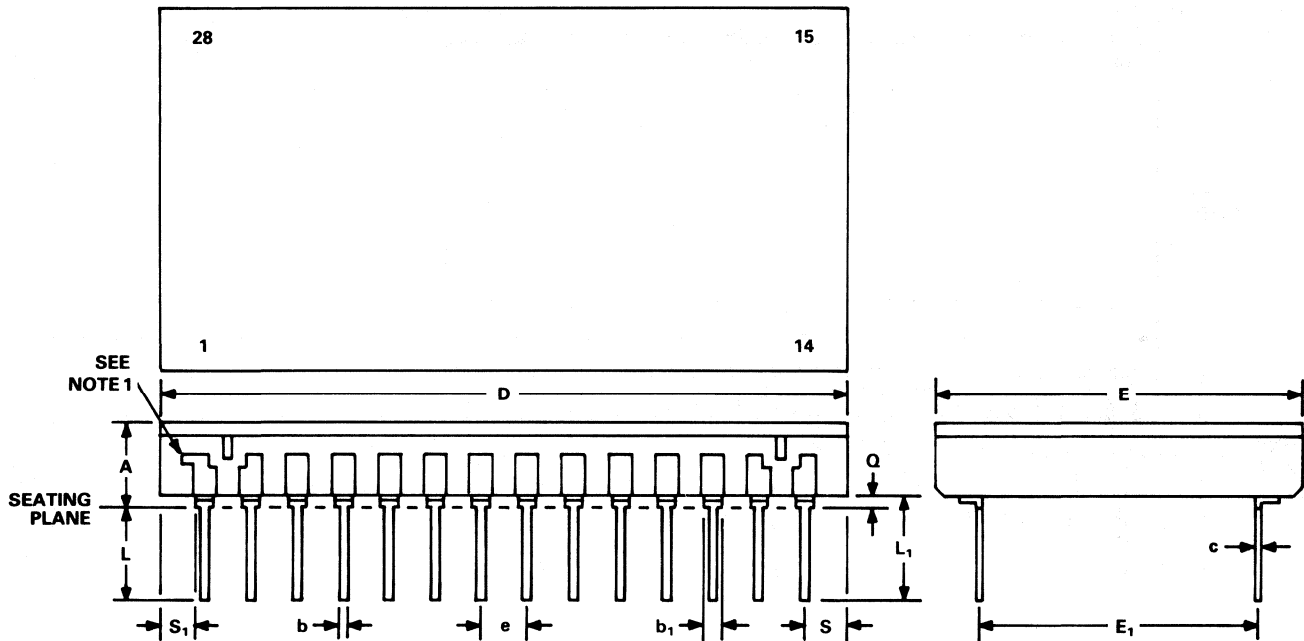


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		1.414		34.64	
E	0.580	0.610	14.73	15.49	
E_1	0.590	0.610	14.99	15.49	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	2
S		0.098		2.49	4
S_1	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E_1 shall be measured at the centerline of the leads.
6. Twenty-six spaces.

DH-28A
28-Pin Bottom Brazed Ceramic

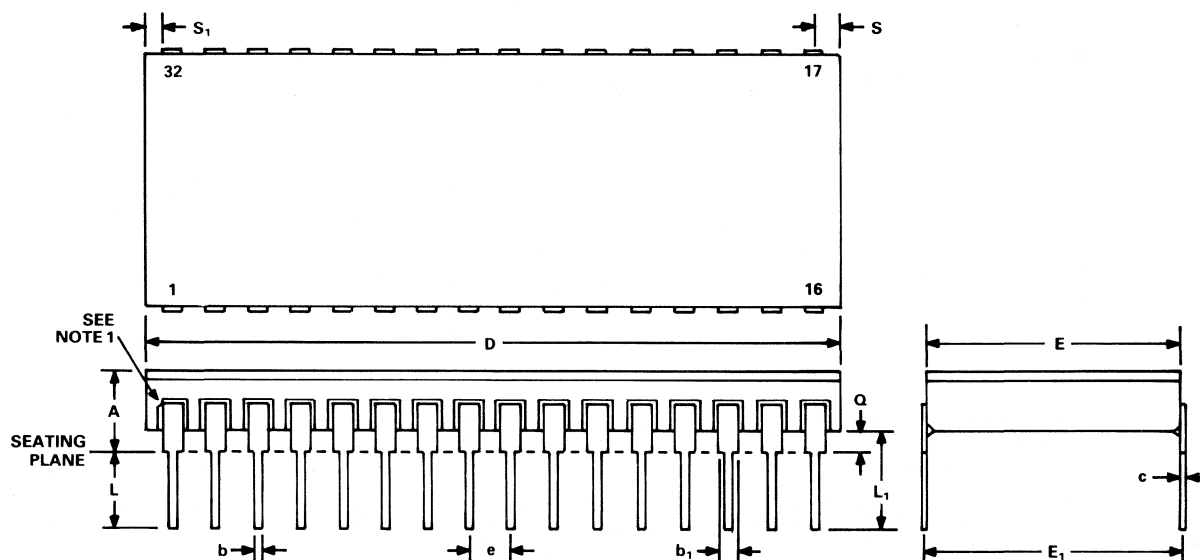


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		1.575		40.00	
E	0.770	0.810	19.56	20.57	
E ₁	0.590	0.610	14.99	15.49	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.150	0.200	3.81	5.08	
L ₁	0.180		4.57		
Q	0.015	0.035	0.38	0.89	2
S		0.137		3.48	4
S ₁	0.100		2.54		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Twenty-six spaces.

DH-32B
32-Pin Side Brazed (Large Cavity)

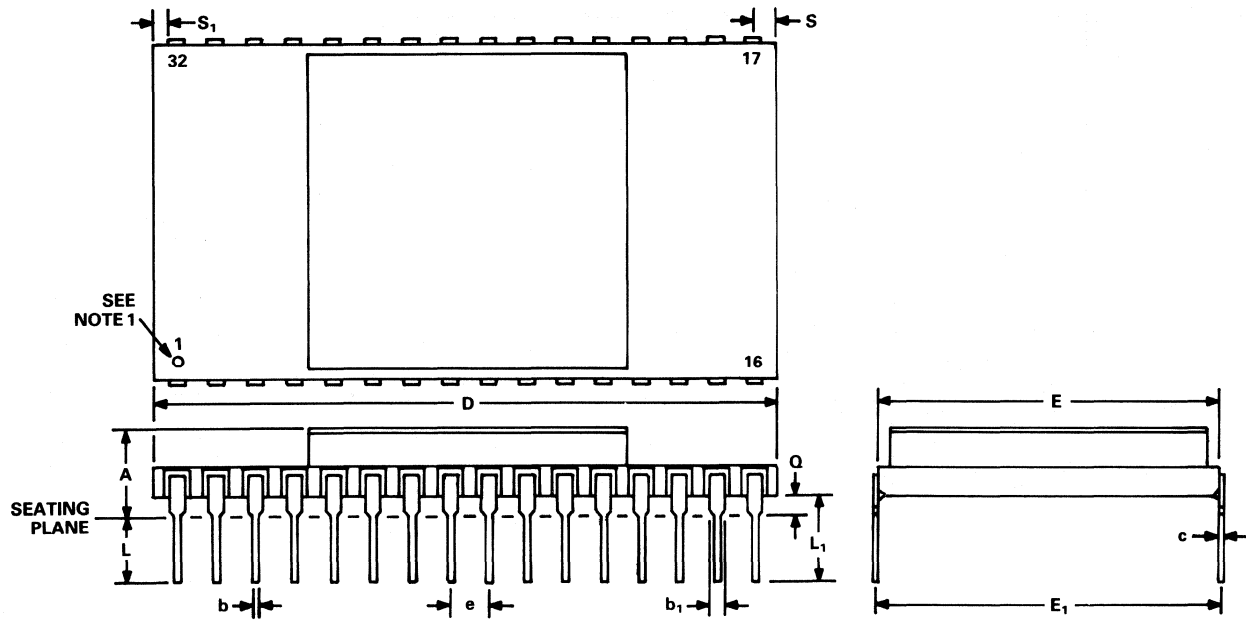


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.230		5.84	
b	0.016	0.020	0.41	0.51	
b ₁	0.045	0.055	1.14	1.40	
c	0.009	0.012	0.23	0.31	
D	1.584	1.640	40.64	41.66	
E	0.580	0.605	14.73	15.24	
E ₁	0.590	0.610	14.99	15.49	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.125	0.175	3.18	4.44	
L ₁	0.180		4.57		
Q	0.040	0.060	1.02	1.52	2
S		0.080		2.03	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Thirty spaces.

DH-32C
32-Pin Side Brazed (Small Cavity)



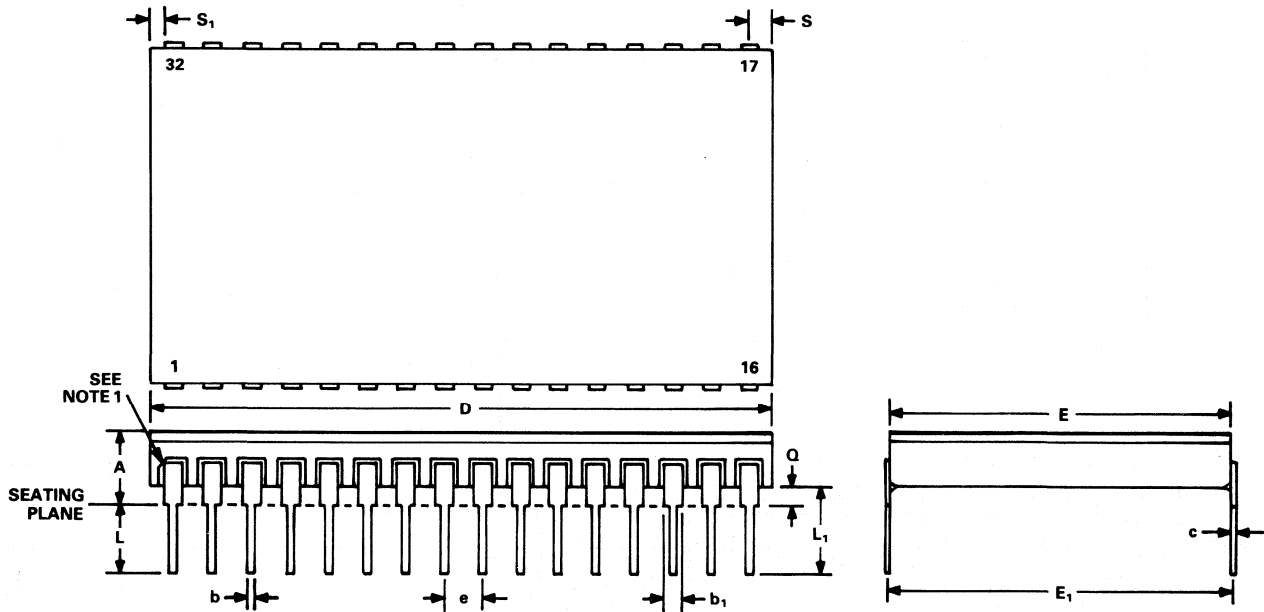
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b ₁	0.035	0.055	0.89	1.40	
c	0.009	0.012	0.23	0.31	
D		1.620		41.14	
E	0.870	0.910	22.10	23.11	
E ₁	0.890	0.930	22.61	23.62	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.150	0.180	3.81	4.57	
L ₁	0.190	0.230	4.83	5.84	
Q	0.015	0.060	1.02	1.52	2
S		0.098		2.49	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Thirty spaces.

DH-32D

32-Pin Side Brazed (Medium Cavity)

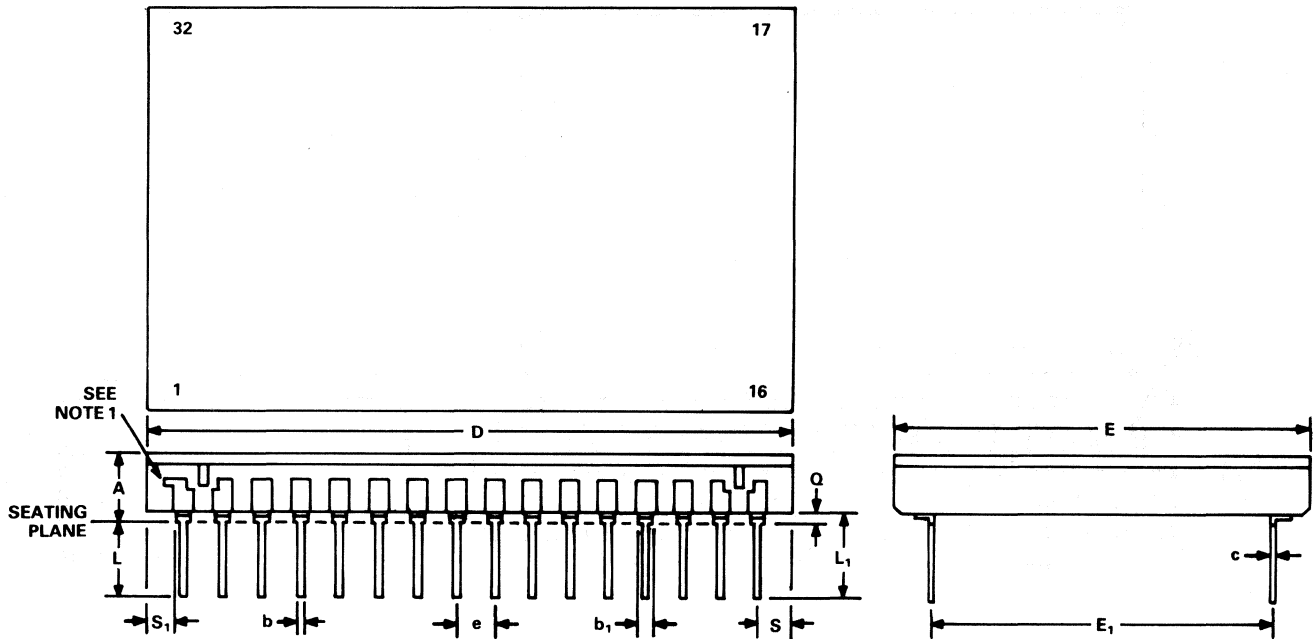


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.230		5.84	
b	0.016	0.020	0.41	0.51	
b ₁	0.045	0.055	1.14	1.40	
c	0.009	0.012	0.23	0.31	
D	1.584	1.640	40.64	41.66	
E	0.880	0.905	22.35	22.99	
E ₁	0.910	0.930	23.11	23.62	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.125	0.175	3.18	4.44	
L ₁	0.180		4.57		
Q	0.040	0.060	1.02	1.52	2
S		0.080		2.03	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads.
6. Thirty spaces.

DH-32E
32-Pin Bottom Brazed Ceramic

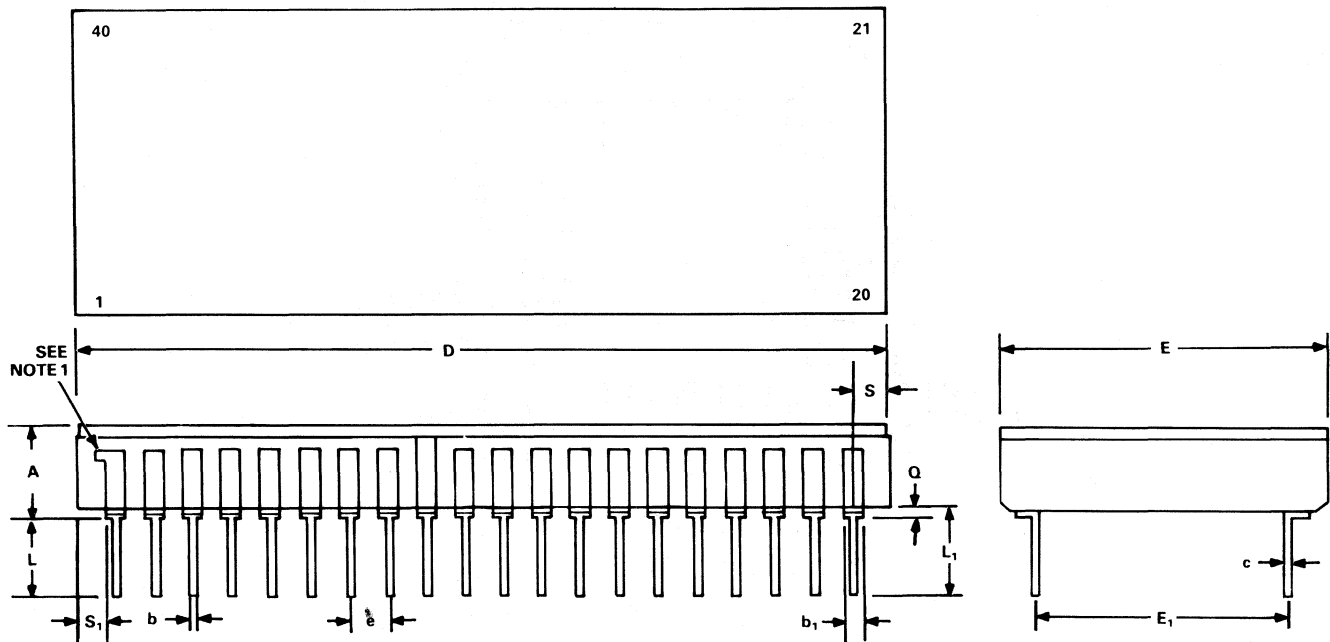


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		1.750		44.31	
E	1.075	1.105	27.31	28.07	
E ₁	0.890	0.910	22.61	23.10	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120	0.160	3.05	4.06	
L ₁	0.145	0.185	3.68	4.69	
Q	0.015	0.025	0.38	0.63	2
S		0.120		3.05	4
S ₁	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E₁ shall be measured at the centerline of the leads at standoff.
6. Thirty spaces.

DH-40A
40-Pin Bottom Brazed Ceramic DIP



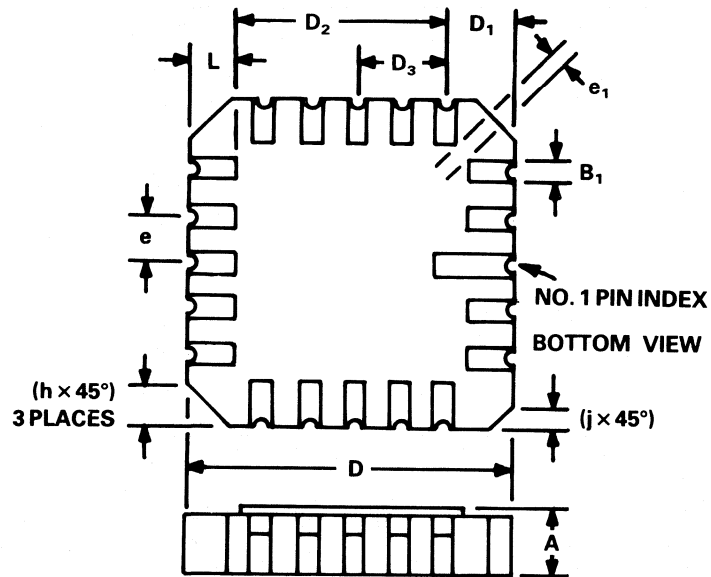
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.225	4.32	5.72	
b	0.014	0.023	0.36	0.58	
b ₁	0.030	0.050	0.76	1.27	2
c	0.008	0.015	0.20	0.38	
D	2.070	2.120	52.58	53.85	
E	0.770	0.810	19.56	20.57	
E ₁	0.580	0.620	14.73	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120	0.200	3.05	5.08	
L ₁	0.140	0.230	3.56	5.84	
Q	0.015	0.045	0.38	1.02	3
S		0.098		2.49	5
S ₁	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E₁ shall be measured at the centerline of all the leads.
7. Thirty-eight spaces.

E-20A

20-Terminal Leadless Chip Carrier



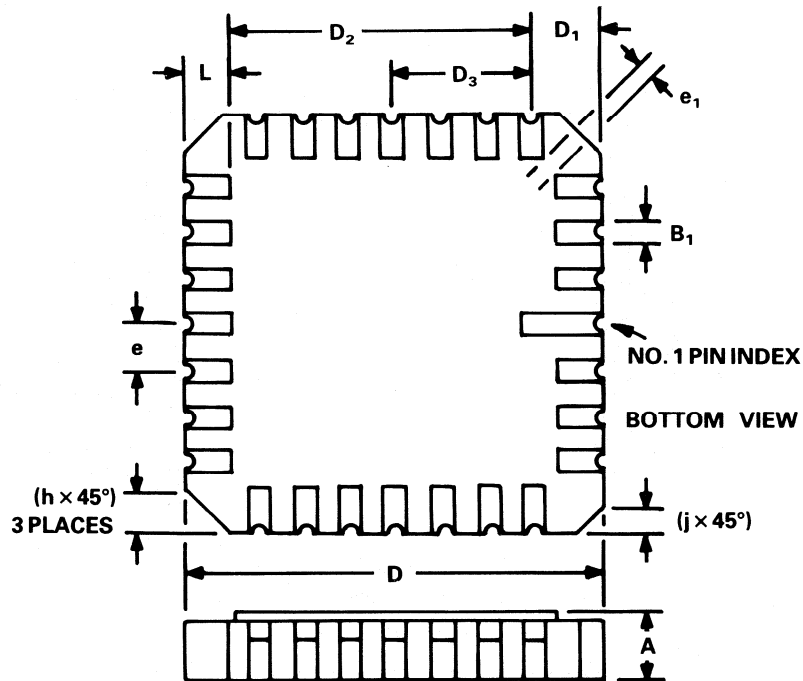
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	1
B ₁	0.022	0.028	0.56	0.71	
D	0.342	0.358	8.69	9.09	2
D ₁	0.075 REF		1.91 REF		3
D ₂	0.200 BSC		5.08 BSC		
D ₃	0.100 BSC		2.54 BSC		
e	0.050 BSC		1.27 BSC		
e ₁	0.015		0.381		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES

1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.

E-28A

28-Terminal Leadless Chip Carrier



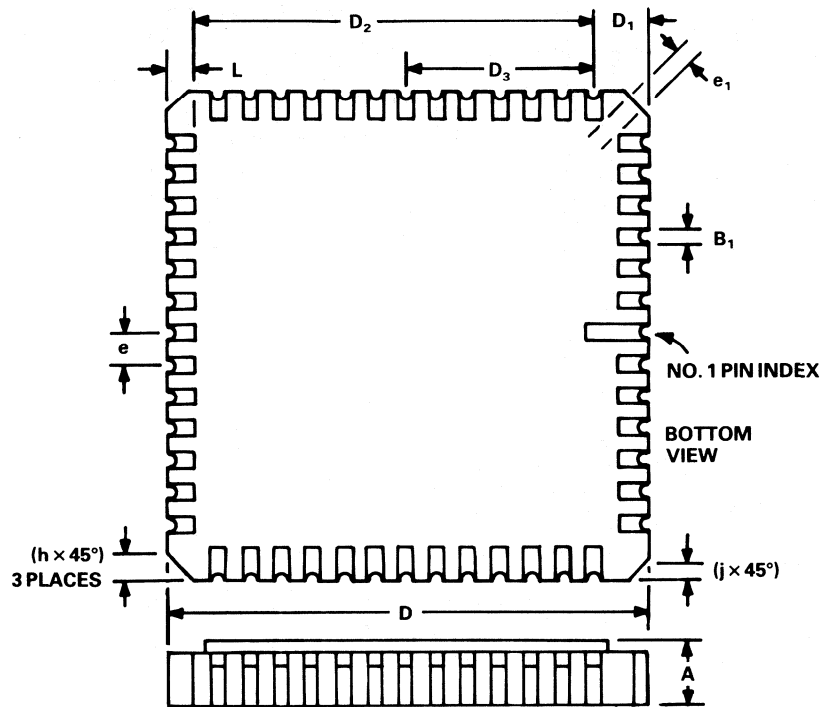
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	1
B ₁	0.022	0.028	0.56	0.71	
D	0.442	0.460	11.23	11.68	2
D ₁	0.075 REF		1.91 REF		3
D ₂	0.300 BSC		7.62 BSC		
D ₃	0.150 BSC		3.81 BSC		
e	0.050 BSC		1.27 BSC		
e ₁	0.015		0.381		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES

1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.

E-52A

52-Terminal Leadless Chip Carrier

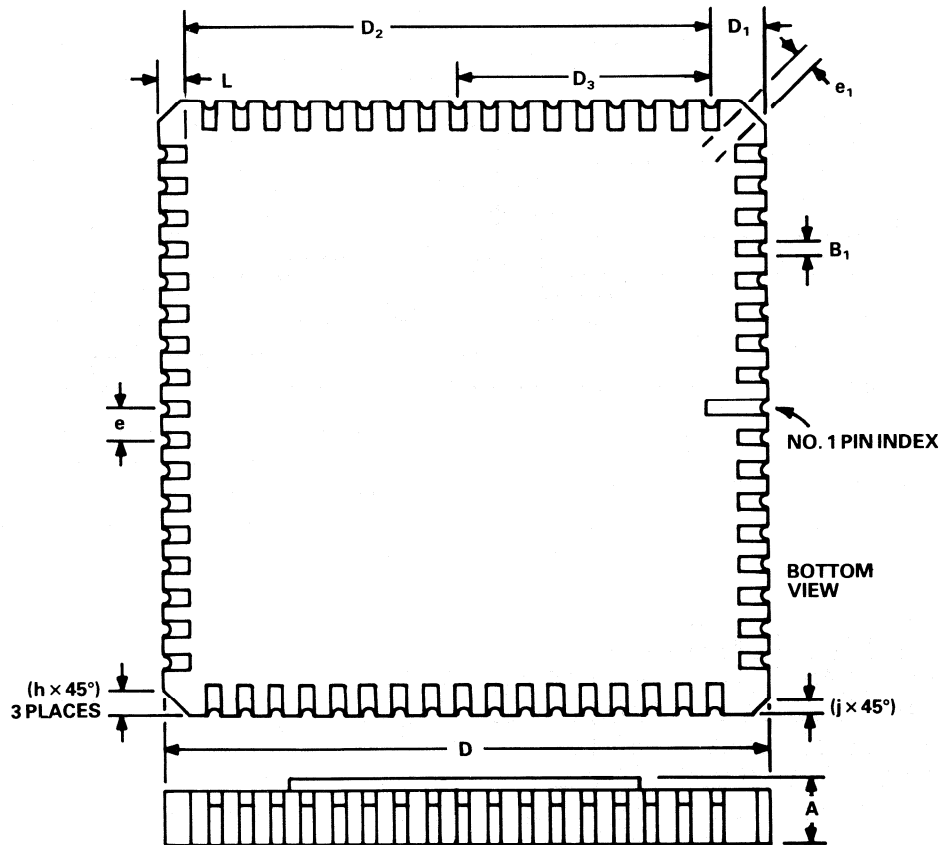


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.082	0.120	2.08	3.05	1
B ₁	0.022	0.028	0.56	0.71	
D	0.739	0.761	18.77	19.33	2
D ₁	0.075 REF		1.91 REF		3
D ₂	0.600 BSC		15.24 BSC		
D ₃	0.300 BSC		7.62 BSC		
e	0.050 BSC		1.27 BSC		
e ₁	0.015		0.381		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES

1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.

E-68A
68-Terminal Leadless Chip Carrier

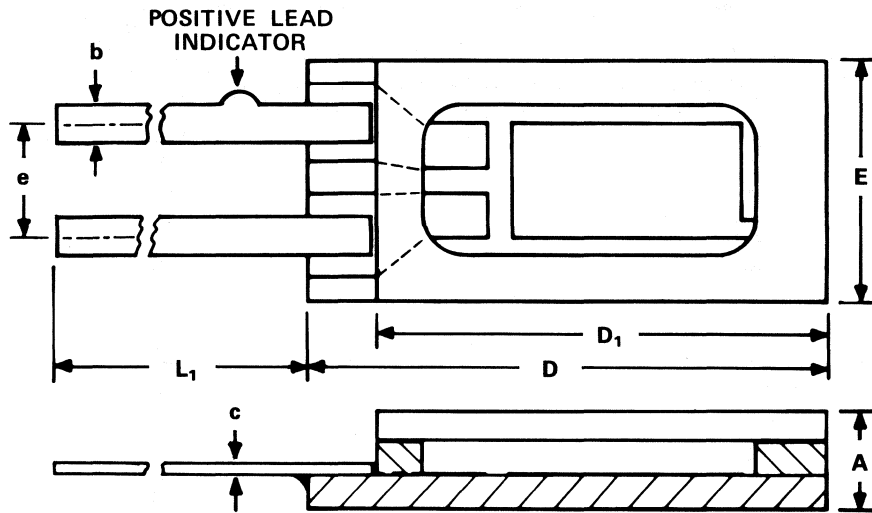


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.082	0.120	2.08	3.05	1
B ₁	0.022	0.028	0.56	0.71	
D	0.938	0.962	23.83	24.43	2
D ₁	0.075	REF	1.91	REF	3
D ₂	0.800	BSC	20.32	BSC	
D ₃	0.400	BSC	10.16	BSC	
e	0.050	BSC	1.27	BSC	
e ₁	0.015		0.381		
j	0.020	REF	0.51		
h	0.040	REF	1.02		
L	0.045	0.055	1.14	1.40	

NOTES

1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.

F-2A
2-Lead Flat Pack

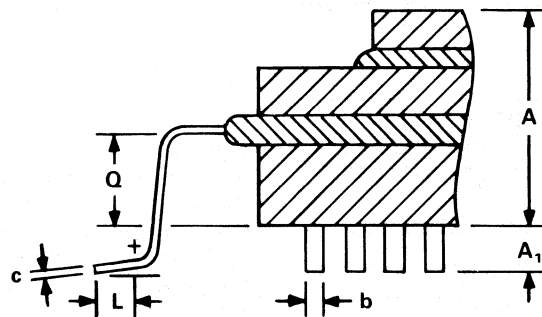
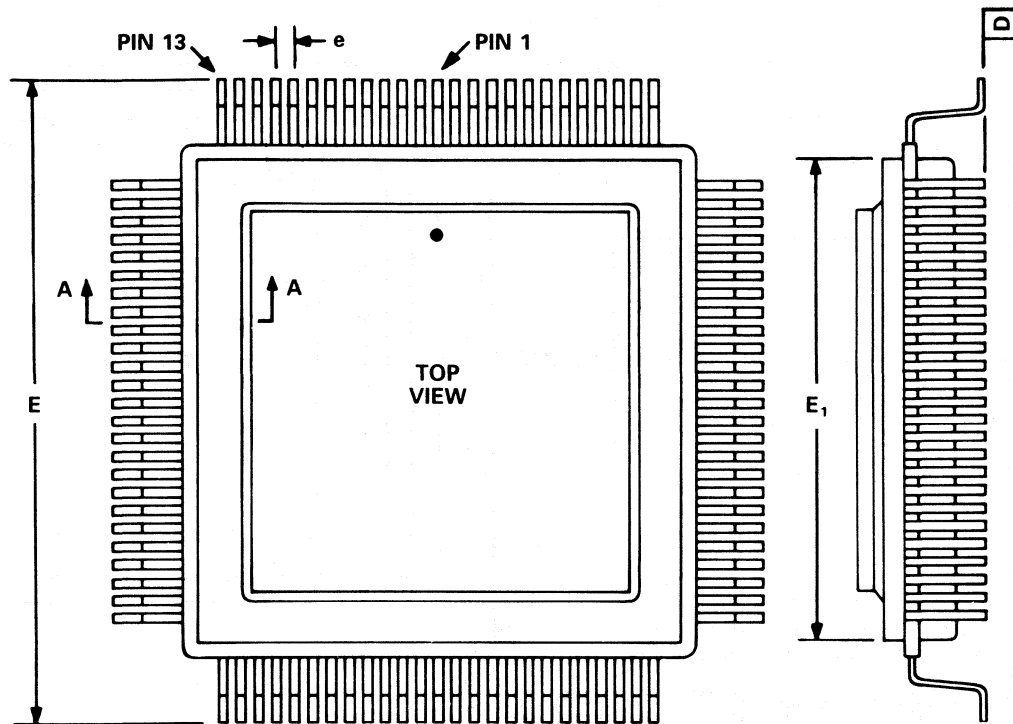


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.044	0.066	1.12	1.67	
b	0.015	0.019	0.38	0.48	
c	0.0045	0.0065	0.12	0.17	
D		0.250		6.35	1
D ₁		0.220		5.59	
E	0.081	0.093	2.06	2.36	1
e	0.045	0.055	1.14	1.40	
L ₁	0.750		19.05		

NOTE

1. This dimension allows for off-center lid, meniscus and solder overrun.

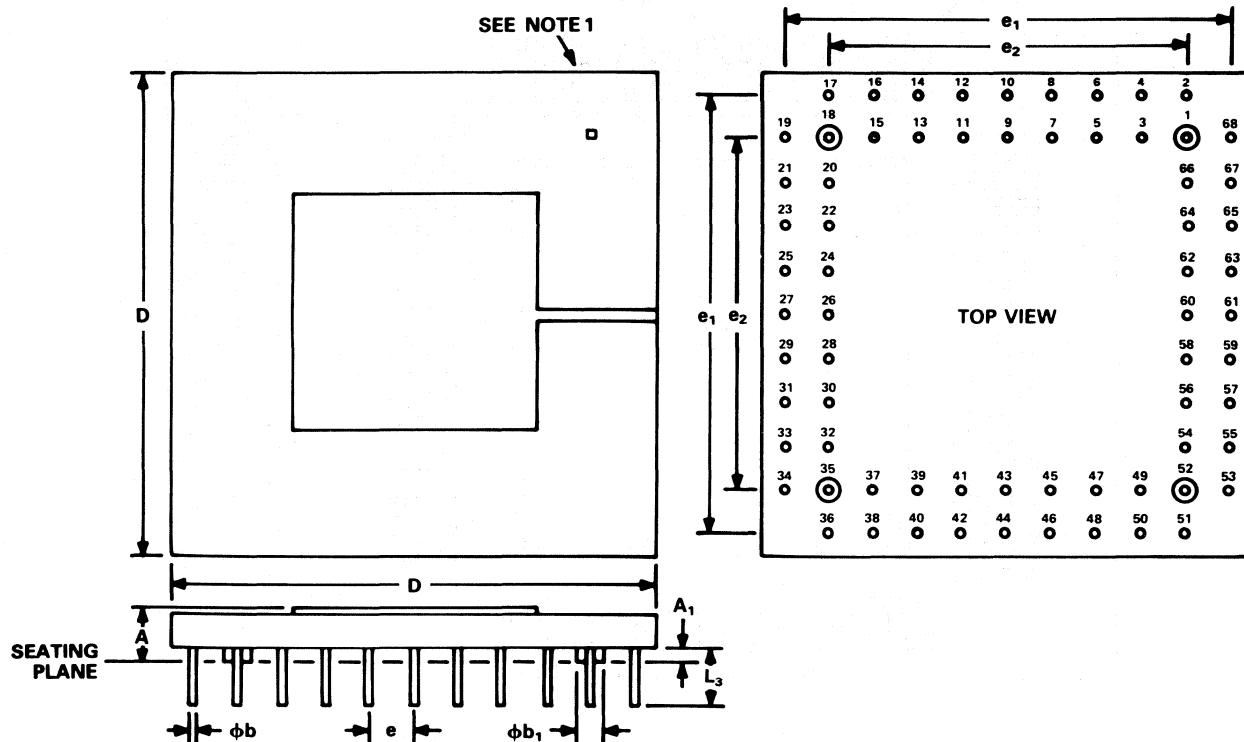
F-100A
100-Lead Ceramic Quad Flat Pack



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.114	0.174	2.91	4.41
A ₁	0.020	0.040	0.51	1.02
b	0.008	0.013	0.20	0.33
c	0.004	0.006	0.10	0.15
E	0.875	0.885	22.23	22.48
E ₁	0.660	0.700	16.76	17.78
e	0.023	0.027	0.58	0.69
L	0.020	0.030	0.51	0.76
Q	0.055	0.075	1.40	1.91
D		0.008		0.20

REV. A

G-68A
68-Pin Grid Array

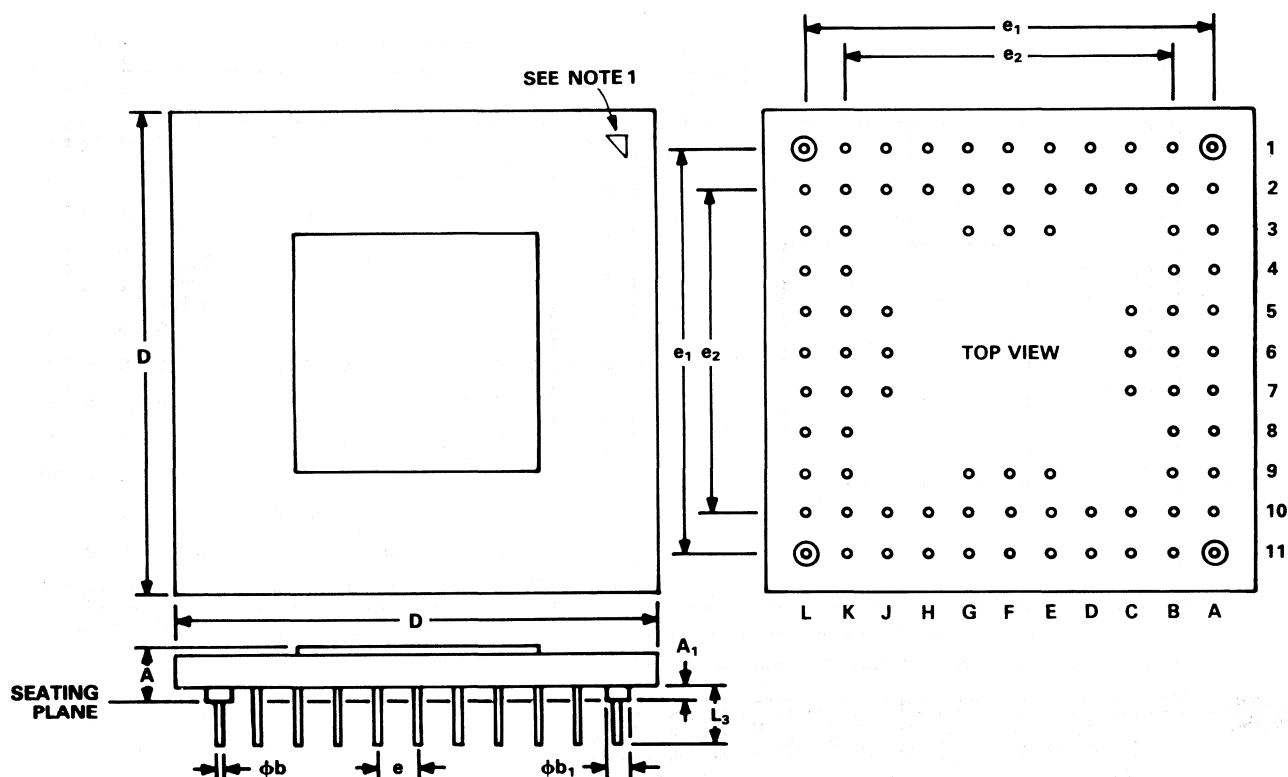


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.123	0.164	3.12	4.17	3
A ₁	0.035	0.055	0.89	1.40	3
φb	0.016	0.021	0.41	0.53	
φb ₁	0.045	0.060	1.14	1.52	2
D	1.080	1.110	27.43	28.19	6
e ₁	0.988	1.012	25.10	25.70	5
e ₂	0.788	0.812	20.02	20.62	5
e	0.095	0.105	2.41	2.67	4
L ₃	0.145	0.190	3.68	4.83	

NOTES

1. Index area; a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension φb₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Lead center when α is 0°; e₁ shall be measured at the centerline of the leads.
6. All four sides.

G-84A
84-Pin Grid Array



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.118	0.169	3.00	4.29	3
A ₁	0.025	0.055	0.64	1.40	3
φb	0.018	0.022	0.46	0.56	
φb ₁	0.045	0.065	1.14	1.65	2
D	1.080	1.120	27.43	28.45	6
e ₁	0.988	1.012	25.10	25.70	5
e ₂	0.788	0.812	20.02	20.62	5
e	0.095	0.105	2.41	2.67	4
L ₃	0.175	0.185	4.45	4.70	

NOTES

1. Index area; a lead one identification mark is located adjacent to location lead L1.
2. The minimum limit for dimension φb₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Lead center when α is 0°; e₁ shall be measured at the centerline of the leads.
6. All four sides.

100-Pin Grid Array



NOTES

1. Index area; a lead one identification mark is located adjacent to lead one.

2. The minimum limit for dimension ϕb_1 may be 0.023" (0.58 mm) for all four corner leads only.

- 3. Dimension shall be measured from the seating plane to the base plane.**

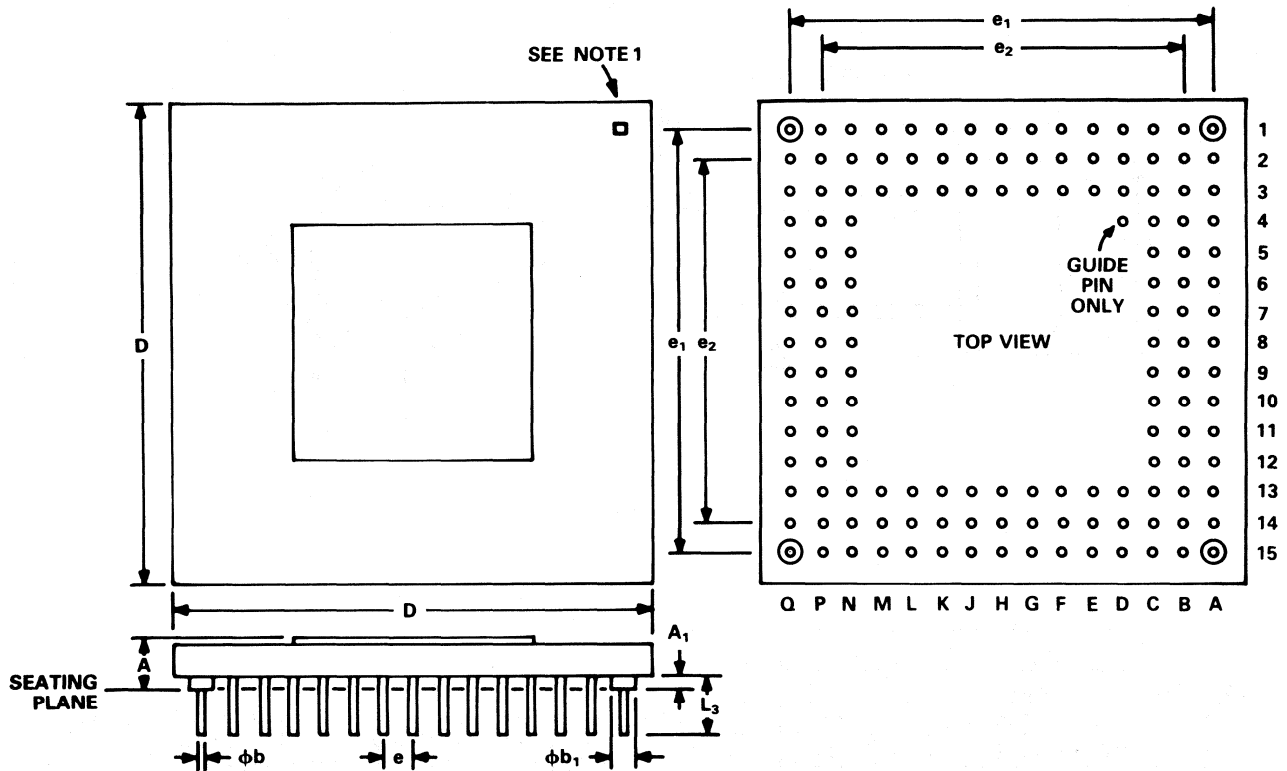
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.

5. Lead center when α is 0° ; e_1 shall be measured at the centerline of the leads.

- 6. All four sides.**

7. Gold plating a maximum of 50 $\mu\text{in.}$ over 100 $\mu\text{in.}$ ref. Thickness of nickel.

G-144A
144-Pin Grid Array



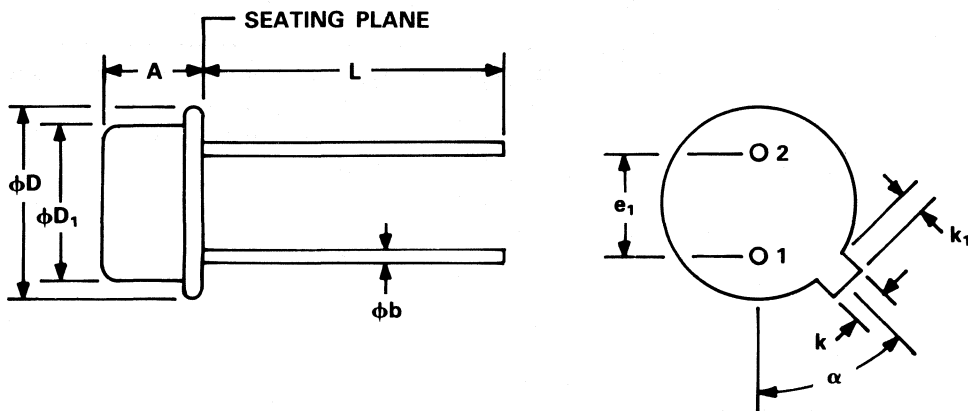
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.132	0.165	3.35	4.19	3
A ₁	0.045	0.055	1.14	1.40	3
ϕb	0.016	0.020	0.41	0.51	
ϕb_1	0.045	0.055	1.14	1.40	2
D	1.559	1.591	39.60	40.41	6
e_1	1.388	1.412	35.26	35.86	5
e_2	1.188	1.212	30.18	30.78	5
e	0.095	0.105	2.41	2.67	4
L ₃	0.175	0.185	4.45	4.70	

NOTES

1. Index area; a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension ϕb_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Lead center when α is 0°; e_1 shall be measured at the centerline of the leads.
6. All four sides.
7. Gold plating a maximum of 50 μ in. over 100 μ in. ref. Thickness of nickel.

H-02A

2-Lead Metal Can



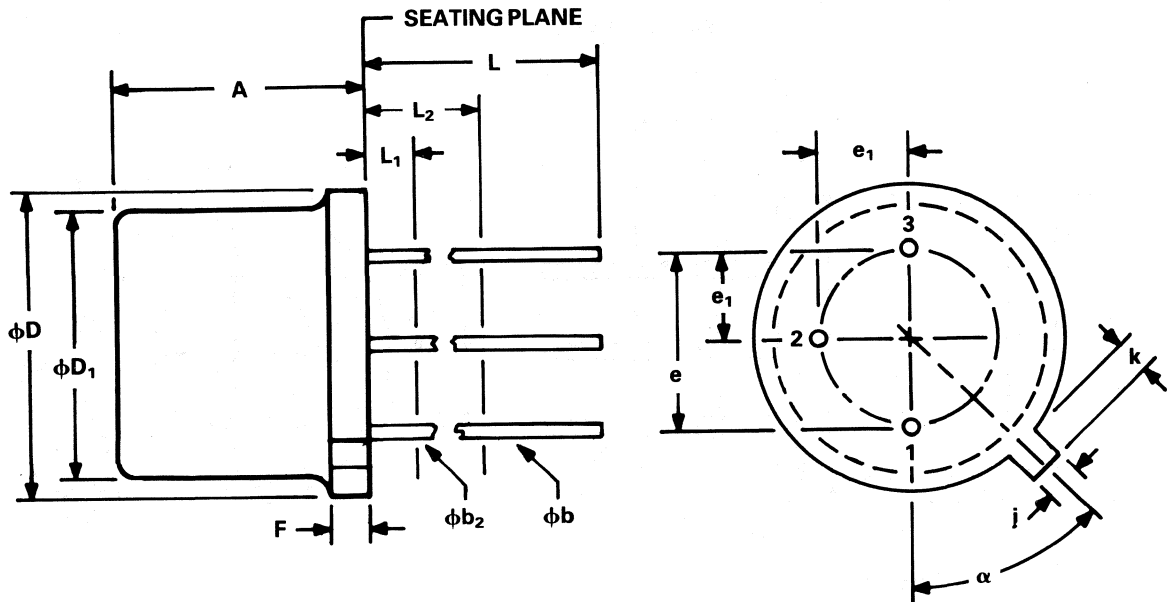
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.125	0.150	3.17	3.81	
ϕb	0.015	0.019	0.38	0.48	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e_1	0.100 BCS		2.54 BSC		1
k	0.036	0.045	0.91	1.17	
k_1	0.028	0.048	0.71	1.22	
L	0.500	0.750	12.70	19.05	
α	45° BSC		45° BSC		1

NOTES

1. Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.54" (1.37 mm) + 0.001" (0.03 mm) – 0.000" (0.00 mm) below the seating plane of the device are within 0.007" (0.18 mm) of their true positions relative to a maximum-width tab.
2. All leads – increase maximum limit 0.003" (0.08 mm) when hot solder dip finish is applied.

H-03A

3-Pin Can



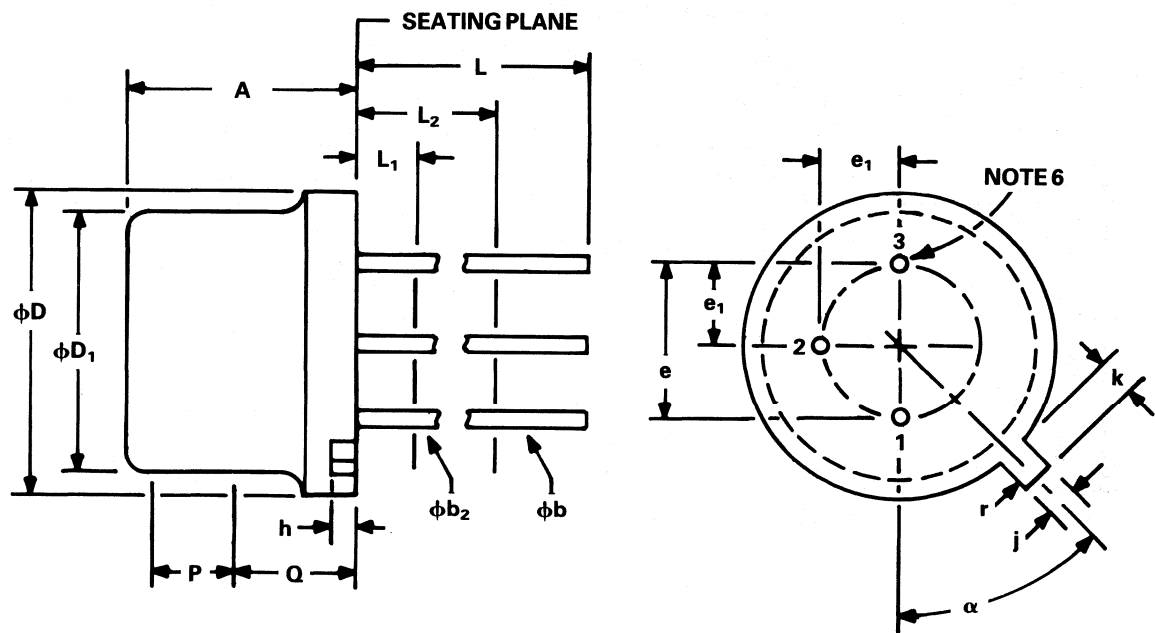
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.115	0.150	2.92	3.81	
ϕb		0.021		0.53	1, 4
ϕb_2	0.016	0.019	0.41	0.48	1, 4
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		2
e_1	0.050 T.P.		1.27 T.P.		2
F		0.030		0.76	
j	0.036	0.046	0.91	1.17	
k	0.028	0.048	0.71	1.22	3
L	0.500		12.70		1
L_1		0.050		1.27	1
L_2	0.250		6.35		
α	45° T.P.				

NOTES

1. (Three leads) ϕb_2 applies between L_1 and L_2 . ϕb applies between L_2 and 0.5" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70 mm) from seating plane.
2. Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.054" (1.4 mm) + 0.001" (0.03 mm) - 0.000" (0.000 mm) below the seating plane of the device are within 0.007" (0.18 mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads - increase maximum limit 0.003" (0.08 mm) when hot solder dip finish is applied.

H-03B

3-Pin Can



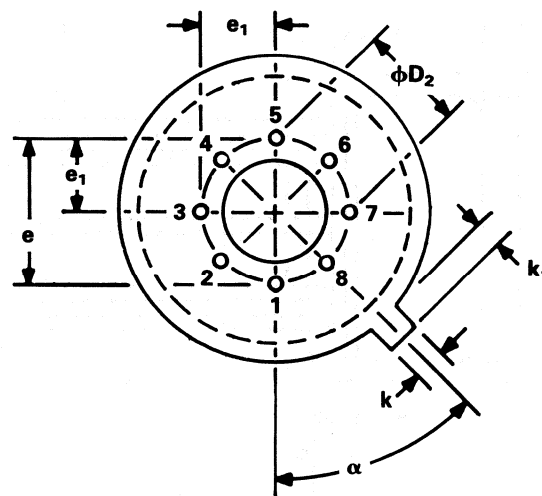
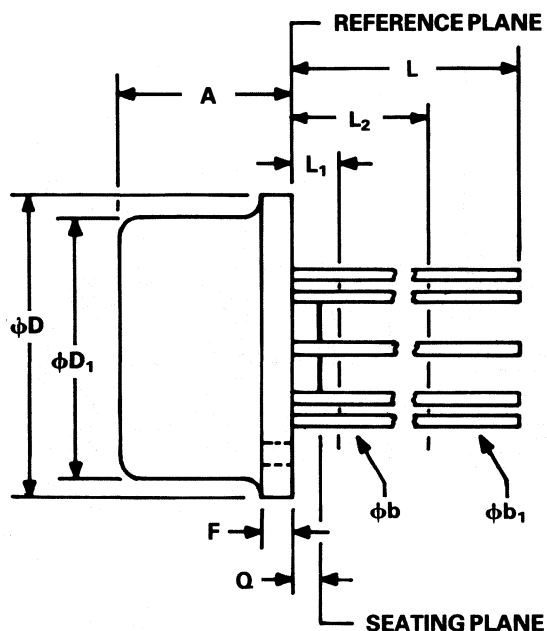
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.021	0.41	0.53	2, 7
ϕb_2	0.016	0.019	0.41	0.48	2, 7
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
e	0.200 T.P.		5.08 T.P.		4
e ₁	0.100 T.P.		2.54 T.P.		
h	0.015	0.035	0.38	0.89	
j	0.028	0.034	0.71	0.86	
k	0.029	0.045	0.74	1.14	3
L	0.500		12.70		2
L ₁		0.050		1.27	2
L ₂	0.250		6.35		2
P	0.100		2.54		1
Q					5
r		0.007		0.18	
α	45° T.P.				

NOTES

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010" (0.25 mm)
2. (Three leads) ϕb_2 applies between L₁ and L₂. ϕb applies between L₂ and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L₁ and beyond 0.500" (12.70 mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.054" (1.37 mm) + 0.001" (0.03 mm) - 0.000" (0.000 mm) below the seating plane of the device are within 0.007" (0.18 mm) of their true positions relative to the maximum-width tab.
5. Details of outline in this zone optional.
6. Lead #3 connected to case.
7. All leads - increase maximum limit 0.003" (0.08 mm) when hot solder dip finish is applied.

H-08A

8-Pin Can



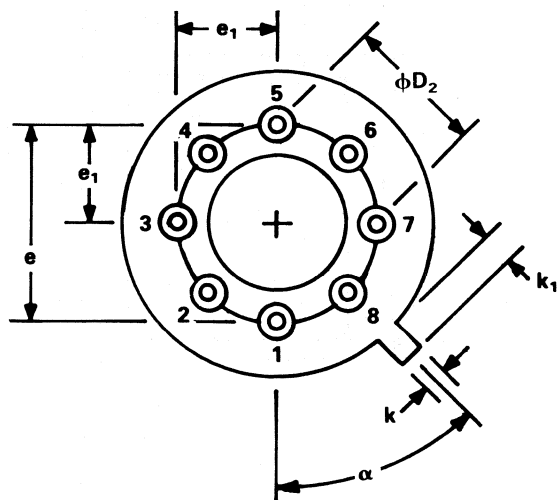
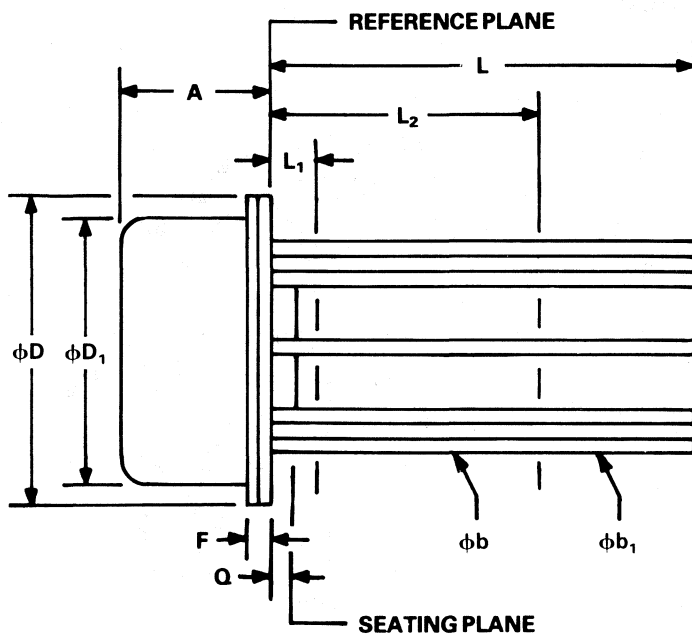
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb ₁	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD ₁	0.305	0.335	7.75	8.51	
ϕD ₂	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e ₁	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k ₁	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L ₁		0.050		1.27	
L ₂	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L₁ and L₂. ϕb₁ applies between L₂ and 0.500" (12.70 mm) from the reference plane. Diameter is uncontrolled in L₁ and beyond 0.500" (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.054" (1.37 mm) + 0.001" (0.03 mm) - 0.000" (0.000 mm) below the base plane of the product is within 0.007" (0.18 mm) of their true position relative to the maximum width tab.
4. All leads - increase maximum limit 0.003" (0.08 mm) when hot solder dip finish is applied.

H-08B

8-Pin Can



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb ₁	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD ₁	0.305	0.335	7.75	8.51	
ϕD ₂	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e ₁	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k ₁	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L ₁		0.050		1.27	1
L ₂	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

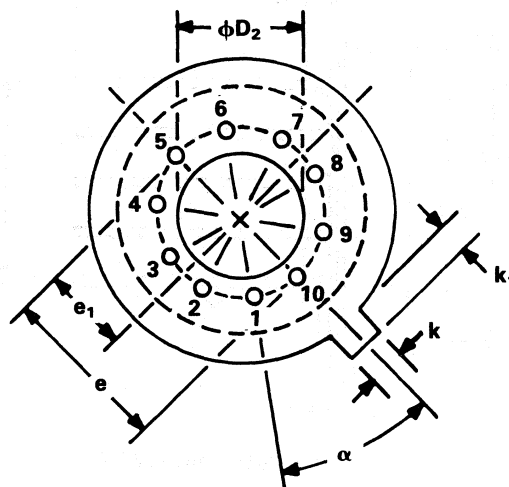
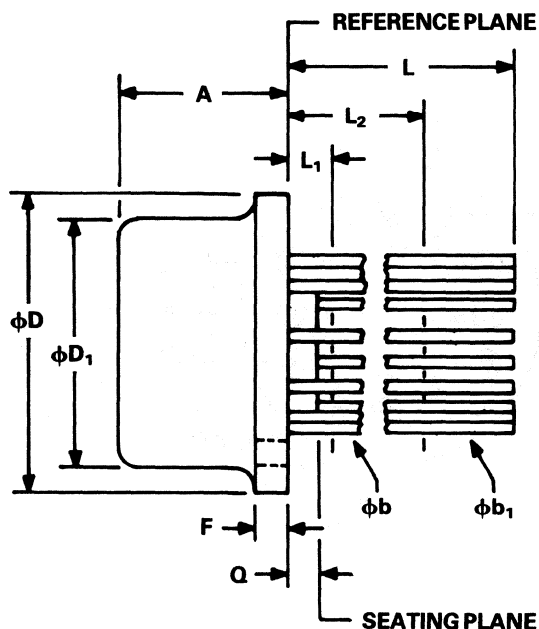
NOTES

- (All leads) ϕb applies between L₁ and L₂. ϕb₁ applies between L₂ and 0.500" (12.70 mm) from the reference plane. Diameter is uncontrolled in L₁ and beyond 0.500" (12.70 mm) from the reference plane.
- Measured from the maximum diameter of the product.
- Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.054" (1.37 mm) + 0.001" (0.03 mm) - 0.000" (0.000 mm) below the base plane of the product is within 0.007" (0.18 mm) of their true position relative to the maximum width tab.
- All leads - increase maximum limit 0.003" (0.08 mm) when hot solder dip finish is applied.

REV. B

H-10A

10-Pin Can



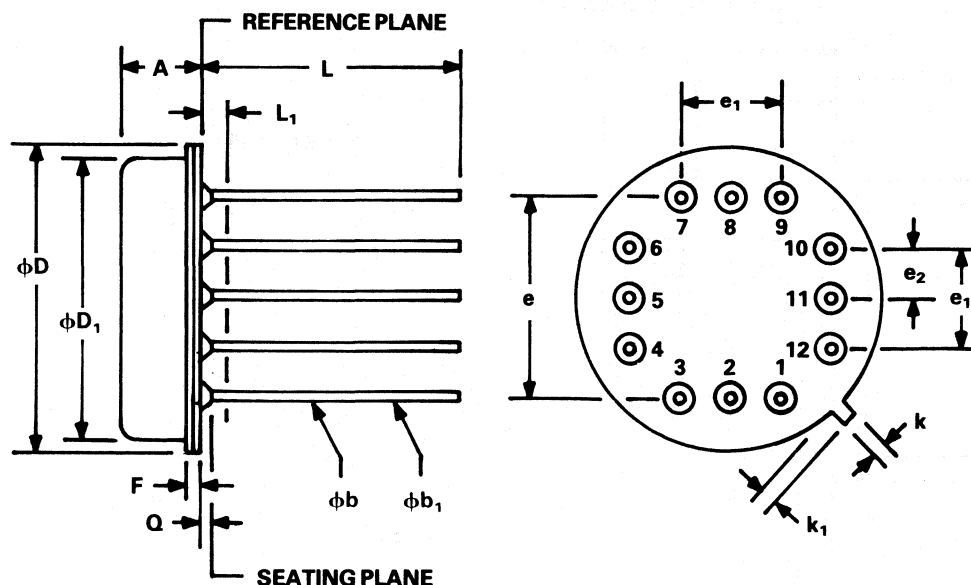
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb ₁	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD ₁	0.305	0.335	7.75	8.51	
ϕD ₂	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e ₁	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k ₁	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L ₁		0.050		1.27	1
L ₂	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	36° BSC		36° BSC		3

NOTES

1. (Three leads) ϕb₂ applies between L₁ and L₂. ϕb applies between L₂ and 0.5" (12.70 mm) from the seating plane. Diameter is uncontrolled in L₁ and beyond 0.5" (12.70 mm) from the seating plane.
2. Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.054" (1.4 mm) + 0.001" (0.03 mm) - 0.000" (0.000 mm) below the seating plane of the device are within 0.007" (0.18 mm) of their true position relative to the maximum-width tab.
3. Measured from the maximum diameter of the actual device.
4. All leads - increase maximum limit 0.003" (0.08 mm) when hot solder dip finish is applied.

H-12A

12-Pin Can

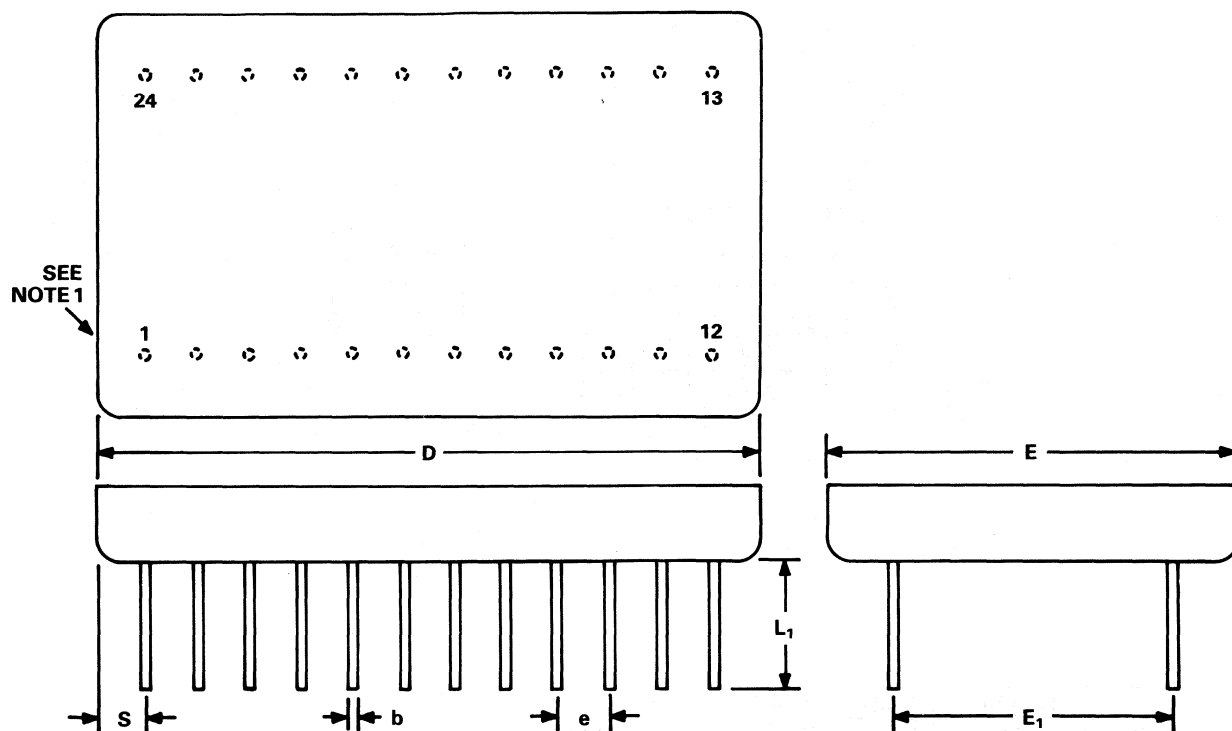


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.148	0.181	3.76	4.60	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.592	0.615	15.04	15.62	
ϕD_1	0.545	0.555	13.84	14.10	
e	0.400 BSC		10.16 BSC		3
e_1	0.200 BSC		5.00 BSC		3
e_2	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.026	0.036	0.66	0.91	
k_1	0.027	0.037	0.68	0.94	2
L	0.375		9.50		
L_1		0.050		1.27	1
Q	0.010	0.045	0.25	1.14	

NOTES

- (All leads) ϕb applies between L and L_1 . ϕb_1 applies between L_1 and 0.375" (9.50 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.375" (9.50 mm) from the reference plane.
- Measured from the maximum diameter of the product.
- Leads having a maximum diameter 0.019" (0.48 mm) measured in gauging plane 0.054" (1.37 mm) + 0.001" (0.03 mm) – 0.000" (0.000 mm) below the base plane of the product are within 0.007" (0.18 mm) of their true position relative to the maximum width tab.

M-24A
24-Pin Metal Platform

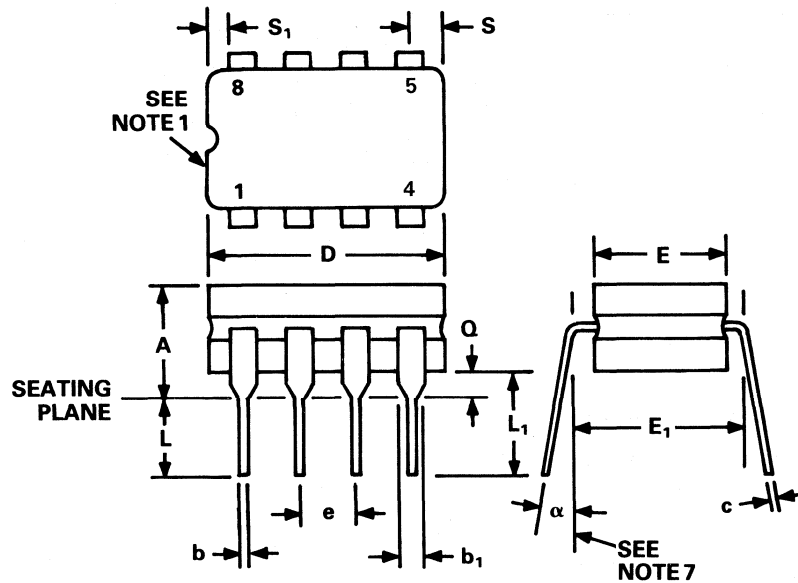


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
b	0.014	0.023	0.36	0.58	
D	1.265	1.280	32.131	32.51	
E	0.765	0.780	19.431	19.80	
E ₁	0.590	0.620	12.95	15.75	3
e	0.090	0.110	2.29	2.79	4
L ₁	0.230	0.270	5.84	6.85	
S		0.090		2.29	2

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E₁ shall be measured at the centerline of the leads.
4. Twenty-two spaces.

Q-8
8-Lead Cerdip

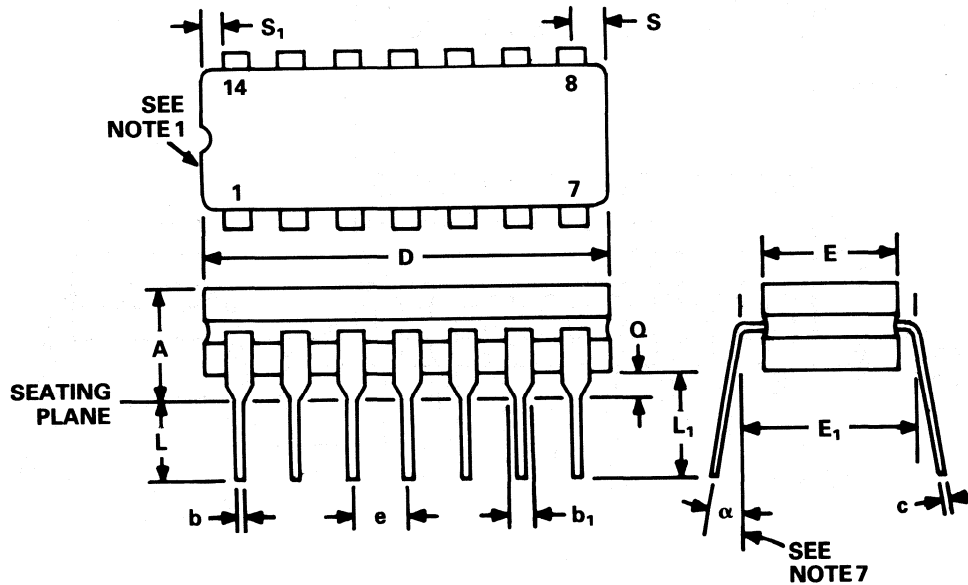


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

Q-14
14-Lead Cerdip

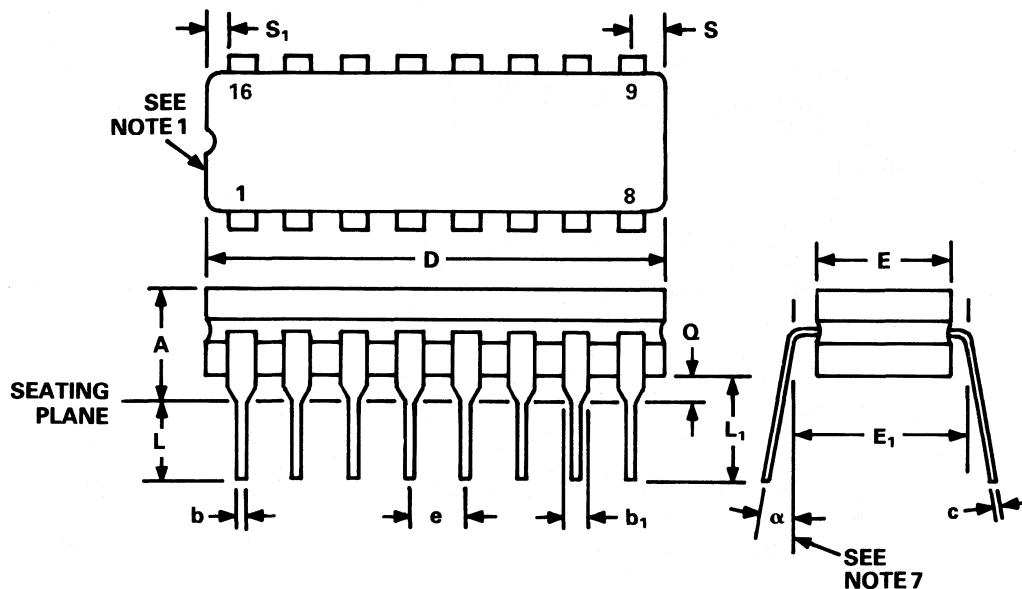


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twelve spaces.

Q-16
16-Lead Cerdip

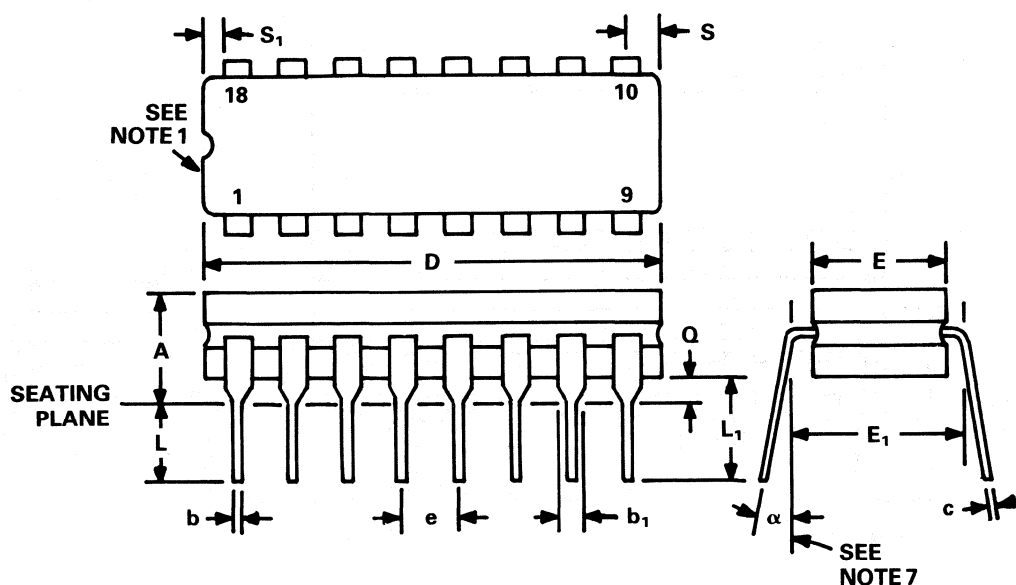


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

Q-18
18-Lead Cerdip

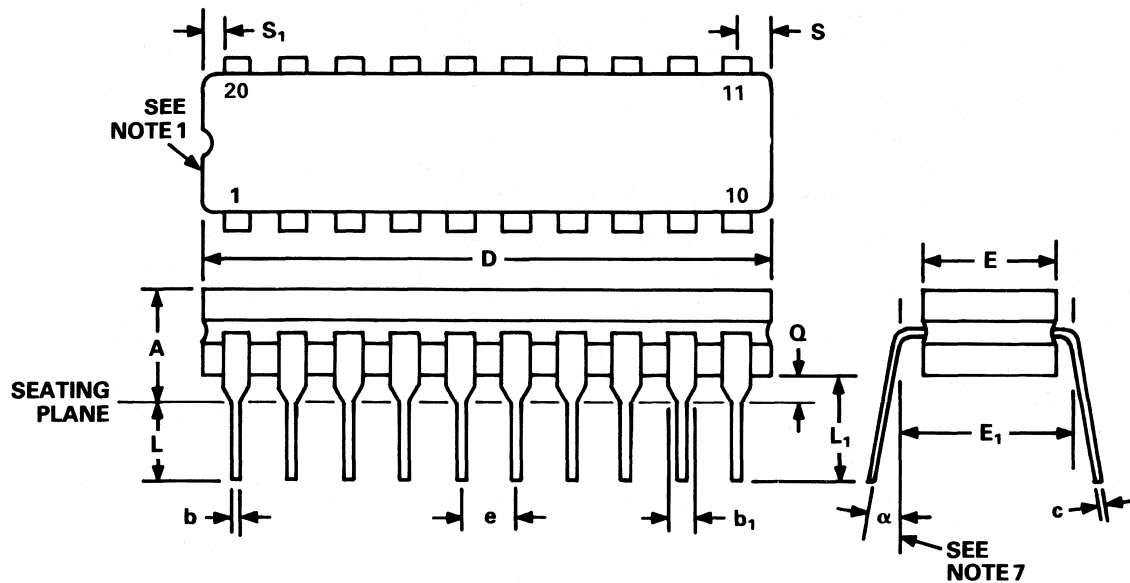


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

Q-20
20-Lead Cerdip

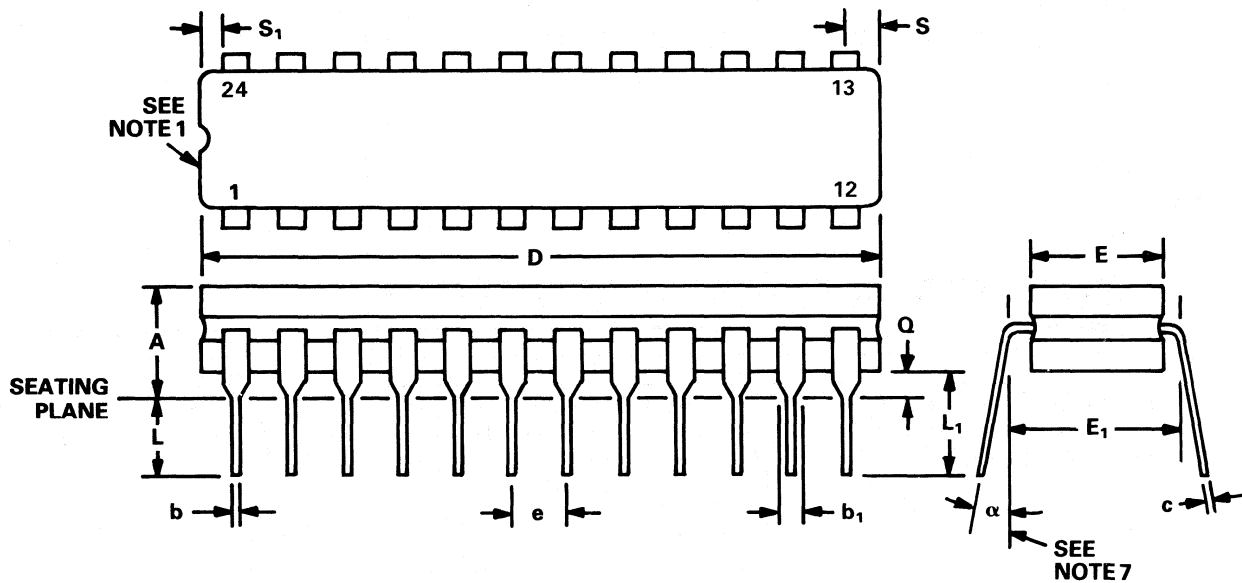


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b ₁	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L ₁	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S ₁	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b₁ may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Eighteen spaces.

Q-24
24-Lead Cerdip

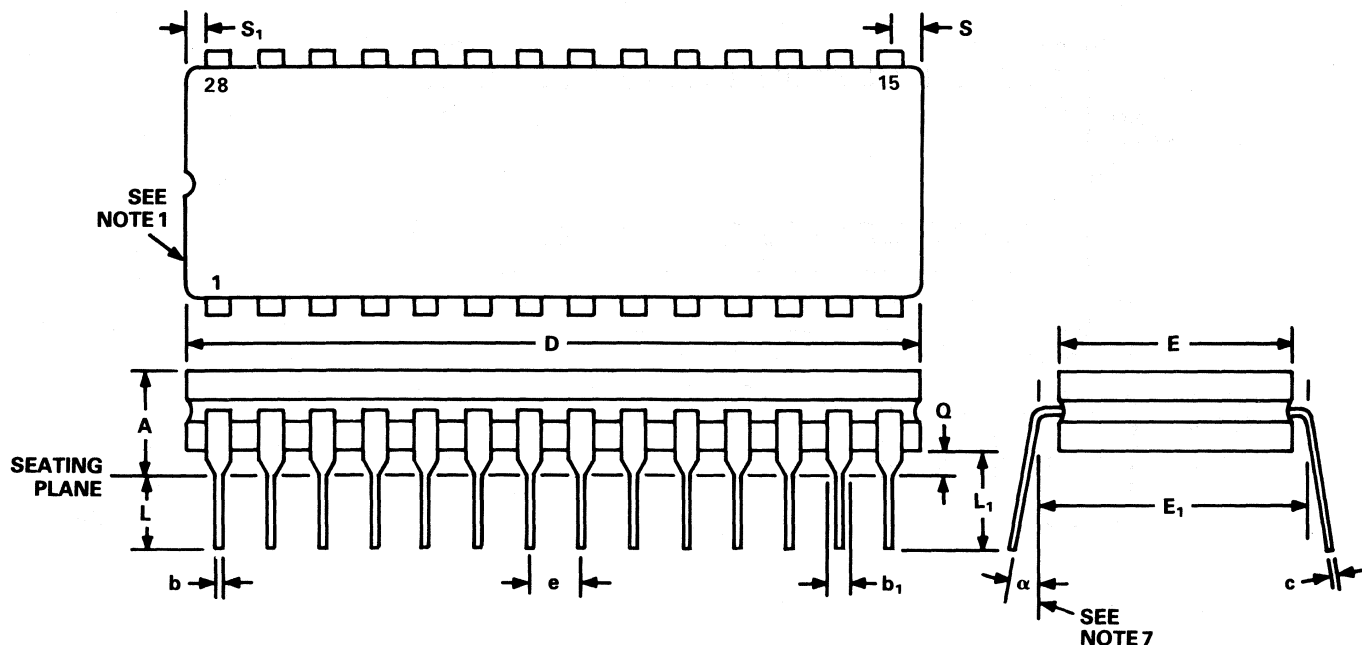


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-two spaces.

Q-28
28-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-six spaces.

Appendix 2

Glossary

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1. 10/10/10
2. 10/10/10

General Specifications

SPECIFICATION	SYMBOL	DEFINITION
Accuracy, Relative	RA	Relative accuracy error, expressed in %, ppm, or fractions of 1LSB, is the deviation of the analog value at any input (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. This definition applies to ADCs, DACs and Analog Multipliers.
Acquisition Time	t_{AQ}	Acquisition time in a sample-track/hold is the time required by the output of the device to reach its final value, within a specified error band, after the sample-track command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.
Aperture (Delay) Time	t_{AD}	This is the time required after the <i>hold</i> command for the switch to open fully. The sample is, in effect, delayed by this interval, and the <i>hold</i> command would have to be advanced by this amount for precise timing.
Aperture Uncertainty – or Aperture (Delay) Jitter	t_{AU}	This is the range of variation in the <i>aperture time</i> . If the <i>aperture time</i> is “tuned out” by advancing the <i>hold</i> command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency for a given resolution.
Bipolar Offset	B_{POE}	For almost all bipolar coded converters, (e.g., ± 10 volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter. This makes the zero point of the converter independent of thermal drift of the reference, because the 1/2 scale offset cancels the weight of the MSB at zero, independent of the amplitude of both.
Charge Transfer (or <i>hold</i> step)	QT	The principal component of <i>sample-to-hold</i> offset (or pedestal) is the charge transferred to the storage capacitor via stray capacitance when switching to the <i>hold</i> mode. It can sometimes be reduced by lightly coupling the appropriate-polarity version of the <i>hold</i> signal to the capacitor for cancellation. The associated voltage error (Q/C) can be reduced by using greater capacitance for storage; but this increases response time.
Closed Loop Bandwidth	BW	The frequency at which the magnitude of the small signal voltage gain of the amplifier, operated closed loop as a unity gain follower is 3dB below unity.
Common-Mode Impedance	Z_{CM}	The impedance between each input and power supply common.

SPECIFICATION	SYMBOL	DEFINITION
Common-Mode Rejection Ratio	CMRR	Common-mode rejection ratio is the ratio of common-mode voltage input to the resulting common-mode error output voltage referred to the input (i.e., divided by the closed loop gain). Expressing it logarithmically, it then becomes the common-mode rejection (CMR (in dB) = $20 \text{ Log}_{10} (\text{CMRR})$).
Common-Mode Voltage Range	CMVR	Common-mode voltage range is defined as $(V_{\text{IN}+}) + (V_{\text{IN}-})/2$. The maximum range of common-mode voltage is that voltage which will allow normal operation of the amplifier.
Compliance-Voltage Range	CVR	For a current-output device, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.
Conversion Time and Conversion Rate	t_{CONV}	The time required for a complete measurement by an ADC is called <i>conversion time</i> . For most converters (assuming no significant additional systemic delays), this is identical to the inverse of <i>conversion rate</i> . However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined, resulting in a higher conversion rate.
Differential Input Impedance	Z_{IND}	The impedance between the two input terminals, usually includes resistance and capacitance.
Differential Input Resistance	R_{IND}	Resistive component of Differential Input Impedance.
Differential Voltage	V_{DIFF}	Differential voltage is defined as $V_{\text{IN}+} - V_{\text{IN}-}$. The maximum differential voltage is the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.
Droop	V_{DRP} or I_{DRP}	Droop is the change of the output voltage of an S/H during <i>hold</i> as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a (<i>droop</i> or <i>drift</i>) current. (Note: $I_{\text{DRP}} = C_{\text{H}} \frac{dV}{dt}$ where C_{H} is the <i>hold</i> capacitance.)
Feedthrough	FTE	Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., <i>feedthrough error</i> in a multiplying DAC. It is variously specified in %, ppm, fractions of 1LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.
Full Power Bandwidth	FBW	The maximum frequency at which an amplifier can produce the specified peak-to-peak output voltage into its rated load at a specified distortion level.

SPECIFICATION	SYMBOL	DEFINITION
Gain Bandwidth Product	GBW	The product of the gain and small signal bandwidth for an operational amplifier, or the product of open loop gain available at a specified frequency times that frequency.
Gain Open Loop	A_{VS}	The ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change.
High Level Output Voltage	V_{OH}	The voltage at a digital output with input conditions applied that will establish a high level at the output.
High Level Input Voltage	V_{IH}	The most positive (least negative) value of high level input voltage for the proper operation of the logic element.
High Level Three-State Leakage Current	I_{OZH}	The current flowing into an output with input conditions that will establish the high impedance state at the output and with the high voltage applied to the output.
Input Bias Current	I_{IB}	Bias current is defined as the current required at either input from an infinite impedance source to drive the output to zero. All Analog Devices' specifications pertain to the larger of the two, (for differential amps) not the average. FET input bias current is specified at the warmed-up value.
Input Bias Current Drift	dI_{IB}/dT	The ratio of the change in bias current to the change in temperature.
Input Noise Current	I_{NPP}	Low frequency input noise current is the peak-to-peak variation within a specified frequency band.
Input Noise Current Density	I_N	Wideband noise is specified as either rms noise in a given bandwidth or spectral density in a 1Hz band surrounding a specified frequency ($pA/\sqrt{Hz}$).
Input Noise Voltage	E_{NPP}	Low frequency input noise voltage is the peak-to-peak variation within a specified frequency band.
Input Noise Voltage Density	E_N	Wideband noise is specified as either rms noise in a given bandwidth or spectral <i>density</i> in a 1Hz band surrounding a specified frequency ($nV/\sqrt{Hz}$).
Input Offset Current	I_{IO}	Offset current is the difference between the bias currents at the two inputs, with the output at zero volts.
Input Offset Current Drift	TCI_{OS}	The ratio of the maximum change in offset current over a given temperature range to the change in temperature.
Input Offset Voltage	V_{IO}	Offset voltage is the voltage require at the input from zero source impedance to drive the output to zero.
Input Offset Voltage Drift	dV_{OS}/dT	The ratio of the maximum change in offset voltage over a given temperature range to the change in temperature. Generally offset drift is higher when initial offset is higher.
Input Offset Voltage Match	$DIFFV_{OS}$	The difference between the offset voltages of one side of a dual op amp to the other ($V_{OS1} - V_{OS2}$).

SPECIFICATION	SYMBOL	DEFINITION
Least Significant Bit	LSB	In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 the right-most digit is the LSB. Its analog weight, relative to full scale is 2^{-n} , where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n -bit converter. In converter nomenclature (e.g., fractional binary), it is Bit n ; in bus nomenclature (integer binary), it is Data Bit 0.
Line Regulation	V_{RLINE}	The change in output voltage due to a specified change in input voltage. It is usually expressed in percent per volt or microvolts per volt of input change
Linearity	RA	Linearity error of a converter (also), <i>integral nonlinearity</i> , see Linearity, Differential), expressed in percent or ppm of full-scale range, or (sub) multiples of 1LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is the same as relative-accuracy error.
Linearity, Differential	DNL	Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2^{-n} of full scale for an n -bit converter). Any deviation of the measured "step" from the ideal difference is called <i>differential nonlinearity</i> , expressed in (sub) multiples of 1LSB. It is an important specification, because a differential linearity error greater than 1LSB can lead to nonmonotonic response in a D/A converter and missed codes in an A/D converter.
Load Regulation	V_{RLOAD}	The change in output voltage for a specified change in load current at low frequency. It is generally expressed in microvolts per milliampere, or ohms of dc output resistance. This specification includes the effect of self-heating due to increased power dissipation at higher load current.
Low Level Input Voltage	V_{IL}	The most positive (least negative) value of <i>low level</i> digital input voltage for the proper operation of the logic element.
Low Level Output Voltage	V_{OL}	The voltage at a digital output with input conditions applied that will establish a low-level at the output.

SPECIFICATION	SYMBOL	DEFINITION
Low Level Three-State Leakage Current	I_{EzL}	The current flowing into an output with input conditions that will establish the low impedance state at the output and with the low level voltage applied to the output.
Monotonic		A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The condition "monotonic" requires that the derivative of the transfer function never changes signs.
Most Significant Bit	MSB	In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the left most "1" is the MSB, with a weight of 2^{n-1} , or 8LSBs. Its analog weight, relative to a DAC's full-scale span, is 1/2. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits. In converter nomenclature (fractional binary), it is Bit 1; in bus nomenclature (integer binary), it is Data Bit (n-1).
Multiplexer/Switch Terminology	C_{OUT}	Capacitance between the output terminal and ground with all switches open.
	$CS - C_{OUT}$	Capacitance between any open "S" and the output terminal.
	$CS(CD)$	Capacitance between input (output) and ground. (This capacitance is specified for the switch open and closed.)
	C_{DS}	Capacitance between input and output. (This will determine the switch isolation over frequency.)
	$C_{DS}(C_{SS})$	Capacitance between inputs (outputs) of any 2 switches. (This will determine the cross coupling between switches vs. frequency.)
	$I_D(I_S) OFF$	Current at any switch input (output). This is a leakage current when the switch is open.
	I_{OUT}	Current at the output. This is a leakage current when all switches are open.
	R_{ON}	Ohmic resistance between the input and output off and "on" channel.
	R_{ON} vs. Temperature	R_{ON} drift over the temperature range.
	R_{ON} vs. Between Switches	Difference between the R_{ON} 's of any two switches.
	R_{ON} vs. Temperature Between Switches	Differences between the R_{ON} drifts of any two switches.

SPECIFICATION	SYMBOL	DEFINITION
	$t_{\text{TRANSITION}}$	Delay time when switching from one address state to another.
	t_{OPEN}	“OFF” time of both switches when switching from one address state to another.
	$t_{\text{ON(EN)}}$	Delay time between the 50% points of the enable input and switch “ON” condition.
	$t_{\text{OFF(EN)}}$	Delay time between the 50% points of the enable input and the switch “OFF” condition.
	V_{INL}	Digital threshold voltage for the low state.
	V_{INH}	Digital threshold voltage for the high state.
Output Sink Current	I_{SINK}	The maximum current (negative at positive voltage, positive at negative voltage) that flow into the output terminal of the device.
Output Source Current	I_{SOURCE}	The maximum positive current at positive voltage, or negative current at negative voltage that can be delivered by the device.
Output Voltage Noise (En p-p)	OE_N	The peak-to-peak output noise voltage in a specified frequency band.
Output Voltage Swing	V_{OUT}	The maximum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs.
Power Dissipation	P_D	The total power dissipated in a device with no load. Also, maximum allowable power in a device.
Power-Supply-Rejection Ratio – Linear Devices	PSRR	The ratio of a change in power supply voltage to the resulting change in input offset voltage.
Power-Supply-Rejection Ratio – Converters	PSRR	The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1LSB) for a 1% dc change in the power supply (e.g., 0.05%/ % VS).
Quiescent Current or Supply Current	$I_Q, I_{CC}, I_{DD}, I_{SS}, I_{EE}$	The current required from the supply to operate the device with no load.
Rated Output Current	I_{OUT}	The minimum guaranteed value of current supplied at the rated output voltage
Resolution	RES	An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a <i>resolution</i> of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7118 LOGDAC has a logarithmic gain resolution of $1.5/88.5\text{dB} = 1:59\text{dB}$, which corresponds to a gain increment of 18.9%/step, or 26,600:1.

SPECIFICATION	SYMBOL	DEFINITION
Sample-to-Hold Offset	SH _{OS}	A shift in level between the last value in <i>sample</i> and the value settled-to in <i>hold</i> , is the residual step error after the <i>charge transfer</i> is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as <i>offset nonlinearity</i> .
Settling Time – Amplifier	t _{SL}	Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a “long tail” due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and the specified compensation. A full-scale unipolar step input is used, and both polarities are tested. Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be predicted from the other dynamic specifications.
Settling Time – DAC	t _{SL}	The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually $\pm 1/2\text{LSB}$) of the final value. Typical prescribed changes are full-scale, 1MSB, and 1LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op amp circuit.
Slew Rate	t _{SR}	The ratio of a change in output current or voltage to the minimum time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative going changes. Slew rate may be specified either irrespective of distortion or with sine wave distortion limited to a fixed percentage, usually 3%.

SPECIFICATION	SYMBOL	DEFINITION
Thermal Characteristics	θ_{JA}	Thermal resistance of an IC package, junction to ambient.
	θ_{JC}	Thermal resistance of an IC package, junction to case.
	T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
X or Y Feedthrough	FT_X or FT_Y	The signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an input offset at the zero input (which can be trimmed out), and a nonlinear one, which is irreducible.

Absolute Maximum Ratings

A listing of the voltages, currents, power and temperatures which, if exceeded, may cause parametric, functional, or catastrophic failure of a device. The simultaneous use of multiple maximum ratings must be avoided.

Attributes Data

A listing of gross quantities accepted and rejected at a screening or Quality Conformance Test.

Analog Device

An IC with an output that has a mathematical function in relation to the input.

Burn-In

A test performed at a specified temperature with the device subjected to bias voltages. Duration and other conditions are stipulated in Test Method 1015 of MIL-STD-883. The most common time and temperature conditions are 160 hours at 125°C.

Case Outline

The physical dimensions of a device as detailed in Appendix 1.

Class B

Refers to a class of devices that are subjected to a series of predetermined tests and conditions in accordance with Test Method 5004, Test Method 5005, Test Method 5008 (for hybrids) and paragraph 1.2.1 of MIL-STD-883. Class B devices are the most commonly used devices in military systems for ground support and airborne equipment.

Date Code

A four digit code identifying a six-week period of sealing or optionally the seal week of an inspection lot. The first two digits of the date code represent the year and the second two digits the week. An example of this is a date code of 9001 which covers the week of December 31, 1988 through January 6, 1990.

Note: The first week of the year is that calendar week in which the first Thursday falls.

Certificate of Conformance

A document signed by a quality representative or a designated alternative attesting to the conformity of the material to all purchase order and specification requirements.

Change Notification

Also referred to as major change notification and configuration change. The process whereby a procuring activity is notified of a change in a previously supplied product. This change may affect the electrical properties, mechanical properties or processing of a device. Analog Devices change notification is in accordance with the Class 1 requirements of MIL-STD-480.

Device Type

Device type as referenced in this catalog refers to a specific grade and package. A generic device type will contain variations in electrical performance and package options.

Device Class

The devices described in this catalog are product assurance level class B devices IAW MIL-STD-883 and applicable paragraphs of MIL-M-38510.

DIP

Term used in the package outline section is an abbreviation for dual-in-line package.

Electrostatic Discharge Damage (ESD)

A term used to describe the level at which a device is susceptible to damage or degradation due to exposure of an electrostatic discharge.

Generic Data

Data derived from devices that are in the same family grouping as the supplied devices. Family groupings are defined in Appendix E of MIL-M-38510.

Group A

The testing of a sample to verify the lot conformance to the electrical test requirements. The electrical tests are performed at the ambient and specified temperature limits for specified subgroupings.

Group B

A set of sampling tests performed to check brand permanence, solderability and bond strength of devices. The test requirements and MIL-STD-883 test methods invoked are detailed in Table II B, Test Method 5005 of MIL-STD-883. Group B requirements for hybrids are specified in Test Method 5008 of MIL-STD-883.

Group C

A 1000 hour steady state life test performed on devices once per year on a generic basis. The test is performed to demonstrate the quality or reliability of devices subjected to specified conditions over an extended period of time. Test conditions and methodology are detailed in test methods 1005 of MIL-STD-883. The test is performed per Table III, Method 5005 of MIL-STD-883.

Group D

A series of tests, humorously called "shake, rattle and roll," used to verify the ability of devices to pass a set of mechanical and temperature stress testing. The testing is usually destructive in nature and performed on a yearly basis. The test methodology and sequence of testing is detailed in Table IV of Method 5005/MIL-STD-883.

JAN

A term originally used to signify "Joint Army Navy." A trademark of the U.S. government used to indicate that a device is in accordance with a controlled specification and manufactured in an approved DESC-EQM facility.

IAW

Term used as an abbreviation for "in accordance with."

MIL-M-38510

A specification that establishes the general requirements for monolithic, multichip and hybrid microcircuits and the quality and reliability assurance requirements that are required in their acquisition. Compliant 883 devices are required to meet the MIL-M-38510 paragraphs that are specified in paragraph 1.2.1 of MIL-STD-883. JAN devices are required to meet all sections of MIL-M-38510 for the device class and device type under consideration.

MIL-STD-883

The specification used to describe the procedures and accept/reject criteria for the environmental/physical and electrical testing of microcircuits.

Steady State Life

A 1000 hour sample test performed under the same temperature and electrical conditions as burn-in. The test procedure used is IAW Method 1005 of MIL-STD-883.

Percent Defective Allowable (PDA)

The maximum percent defective that is allowed for a 100% screening test. The 160 hour burn-in test for 883 compliant devices has a 5% PDA, which means a lot containing greater than 5% rejects for 25°C electrical testing post-burn-in is considered to have failed. A re-burn-in is allowed on a failed lot with some restrictions (i.e., lot has less than 20% total failures and the PDA for the re-burn-in is 3%).

Internal Visual

Also referred to as Pre-Cap, Pre-Seal or 3rd Optical, this is a visual determination of the acceptability of a device performed prior to sealing and at the die level. The accept/reject criteria are detailed in Method 2010 of MIL-STD-883. For hybrid devices Method 2017 of MIL-STD-883 is applicable.

Qualification Testing

The sample testing of an initial lot to determine the products acceptability and compliance to a series of test methods and procedures defined in Test Method 5005 of MIL-STD-883 (Test Method 5008 for hybrids). A redesign or change in materials used in the manufacture of a device usually requires requalification. The requalification is limited in scope and entails only the testing required to determine the acceptability of the change. This term is sometimes erroneously used in lieu of Quality Conformance Inspection.

Quality Conformance Inspection (QCI)

The periodic sample testing performed to ensure the continued quality and reliability of devices after qualification. The test methods and procedures used for JAN and 883 compliant devices is detailed in Test Method 5005 of MIL-STD-883 (Test Method 5008 for hybrids).

Screening

Testing performed on a 100% basis to achieve the required levels of quality and reliability. The test sequences and requirements are detailed in Method 5004 of MIL-STD-883 for ICs, Test Method 5008 for hybrids.

SCDs (Source Control Drawings/Specification Control Drawings)

Drawings prepared or specified by the customer for the mechanical, electrical and/or processing of devices to be supplied in conjunction with a purchase order. The term SCD is used regardless if the drawing is used to control the source of supply (Source Control Drawings) or the detail requirements of the device (Specification Control Drawing).

Standard Military Drawings

Previously referred to as DESC (Defense Electronics Supply Center) drawings: Drawings controlled and issued by the government agency, DESC-ECS, located in Dayton, Ohio. The use of standard military drawings is an attempt by the government to reduce the proliferation of SCDs describing the same device type. Devices supplied to an SMD must be 883 compliant IAW paragraph 1.2.1 of MIL-STD-883. Copies of SMDs are available from DESC.

Variables Data

Recorded data on a specific device. The term is usually used to describe the reading and recording of electrical parameters at pre-burn-in, post-burn-in and/or Group A for a serialized device. Sometimes confused with attributes data which does not have traceable data to an individual device.

Worldwide Sales Directory

North America

State	Organization	Telephone	Fax
Alabama	Currie, Peak & Frazier	(205) 536-1506	(205) 551-0558
Alaska	ADI Washington	(206) 575-6344	(206) 575-3351
Arizona	Piper Sales	(602) 949-0048	(602) 894-1032
Arkansas	ADI Dallas	(214) 231-5094	(214) 231-9943
California	ADI Campbell	(408) 559-2037	(408) 559-4783
	ADI Santa Ana	(714) 641-9391	(714) 641-3937
	ADI San Diego	(619) 268-4621	(619) 268-4671
Colorado	Piper Sales	(303) 443-5337	(303) 651-2378
Connecticut			
Fairfield Co.	Harwood-Sandler Assoc.	(516) 673-1900	(516) 673-2848
All Others	ADI Hartford	(203) 633-5964	(203) 659-4572
Delaware	ADI Philadelphia	(215) 643-7790	(215) 643-6198
Florida	Currie, Peak & Frazier		
	Melbourne	(407) 724-6795	(407) 951-9717
	Orlando	(407) 855-0843	(407) 851-1464
	Tampa	(813) 963-1076	(813) 968-2480
Georgia	Currie, Peak & Frazier	(404) 497-9404	(404) 497-9412
Hawaii	ADI Santa Ana	(714) 641-9391	(714) 641-3937
Idaho	Piper Sales	(801) 466-9336	(801) 466-9405
Illinois			
Southern	Technical Sales	(314) 521-2044	(314) 521-1359
Northern	Torkelson Assoc.	(312) 945-8700	(312) 520-1332
Indiana	Torkelson Assoc.	(317) 244-7867	(317) 244-7878
Iowa	Torkelson Assoc.	(319)-373-0200	(319) 373-0144
Kansas	Technical Sales	(913) 829-2800	(913) 829-9549
Kentucky	Currie, Peak & Frazier	(615) 459-0743	(205) 551-0558
Louisiana	ADI Dallas	(214) 231-5094	(214) 231-9943
Maine	ADI Norwood	(617) 329-4700	(617) 326-8703
Maryland	ADI Columbia	(301) 992-1994	(301) 992-1823
Massachusetts	ADI Norwood	(617) 329-4700	(617) 326-8703
Michigan	Rathsburg Assoc.	(313) 489-1500	(313) 489-1480
Minnesota	Torkelson Assoc.	(612) 835-2414	(612) 835-5470
Mississippi	Currie, Peak & Frazier	(205) 536-1506	(205) 551-0558
Missouri	Technical Sales	(314) 521-2044	(314) 521-1359
Montana	Piper Sales	(801) 466-9336	(801) 466-9405
Nebraska	Technical Sales	(913) 829-2800	(913) 829-9549
Nevada	Piper Sales	(505) 828-1300	(505) 828-1380
New Hampshire	ADI Norwood	(617) 329-4700	(617) 326-8703

State	Organization	Telephone	Fax
New Jersey			
Southern	ADI New York	(716) 425-4101	(716) 425-1112
Northern	Harwood-Sandler Assoc.	(516) 673-1900	(516) 673-2848
New Mexico	Piper Sales	(505) 828-1300	(505) 828-1380
New York			
New York	Harwood-Sandler Assoc.	(516) 673-1900	(516) 673-2848
Rochester	BBD Electronics	(716) 425-4101	(716) 425-1112
North Carolina	Currie, Peak & Frazier	(919) 373-0380	(919) 273-6308
North Dakota	Torkelson Assoc.	(612) 835-2414	(612) 835-5470
Ohio			
Northern	J. R. Thornberry Assoc.	(216) 248-4995	(216) 248-0026
Southern	ADI Columbus	(614) 764-8795	(614) 792-1102
Oklahoma	ADI Dallas	(214) 231-5094	(214) 231-9943
Oregon	ADI Seattle	(206) 575-6344	(206) 575-3351
Pennsylvania	ADI Philadelphia	(215) 643-7790	(215) 643-6198
Rhode Island	ADI Norwood	(617) 329-4700	(617) 326-8703
South Carolina	Currie, Peak & Frazier	(919) 373-0380	(919) 273-6308
South Dakota	Torkelson Assoc.	(612) 835-2414	(612) 835-5470
Tennessee	Currie, Peak & Frazier	(615) 459-0743	(205) 551-0558
Texas			
Dallas	ADI Dallas	(214) 231-5094	(214) 231-9943
El Paso	Piper Sales	(505) 828-1300	(505) 828-1380
Utah	Piper Sales	(801) 466-9336	(801) 466-9405
Vermont	ADI Norwood	(617) 329-4700	(617) 326-8703
Virginia	ADI Columbia	(301) 992-1994	(301) 992-1823
Washington	ADI Seattle	(206) 575-6344	(206) 575-3351
West Virginia	J. R. Thornberry	(412) 745-8441	(412) 745-8443
Wisconsin	Torkelson Assoc.	(414) 784-7736	(414) 784-7969
Wyoming	Piper Sales	(801) 466-9336	(801) 466-9405
Canada			
Montreal	BBD Electronics	(514) 697-0804	(514) 697-0277
Ottawa	BBD Electronics	(613) 729-0023	(613) 729-4256
Toronto	BBD Electronics	(416) 821-7800	(416) 821-4541
Mexico	Canadien	(5283) 351721 (5283) 351661	(5283) 357487
Puerto Rico	ADI Norwood	(617) 329-4700	(617) 326-8703

International

Country	Organization	Telephone	Fax
Australia	Avisun Pty. Ltd.	(02) 4178777	(02) 4178940
Austria	ADI Austria	(222) 885504-0	(222) 88550685
Belgium	ADI Belgium	(3) 2371672	(3) 237 8412
Brazil	Hitech, Comercial E Industrial LTDA	(11) 531 9355	(11) 240 2650
Denmark	ADI Denmark	(42) 845800	(42) 840322
Finland	Oy SW-Instruments	(0) 8041 041	(0) 881911
France	ADI France	(1) 466 62525	(1) 46662412
Holland	ADI Holland	(1620) 81500	(1620) 26819
Hong Kong	General Engineers Hong Kong	(2) 8339013	(2) 8345508
India	Analog Sales (India) Pvt. Ltd.	(212) 333880 (812) 560506	(212) 660688 (812) 213281
Israel	ADI Israel	(52) 911415 (52) 914461	(52) 914261
Italy	ADI Italy	(2) 614 0977 (2) 614 3484 (2) 614 3459	(2) 614 1232
	Dott Ing Guiseppe de Mico Spa	(2) 9520551	(2) 9522227
Japan	ADI Japan	(3) 263 6826	(3) 221 5187
Korea	AD Korea	(2) 554 3301	(2) 554 2261
Mexico	Canadien	(83) 351721 (83) 351661	(83) 357487
New Zealand	W. Arthur Fisher Ltd.	(9) 592 629	(9) 597 854
Norway	BIT Elektronik A.S.	(3) 847099	(3) 84 5510
People's Republic of China	Excelpoint Company Ltd.	(1) 890721 X120	(1) 831 4577
Singapore	Excelpoint Systems Pte. Ltd.	2848537	284 8547
South Africa	Analoig Data Products cc	(11) 882 1620	(11) 882 1630
Spain	Diode Espana SA	(1) 555 3686	(1) 556 7159
Sweden	ADI Sweden	(8) 282740	(8) 292842
Switzerland	ADI Switzerland	(22) 7315760	(22) 731 9154
Taiwan	Micro Electronics Co.	(2) 7198419	(2) 719 7916
Turkey	Elektro	(1) 3372245	(1) 3368814
United Kingdom	ADI Ltd.	(932) 232222	(932) 247401
West Germany	ADI West Germany	(89) 570050	(89) 57005157

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